DATASHEET
FOR
256M BIT SPI NOR FLASH

BY25FQ256ES

Features

- **Serial Peripheral Interface**
  - Standard SPI: SCLK, /CS, SI, SO, /WP, /HOLD
  - Dual SPI: SCLK, /CS, IO0, IO1, /WP, /HOLD
  - Quad SPI: SCLK, /CS, IO0, IO1, IO2, IO3
  - QPI: SCLK, /CS, IO0, IO1, IO2, IO3
  - DTR (Double Transfer Rate) Read
  - 3 or 4-Byte Addressing Mode
- **Read**
  - Allows XIP (execute in place) Operation
  - Continuous Read with 8/16/32/64-byte Wrap
- **Program**
  - Serial-input Page Program up to 256bytes
  - Program Suspend and Resume
- **Erase**
  - Block Erase (64/32 KB)
  - Sector Erase (4 KB)
  - Chip Erase
  - Erase Suspend and Resume
- **High Speed Clock Frequency**
  - 133MHz for fast read
  - Dual I/O Data transfer up to 300Mbits/s
  - Quad I/O Data transfer up to 600Mbits/s
  - QPI Mode Data transfer up to 600Mbits/s
  - DTR Data transfer up to 800Mbits/s
- **Program/Erase Speed**
  - Page Program time: 0.3ms typical
  - Sector Erase time: 25ms typical
  - Block Erase time: 60ms/100ms typical
  - Chip Erase time: 45s typical
- **Flexible Architecture**
  - Sector of 4K-byte
  - Block of 32/64K-byte
- **Low Power Consumption**
  - 12mA typical active current
  - 1uA typical power down current
- **Software/Hardware Write Protection**

- 3x1024-Byte Security Registers with OTP Locks
  - Discoverable Parameters (SFDP) register
  - Enable/Disable protection with /WP Pin
  - Top/Bottom, Complement array protection
  - Individual Block Memory Protection
- **Temperature Range**
  - Commercial (-40℃ to +85℃)
  - Industrial (-40℃ to +85℃)
  - Industrial (-40℃ to +105℃)
  - Industrial (-40℃ to +125℃)
- **Cycling Endurance/Data Retention**
  - Typical 100k Program-Erase cycles on any sector
  - Typical 20-year data retention
- **Package Information**
  - SOP 8 - 208mil
  - SOP16 - 300mil
  - WSON8 - 5x6mm
  - WSON8 - 6x8mm

Contents

1. Description

The BY25FQ256 is 256M-bit Serial Peripheral Interface(SPI) Flash memory, supports the Dual/Quad SPI: Serial Clock, Chip Select, Serial Data I/O0 (SI), I/O1 (SO), I/O2 (/WP), and I/O3 (/HOLD), Reset; and supports the QPI: Serial Clock, Chip Select, I/O0, I/O1, I/O2, and I/O3, Reset; The Dual I/O data is transferred with speed of 266Mbits/s and the Quad I/O & Quad output & QPI data is transferred with speed of 532Mbits/s. The Double Transfer Rate (DTR) Read is transferred with speed of 528Mbits/s. The device uses a single low voltage power supply, ranging from 2.7 Volt to 3.6 Volt.

Additionally, the device supports JEDEC standard manufacturer and device ID and three 1024-bytes Security Registers.

In order to meet environmental requirements, Boya Microelectronics offers 8-pin SOP 208mil, 8-pad WSON 5x6-mm, 8-pad WSON 6x8-mm,16-pin SOP 300mil, and other special-order packages, please contacts Boya Microelectronics for ordering information.

Figure 1. Logic diagram

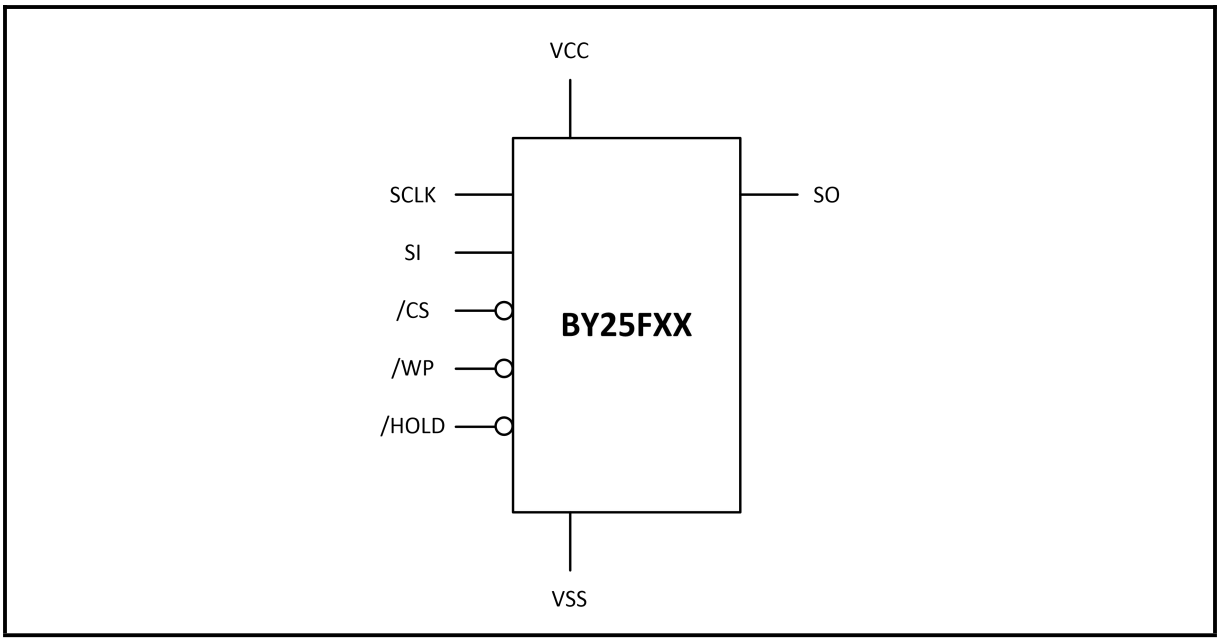


Figure 2. Pin Configuration SOP 208 mil

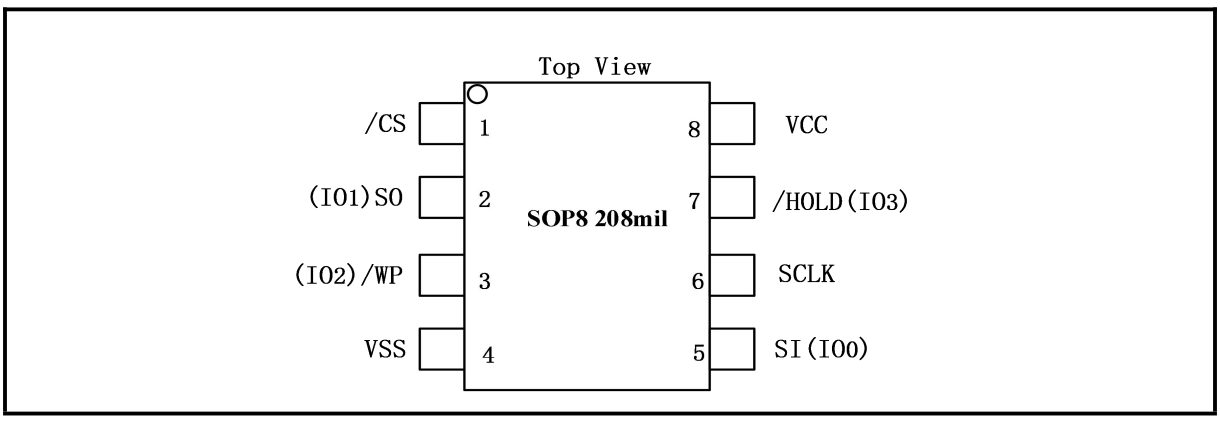


Figure 3. Pin Configuration WSON 5x6-mm and WSON 6*8-mm

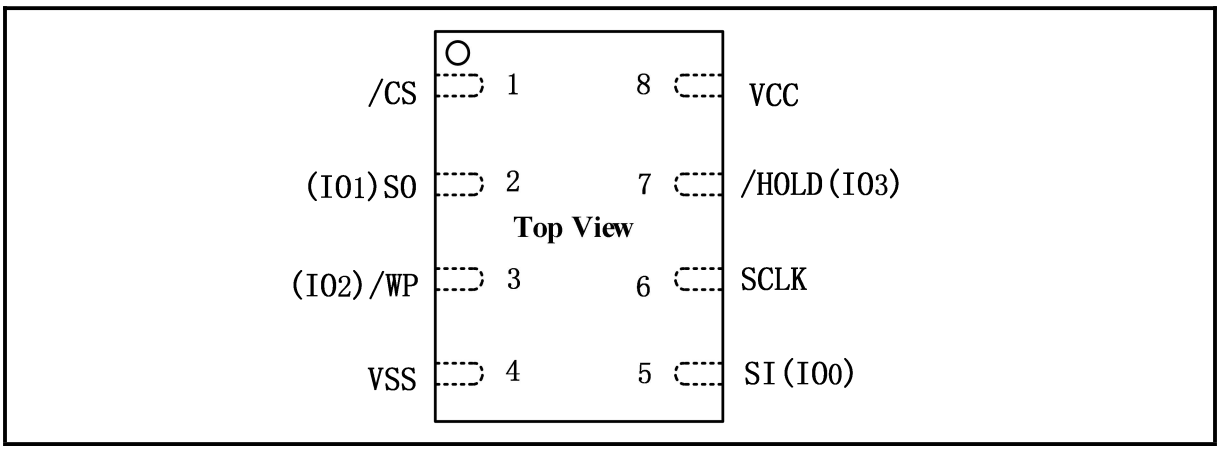
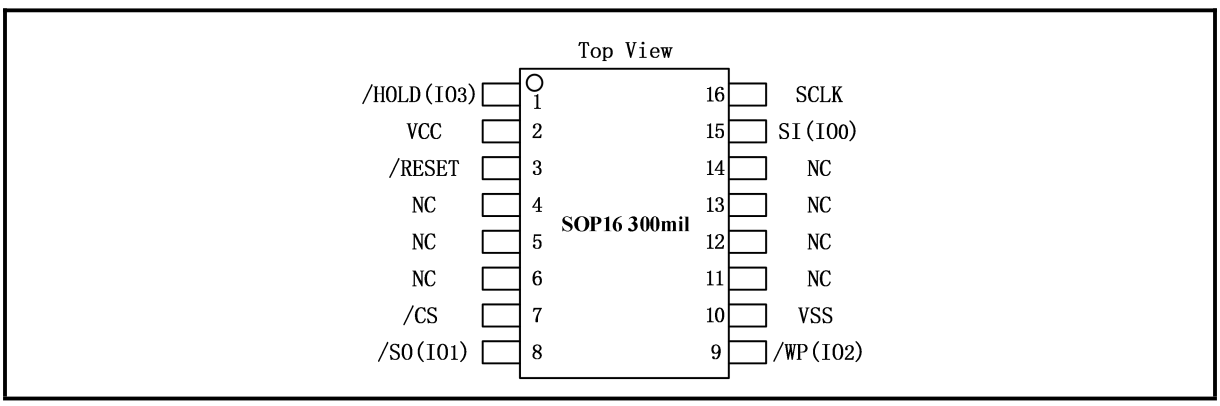


Figure 4. Pin Configuration SOP16 300 mil



2. Signal Description

During all operations, VCC must be held stable and within the specified valid range: VCC (min) to VCC (max).

All of the input and output signals must be held High or Low (according to voltages of VIH, VOH, VIL or VOL, see ***DC Electrical Characteristics***). These signals are described next.

2.1 Input/Output Summary

Table 1. Signal Names

Pin Name	I/O	Description
/CS	I	Chip Select
SO (IO1)	I/O	Serial Output for single bit data Instructions. IO1 for Dual or Quad Instructions
/WP (IO2)	I/O	Write Protect in single bit or Dual data Instructions. IO2 in Quad mode. The signal has an internal pull-up resistor and may be left unconnected in the host system if not used for Quad Instructions
VSS		Ground
SI (IO0)	I/O	Serial Input for single bit data Instructions. IO0 for Dual or Quad Instructions
SCLK	I	Serial Clock
/HOLD/RESET (IO3)(1)	I/O	Hold (pause) serial transfer in single bit or Dual data Instructions when QE=0, HOLD/RST=0. IO3 in Quad-I/O/QPI mode. Also can be configured either as a /RESET pin when QE=0, HOLD/RST=1. The signal has an internal pull-up resistor and may be left unconnected in the host system if not used for Quad Instructions
/RESET(1)	I	Reset input
VCC		Core and I/O Power Supply

2.2 Chip Select (/CS)

The chip select signal indicates when an instruction for the device is in process and the other signals are relevant for the memory device. When the /CS signal is at the logic high state, the device is not selected and all input signals are ignored and all output signals are high impedance. Unless an internal Program, Erase or Write Status Registers embedded operation is in progress, the device will be in the Standby Power mode. Driving the /CS input to logic low state enables the device, placing it in the Active Power mode. After Power Up, a falling edge on /CS is required prior to the start of any instruction.

2.3 Serial Clock (SCLK)

This input signal provides the synchronization reference for the SPI interface. Instructions, addresses, or data input are latched on the rising edge of the SCLK signal. Data output changes after the falling edge of SCLK.

2.4 Serial Input (SI)/IO0

This input signal is used to transfer data serially into the device. It receives instructions, addresses, and data to be programmed. Values are latched on the rising edge of serial SCLK clock signal.

SI becomes IO0 an input and output during Dual and Quad Instructions for receiving instructions, addresses, and data to be programmed (values latched on rising edge of serial SCLK clock signal) as well as shifting out data (on the falling edge of SCLK).

2.5 Serial Data Output (SO)/IO1

This output signal is used to transfer data serially out of the device. Data is shifted out on the falling edge of the serial SCLK clock signal.

SO becomes IO1 an input and output during Dual and Quad Instructions for receiving instructions, addresses, and data to be programmed (values latched on rising edge of serial SCLK clock signal) as well as shifting out data (on the falling edge of SCLK).

2.6 Write Protect (/WP)/IO2

When /WP is driven Low (VIL), while the Status Register Protect bits (SRP1 and SRP0) of the Status Registers (SR2[0] and SR1[7]) are set to 0 and 1 respectively, it is not possible to write to the Status Registers. This prevents any alteration of the Status Registers. As a consequence, all the data bytes in the memory area that are protected by the Block Protect, BP4, BP3 bits in the status registers, are also hardware protected against data modification while /WP remains Low. The /WP function is not available when the Quad mode is enabled (QE) in Status Register 2 (SR2[1]=1).

The /WP function is replaced by IO2 for input and output during Quad mode for receiving addresses, and data to be programmed (values are latched on rising edge of the SCLK signal) as well as shifting out data (on the falling edge of SCLK). /WP has an internal pull-up resistance; when unconnected; /WP is at VIH and may be left unconnected in the host system if not used for Quad mode.

2.7 HOLD (/HOLD) /RESET /IO3

The /HOLD function is only available when QE=0, which can be configured either as a /HOLD pin or as a /RESET pin depending on Status Register setting. If QE=1, the /HOLD function is disabled, the pin acts as dedicated data I/O pin, and the /HOLD or /RESET function is not available.

When QE=0 and HOLD/RES= 0, the /HOLD signal goes low to stop any serial communications with the device, but doesn't stop the operation of write status register, programming, or erasing in progress.

The operation of HOLD, need /CS keep low, and starts on falling edge of the /HOLD signal, with SCLK signal being low (if SCLK is not being low, HOLD operation will not start until SCLK being low). The HOLD condition ends on rising edge of /HOLD signal with SCLK being low (If SCLK is not being low, HOLD operation will not end until SCLK being low).

2.8 RESET

The /RESET pin in 16-pin SOP 300mil packages allows the device to be reset by the controller.

2.9 VCC Power Supply

VCC is the supply voltage. It is the single voltage used for all device functions including read, program, and erase.

2.10 VSS Ground

VSS is the reference for the VCC supply voltage.

3. Block/Sector Addresses

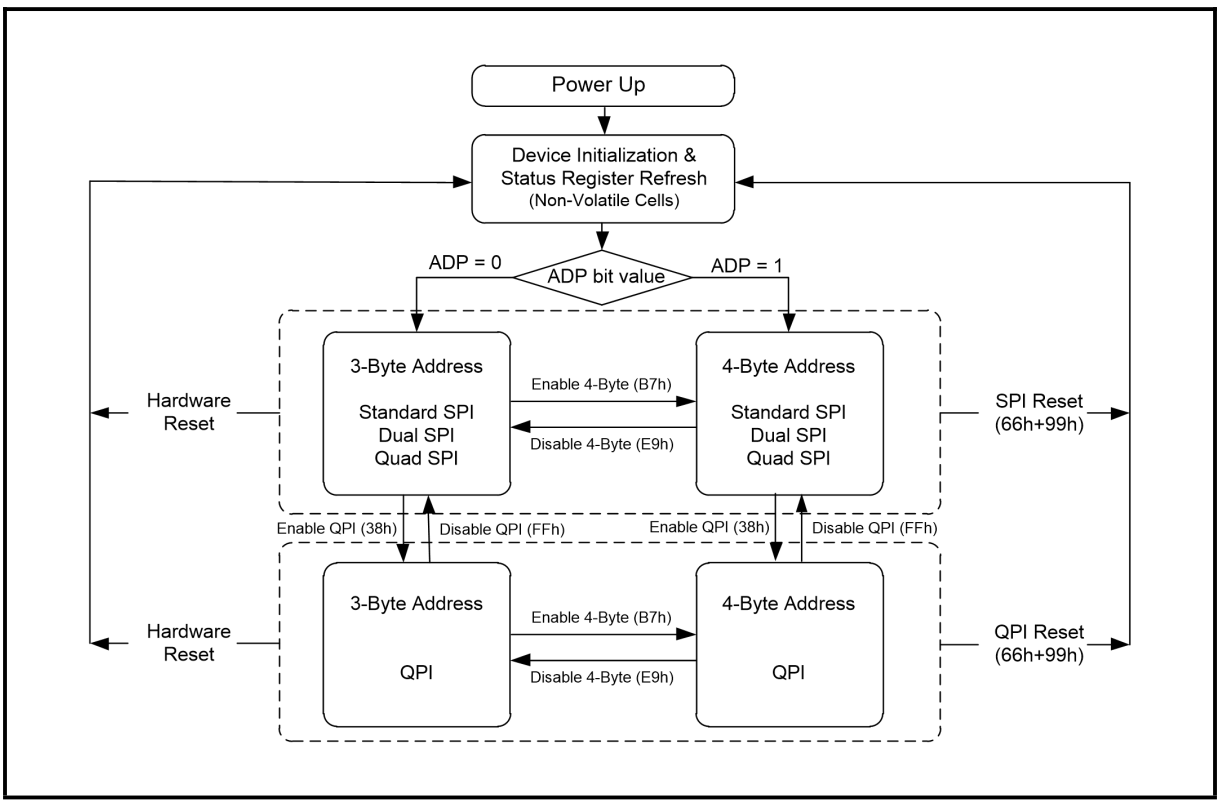
Table 2. Block/Sector Addresses of BY25FQ256

Memory Density	Big Block (4M bit)	Block (64k byte)	Block (32k byte)	Sector No.	Sector Size (KB)	Address range
256Mbit	Big Block 0	Block 0	Half block 0	Sector 0	4	0000000h-0000FFFh
				:	:	:
				Sector 7	4	0007000h-0007FFFh
			Half block 1	Sector 8	4	0008000h-0008FFFh
				:	4	:
				Sector 15	4	000F000h-000FFFFh
		:	:	:	:	:
		Block 7	Half block 14	Sector 112	4	0070000h-0070FFFh
				:	:	:
				Sector 119	4	0077000h-0077FFFh
			Half block 15	Sector 120	4	0078000h-0078FFFh
				:	:	:
				Sector 127	4	007F000h-007FFFFh
	:	:	:	:	:	:
	Big Block 63	Block 504	Half block 1008	Sector 8064	4	1F80000h-1F80FFFh
				:	:	:
				Sector 8071	4	1F87000h-1F87FFFh
			Half block 1009	Sector 8072	4	1F88000h-1F88FFFh
				:	:	:
				Sector 8079	4	1F8F000h-1F8FFFFh
		:	:	:	:	:
		Block 511	Half block 1022	Sector 8176	4	1FF0000h-1FF0FFFh
				:	:	:
				Sector 8183	4	1FF7000h-1FF7FFFh
			Half block 1023	Sector 8184	4	1FF8000h-1FF8FFFh
				:	:	:
				Sector 8191	4	1FFF000h-1FFFFFFh

Notes:
1. Big Block = Uniform Big Block, and the size is 4M bits.
2. Block = Uniform Block, and the size is 64K bytes.
3. Half block = Half Uniform Block, and the size is 32k bytes.
4. Sector = Uniform Sector, and the size is 4K bytes.

4. SPI/QPI Operation

Figure 5. BY25FQ256 Serial Flash Memory Operation Diagram



4.1 Standard SPI Instructions

The BY25FQ256 features a serial peripheral interface on 4 signals bus: Serial Clock (SCLK), Chip Select (/CS), Serial Data Input (SI) and Serial Data Output (SO). Both SPI bus mode 0 and 3 are supported. Input data is latched on the rising edge of SCLK and data shifts out on the falling edge of SCLK.

4.2 Dual SPI Instructions

The BY25FQ256 supports Dual SPI operation when using the “3BH”, “3CH”, “BBH”, “BCH”, and “92H” instructions. These instructions allow data to be transferred to or from the device at two times the rate of the standard SPI. When using the Dual SPI instruction the SI and SO pins become bidirectional I/O pins: IO0 and IO1.

4.3 Quad SPI Instructions

The BY25FQ256 supports Quad SPI operation when using the “6BH”, “6CH”, “EBH”, “EDH”, “ECH”, “94H”, “32H”, and “34H” instructions. These instructions allow data to be transferred to or from the device at four times the rate of the standard SPI. When using the Quad SPI instruction the SI and SO pins become bidirectional I/O pins: IO0 and IO1, and /WP and /HOLD pins become IO2 and IO3. Quad SPI instructions require the non-volatile Quad Enable bit (QE) in Status Register to be set.

4.4 QPI Instructions

The BY25FQ256 supports Quad Peripheral Interface (QPI) operations only when the device is switched from Standard/Dual/Quad SPI mode to QPI mode using the “Enter QPI (38h)” instruction. The typical SPI protocol requires that the byte-long instruction code being shifted into the device only via SI pin in eight serial clocks. The QPI mode utilizes all four IO pins to input the instruction code, thus only two serial clocks are required. Standard/Dual/Quad SPI mode and QPI mode are exclusive. Only one mode can be active at any given time. “Enter QPI (38h)” and “Exit QPI (FFh)” instructions are used to switch between these two modes. Upon power-up or after a software reset using “Reset (99h)” instruction or Hardware Reset, the default state of the device is Standard/Dual/Quad SPI mode. To enable QPI mode, the non-volatile Quad Enable bit (QE) in Status Register-2 is required to be set. When using QPI instructions, the SI and SO pins become bidirectional IO0 and IO1, and the /WP and /HOLD pins become IO2 and IO3 respectively. See ***Figure 5*** for the device operation modes.

4.5 DTR Instructions

The BY25FQ256 supports DTR operation when using the “DTR Quad I/O Fast Read” (EDH/EEH) instructions or the “Burst Read with Wrap (0Ch)” instruction. These instructions allow data to be transferred to or from the device at eight times the rate of the standard SPI, and data output will be latched on both rising and falling edges of the serial clock. When using the DTR instructions the SI and SO pins become bidirectional I/O pins: IO0 and IO1.

4.6 3-Byte/4-Byte Address Modes

The BY25FQ256 provides two Address Modes that can be used to specify any byte of data in the memory array. The 3-Byte Address Mode is backward compatible to older generations of serial flash memory that only support up to 128M-bit data. To address the 256M-bit or more data in 3-Byte Address Mode, Extended Address Register must be used in addition to the 3-Byte addresses.

4-Byte Address Mode is designed to support Serial Flash Memory devices from 256M-bit to 32G-bit. The extended Address Register is not necessary when the 4-Byte Address Mode is enabled.

Upon power up, the BY25FQ256 can operate in either 3-Byte Address Mode or 4-Byte Address Mode, depending on the Non-Volatile Status Register Bit ADP (S17) setting. If ADP=0, the device will operate in 3-Byte Address Mode; if ADP=1, the device will operate in 4-Byte Address Mode. The factory default value for ADP is 0.

To switch between the 3-Byte and 4-Byte Address Modes, “Enter 4-Byte Address Mode (B7h)” or “Exit 4-Byte Address Mode (E9h)” instructions must be used. The current address mode is indicated by the Status Register Bit ADS (S16).

5. Operation Features

5.1 Supply Voltage

5.1.1 Operating Supply Voltage

Prior to selecting the memory and issuing instructions to it, a valid and stable VCC voltage within the specified [VCC(min), VCC(max)] range must be applied (see ***Electrical Characteristics***). In order to secure a stable DC supply voltage, it is recommended to decouple the VCC line with a suitable capacitor (usually of the order of 10*nF* to 100*nF*) close to the VCC/VSS package pins. This voltage must remain stable and valid until the end of the transmission of the instruction and, for a Write instruction, until the completion of the internal write cycle (tW).

5.1.2 Power-up Conditions

When the power supply is turned on, VCC rises continuously from VSS to VCC. During this time, the Chip Select (/CS) line is not allowed to float but should follow the VCC voltage, it is therefore recommended to connect the /CS line to VCC via a suitable pull-up resistor.

In addition, the Chip Select (/CS) input offers a built-in safety feature, as the /CS input is edge sensitive as well as level sensitive: after power-up, the device does not become selected until a falling edge has first been detected on Chip Select (/CS). This ensures that Chip Select (/CS) must have been High, prior to going Low to start the first operation.

5.1.3 Device Reset

In order to prevent inadvertent Write operations during power-up (continuous rise of VCC), a power on reset (POR) circuit is included. At Power-up, the device does not respond to any instruction until VCC has reached the power on reset threshold voltage (this threshold is lower than the minimum VCC operating voltage defined in ***Power-up Timing***).

When VCC is lower than V_{WI}, the device is reset.

5.1.4 Power-down

At Power-down (continuous decrease in VCC), as soon as VCC drops from the normal operating voltage to below the power on reset threshold voltage(V_{WI}), the device stops responding to any instruction sent to it. During Power-down, the device must be deselected (Chip Select (/CS) should be allowed to follow the voltage applied on VCC) and in Standby Power mode (that is there should be no internal Write cycle in progress).

5.2 Active Power and Standby Power Modes

When Chip Select (/CS) is Low, the device is selected, and in the Active Power mode. The device consumes ICC.

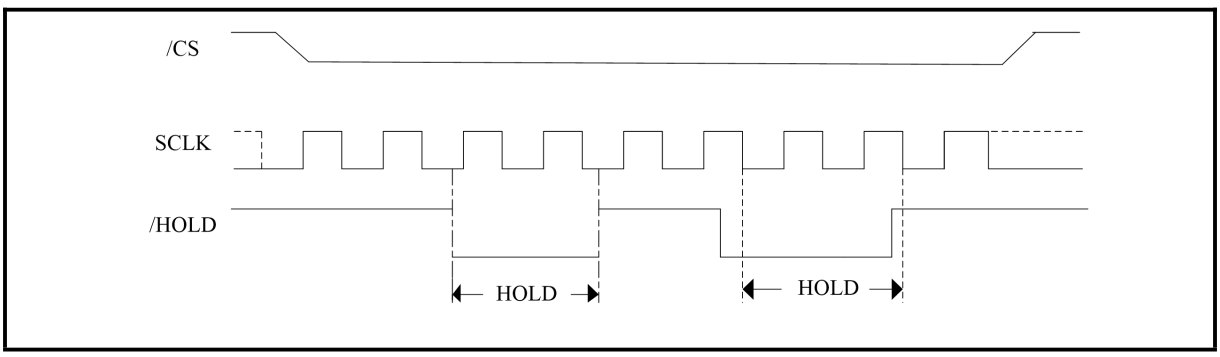
When Chip Select (/CS) is High, the device is deselected. If a Write cycle is not currently in progress, the device then goes in to the Standby Power mode, and the device consumption drops to ICC1.

5.3 Hold Condition

When QE=0, HOLD/RST=0, the Hold (/HOLD) signal is used to pause any serial communications with the device without resetting the clocking sequence. During the Hold condition, the Serial Data Output (SO) is high impedance, and Serial Data Input (SI) and Serial Clock (SCLK) are Don't Care. To enter the Hold condition, the device must be selected, with Chip Select (/CS) Low. Normally, the device is kept selected, for the whole duration of the Hold condition. Deselecting the device while it is in the Hold condition, has the effect of resetting the state of the device, and this mechanism can be used if it is required to reset any processes that had been in progress.

The Hold condition starts when the Hold (/HOLD) signal is driven Low at the same time as Serial Clock (SCLK) already being Low (as shown in ***Figure 6***).The Hold condition ends when the Hold (HOLD) signal is driven High at the same time as Serial Clock (C) already being Low. ***Figure 6*** also shows what happens if the rising and falling edges are not timed to coincide with Serial Clock (SCLK) being Low.

Figure 6. Hold condition activation



5.4 Software Reset & Hardware RESET

5.4.1 Software Reset

The BY25FQ256 can be reset to the initial power-on state by a software reset sequence, either in SPI mode or QPI mode. This sequence must include two consecutive instructions: Enable Reset (66h) & Reset (99h). If the instruction sequence is successfully accepted, the device will take approximately 1uS (tRST) to reset. No instruction will be accepted during the reset period.

5.4.2 Hardware Reset (/HOLD pin or /RESET pin)

The BY25FQ256 can also be configured to utilize hardware /RESET pin. The HOLD/RST bit in the Status Register-3 is the configuration bit for /HOLD pin function or /RESET pin function. When HOLD/RST=0 (factory default), the pin acts as a /HOLD pin as described above; when HOLD/RST=1, the pin acts as a /RESET pin. Drive the /RESET pin low for a minimum period of tRST (1) will reset the device to its initial power-on state. Any on-going Program/Erase operation will be interrupted and data corruption may happen. While /RESET is low, the device will not accept any instruction input.

If QE bit is set to 1, the /HOLD or /RESET function will be disabled, the pin will become one of the four data I/O pin.

For the 16-pin SOP 300mil package, BY25FQ256 provides a dedicated /RESET pin in addition to the /HOLD/RST (IO3) pin. Drive the /RESET pin low for a minimum period of tRST (1) will reset the device to its initial power-on state. The HOLD/RST bit or QE bit in the Status Register will not affect the function of this dedicated /RESET pin.

Hardware /RESET pin has the highest priority among all the input signals. Drive /RESET low for a minimum period of tRST (1) will interrupt any on-going external/internal operations, regardless the status of other SPI signals (/CS, CLK, IOs, /WP and /HOLD).

Notes:

1. While a faster /RESET pulse (as short as a few hundred nanoseconds) will often reset the device, a tRST minimum pulse is recommended to ensure reliable operation.
2. There is an internal pull-up resistor for the dedicated /RESET pin on the 16-pin SOP 300mil package. If the reset function is not used, this pin can be left floating in the system.

5.4.3 Hardware Reset (JEDEC Standard Hardware Reset)

The BY25FQ256 supports JEDEC Standard Hardware Reset. The JEDEC Standard Hardware Reset sequence can also be used to reset the device to its power on state without cycling power.

The reset sequence does not use the SCLK pin. The SCLK has to be low (mode 0) or high (mode 3) through the entire reset sequence. This prevents any confusion with a instruction, as no instruction bits are transferred (clocked).

A reset is commanded when the data on the SI pin is 0101 on four consecutive positive edges of the /CS pin with no edge on the SCLK pin throughout. The is a sequence where

1. /CS is driven active low to select the device.
2. Clock (SCLK) remains stable in either a high or low state.
3. SI is driven low by the bus master, simultaneously with /CS going active low. No SPI bus slave drives SI during /CS low before a transition of SCLK i.e.: slave streaming output active is not allowed until after the first edge of SCLK.
4. /CS is driven inactive. The slave captures the state of SI on the rising edge of /CS.

The above steps are repeated 4 times, each time alternating the state of SI.

After the fourth /CS pulse, the slave triggers its internal reset. SI is low on the first /CS, high on the second, low on the third, high on the fourth. This provides a value of 5H, unlike random noise. Any activity on SCLK during this time will halt the sequence and a Reset will not be generated. Figure below illustrates the timing for hardware Reset operation.

Figure 7. JEDEC Standard Hardware Reset

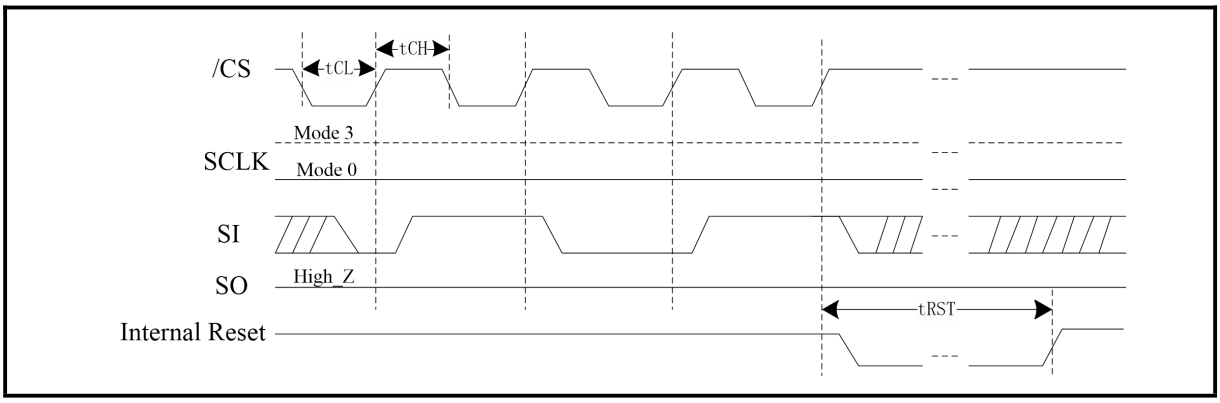


Table 3. JEDEC Standard Hardware Reset Timing Parameters

Parameter	Min.	Typ.	Max.	Unit.
tCL	20			ns
tCH	20			ns
Setup Time	5			ns
Hold Time	5			ns

5.5 Write Protect Features

1. Software Protection (Memory array):

   - The Block Protect (BP4, BP3, BP2, BP1, BP0) bits define the section of the memory array that can be read but not change.

   - Individual Block Memory Protection: The BY25FQ256 also provides another Write Protect method using the Individual Block Memory Protection. Each 64KB block (except the top and bottom blocks, total of 510 blocks) and each 4KB sector within the top/bottom blocks (total of 32 sectors) are equipped with the Individual Block/Sector Lock bit. When the Individual Block/Sector Lock bit is 0, the corresponding sector or block can be erased or programmed; When the Individual Block/Sector Lock bit is set to 1, Erase or Program instructions issued to the corresponding sector or block will be ignored.

   The WPS bit in Status Register-3 is used to decide which Write Protect scheme should be used. When WPS=0 (factory default), the device will only utilize CMP, BP[4:0] bits to protect specific areas of the array; When WPS=1, the device will utilize the Individual Block Memory Protection for write protection.

2. Hardware Protection (Status register): /WP going low to protected the writable bits of Status Register.

3. Deep Power-Down: In Deep Power-Down Mode, all instructions are ignored except the Release from deep Power-Down Mode instruction.

4. Device resets when VCC is below threshold: Upon power-up or at power-down, the BY25FQ256 will maintain a reset condition while VCC is below the threshold value of V_{WI}. While reset, all operations are disabled and no instructions are recognized.

5. Time delay write disable after Power-up: During power-up and after the VCC voltage exceeds VCC $_{(min)}$, all program and erase related instructions are further disabled for a time delay of tVSL. This includes the Write Enable, Page Program, Sector Erase, Block Erase, Chip Erase and the Write Status Register instructions.

6. Write Enable: The Write Enable instruction is set the Write Enable Latch bit. The WEL bit will return to reset by following situation:

   -Power –up
   -Write Disable
   -Write Status Register (Whether the SR is protected, WEL will return to reset)
   -Write Extended Address Register (when in 3-Byte Address Mode)
   -After some Individual Block Memory Protection instructions that need Write Enable instruction (see Table 13) are executed correctly, WEL bit will return to reset (when WPS=1)
   -Page Program (Whether the program area is protected, WEL will return to reset)
   -Sector Erase/Block Erase/Chip Erase (Whether the erase area is protected, WEL will return to reset)
   -Software Reset
   -Hardware Reset

7. One Time Program (OTP) write protection for array and Security Registers using Status Register.

5.6 Status Register

5.6.1 Status Register Table

See ***Table 4*** for detail description of the Status Register bits.

Table 4. Status Register

	SR3							
	S23	**S22**	**S21**	**S20**	**S19**	**S18**	**S17**	**S16**
	HOLD/RST	**DRV1**	**DRV0**	**DC1**	**DC0**	**WPS**	**ADP**	**ADS**
Default (1)	0	0	0	0	0	0	0	0
						OTP		Read only

	SR2							
	S15	**S14**	**S13**	**S12**	**S11**	**S10**	**S9**	**S8**
	SUS1	**CMP**	**LB3**	**LB2**	**LB1**	**SUS2**	**QE**	**SRP1**
Default (1)	0	0	0	0	0	0	0	0
	Read Only		OTP	OTP	OTP	Read Only		

	SR1							
	S7	**S6**	**S5**	**S4**	**S3**	**S2**	**S1**	**S0**
	SRP0	**BP4**	**BP3**	**BP2**	**BP1**	**BP0**	**WEL**	**WIP**
Default (1)	0	0	0	0	0	0	0	0
							Read Only	Read Only

Notes:
1. The default value is set by Manufacturer during wafer sort, Marked as Default in following text

5.6.2 The Status and Control Bits

5.6.2.1 WIP bit

The Write in Progress (WIP) bit indicates whether the memory is busy in program/erase/write status register progress. When WIP bit sets to 1, means the device is busy in program/erase/write status register progress, when WIP bit sets 0, means the device is not in program/erase/write status register progress.

5.6.2.2 WEL bit

The Write Enable Latch (WEL) bit indicates the status of the internal Write Enable Latch. When set to 1 the internal Write Enable Latch is set, when set to 0 the internal Write Enable Latch is reset and no Write Status Register, Program or Erase, etc. instruction is accepted.

5.6.2.3 BP4, BP3, BP2, BP1, BP0 bits

The Block Protect (BP4, BP3, BP2, BP1, BP0) bits are non-volatile. They define the size of the area to be software protected against Program and Erase instructions. These bits are written with the Write Status Register instruction. When WPS=0, and the Block Protect (BP4, BP3, BP2, BP1, BP0) bits are set to 1, the relevant memory area (as defined in ***Table 7-Table 8***).becomes protected against Page Program, Sector Erase and Block Erase instructions. The Block Protect (BP4, BP3, BP2, BP1, BP0) bits can be written provided that the Hardware Protected mode has not been set. The Chip Erase instruction is executed, if the Block Protect (BP2, BP1, BP0) bits are 0 and CMP=0 or The Block Protect (BP2, BP1, BP0) bits are 1 and CMP=1.

5.6.2.4 SRP1, SRP0 bits

The Status Register Protect (SRP1 and SRP0) bits are non-volatile Read/Write bits in the status register. The SRP bits control the method of write protection: software protection, hardware protection, power supply lock-down or one time programmable protection.

Table 5. Status Register protect table

SRP1	SRP0	/WP	Status Register	Description
0	0	X	Software Protected	The Status Register can be written to after a Write Enable instruction, WEL=1.(Factory Default)
0	1	0	Hardware Protected	/WP=0, the Status Register locked and cannot be written.
0	1	1	Hardware Unprotected	/WP=1, the Status Register is unlocked and can be written to after a Write Enable instruction, WEL=1.
1	0	X	Power Supply Lock-Down(1)	Status Register is protected and cannot be written to again until the next Power-Down, Power-Up cycle.
1	1	X	One Time Program(2)	Status Register is permanently protected and cannot be written to.

Notes:

1. When SRP1, SRP0= (1, 0), a Power-Down, Power-Up cycle will change SRP1, SRP0 to (0, 0) state.
2. The One time Program feature is available upon special order. Please contact Boya Microelectronics for details.

5.6.2.5 QE bit

The Quad Enable (QE) bit is a non-volatile Read/Write bit in the Status Register that allows Quad operation. When the QE bit is set to 0 (Default) the /WP pin and /HOLD pin are enable. When the QE pin is set to 1, the Quad IO2 and IO3 pins are enabled. (The QE bit should never be set to 1 during standard SPI or Dual SPI operation if the /WP or /HOLD pins directly to the power supply or ground).

QE bit is required to be set to a 1 before issuing an “Enter QPI (38h)” to switch the device from Standard/Dual/Quad SPI to QPI; otherwise the instruction will be ignored. When the device is in QPI mode, QE bit will remain to be 1. A “Write Status Register” instruction in QPI mode cannot change QE bit from “1” to “0”.

5.6.2.6 LB3/LB2/LB1 bits

The Security Register Lock (LB3/LB2/LB1) bits are non-volatile One Time Program (OTP) bits in Status Register (S13–S11) that provide the write protect control and status to the Security Registers. The default state of LB is 0, the security registers are unlocked. LB can be set to 1 individually using the Write Register instruction. LB is One Time Programmable, once they are set to 1, the Security Registers will become read-only permanently.

5.6.2.7 CMP bit

The Complement Protect (CMP) bit is a non-volatile Read/Write bit in the Status Register (S14). It is used in conjunction the BP4-BP0 bits to provide more flexibility for the array protection. Please see the Status registers Memory Protection table for details. The default setting is CMP=0.

5.6.2.8 SUS1/SUS2 bits

The Suspend Status (SUS1 and SUS2) bits are read only bits in the status register2 (S15 and S10) that are set to 1 after executing a Program/Erase Suspend (75H) instruction (The Erase Suspend will set SUS1 to 1, and the Program Suspend will set the SUS2 to 1). The SUS1 and SUS2 bits are cleared to 0 by Program/Erase Resume (7AH) instruction as well as a power-down, power-up cycle.

5.6.2.9 ADS bit

The Current Address Mode (ADS) bit is a read only bit in the Status Register3 that indicates which address mode the device is currently operating in. When ADS=0, the device is in the 3-Byte Address Mode, when ADS=1, the device is in the 4-Byte Address Mode.

5.6.2.10 ADP bit

The Power-Up Address Mode (ADP) bit is a non-volatile bit that determines the initial address mode when the device is powered on or reset. This bit is only used during the power on or device reset initialization period, and it is only writable by the non-volatile Write Status sequence (06h + 11h). When ADP=0 (factory default), the device will power up into 3-Byte Address Mode, the Extended Address Register must be used to access memory regions beyond 128Mb. When ADP=1, the device will power up into 4-Byte Address Mode directly.

5.6.2.11 HOLD/RST bit

The /HOLD or /RESET Pin Function (HOLD/RST) bit is used to determine whether /HOLD or /RESET function should be implemented on the hardware pin. When HOLD/RST=0 (factory default), the pin acts as /HOLD; when HOLD/RST=1, the pin acts as /RESET. However, /HOLD or /RESET functions are only available when QE=0. If QE is set to 1, the /HOLD and /RESET functions are disabled, the pin acts as a dedicated data I/O pin.

5.6.2.12 WPS bit

There are two write memory array protection methods provided on BY25FQ256：Block Protection (BP) mode or Individual Block Memory Protection mode. The protection modes are mutually exclusive. The WPS bit selects which protection mode is enabled. Please note that the WPS bit is an OTP bit. Once WPS is set to “1”, it cannot be programmed back to “0”.

If WPS=0 (factory default), the BP mode is enabled and Individual Block Memory Protection mode is disabled. Please note that if WPS=0, all Individual Block Memory Protection instructions are not available.

If WPS=1, the Individual Block Memory Protection mode is enabled and BP mode is disabled. Blocks or Sectors are individually protected by their own Individual Block/Sector Lock bit. On power-up, all Blocks or Sectors are write protected by the Individual Block/Sector Lock bits by default. The Individual Block Memory Protection instructions are activated. The CMP, BP[4:0] bits of the Status Register are disabled and have no effect.

5.6.2.13 DC1/DC0 bit

The Dummy Configuration (DC) bit is non-volatile, which selects the number of dummy cycles between the end of address and the start of read data output. Dummy cycles provide additional latency that is needed to complete the initial read access of the flash array before data can be returned to the host system. Some read commands require additional dummy cycles as the SCLK frequency increases.

The following dummy cycle tables provide different dummy cycle settings that are configured.

(STR Mode)

-40 ~ +85C：

DC bit	Numbers of Dummy Cycles(1)	Dual IO Fast Read(BBH)	Fast Read Dual I/O with 4-Byte Address (BCh)
00 (default)	4	108/120R(2) MHz	108/120R(2) MHz
01	8	133/150R(2) MHz	133/150R(2) MHz
10	12	133/150R(2) MHz	133/150R(2) MHz
11	16	133/150R(2) MHz	133/150R(2) MHz

-40 ~ +105C：

DC bit	Numbers of Dummy Cycles(1)	Dual IO Fast Read(BBH)	Fast Read Dual I/O with 4-Byte Address (BCh)
00 (default)	4	108/120R(2) MHz	108/120R(2) MHz
01	8	133/150R(2) MHz	133/150R(2) MHz
10	12	133/150R(2) MHz	133/150R(2) MHz
11	16	133/150R(2) MHz	133/150R(2) MHz

-40 ~ +125C：

DC bit	Numbers of Dummy Cycles(1)	Dual IO Fast Read(BBH)	Fast Read Dual I/O with 4-Byte Address (BCh)
00 (default)	4	108/120R(2) MHz	108/120R(2) MHz
01	8	133/150R(2) MHz	133/150R(2) MHz
10	12	133/150R(2) MHz	133/150R(2) MHz
11	16	133/150R(2) MHz	133/150R(2) MHz

Notes:
1. The number of dummy includes M7-0.
2. "R" mean VCC range= 3.0V-3.6V.

-40 ~ +85C：

DC bit	Numbers of Dummy Cycles(1)	Quad I/O Fast Read (EBH)	Fast Read Quad I/O with 4-Byte Address (ECH)
00	6	100/108R(2) MHz	100/108R(2) MHz
01	10	133/150R(2) MHz	133/150R(2) MHz
10	14	133/150R(2) MHz	133/150R(2) MHz
11	18	133/150R(2) MHz	133/150R(2) MHz

-40 ~ +105C：

DC bit	Numbers of Dummy Cycles(1)	Quad I/O Fast Read (EBH)	Fast Read Quad I/O with 4-Byte Address (ECH)
00	6	100/108R(2) MHz	100/108R(2) MHz
01	10	120/133R(2) MHz	120/133R(2) MHz
10	14	133/150R(2) MHz	133/150R(2) MHz
11	18	133/150R(2) MHz	133/150R(2) MHz

-40 ~ +125C：

DC bit	Numbers of Dummy Cycles(1)	Quad I/O Fast Read (EBH)	Fast Read Quad I/O with 4-Byte Address (ECH)
00	6	96 MHz	96 MHz
01	10	120/133R(2) MHz	120/133R(2) MHz
10	14	120/133R(2) MHz	120/133R(2) MHz
11	18	120/133R(2) MHz	120/133R(2) MHz

Notes:
1. The number of dummy includes M7-0.
2. "R" mean VCC range= 3.0V-3.6V.

(DTR Mode)

-40 ~ +85C：

DC bit	Numbers of Dummy Cycles(1)	DTR Fast Read Quad I/O(EDH)	DTR Quad I/O Fast Read with 4- Byte Address (EEh)
00	6	72/84R(2) MHz	72/84R(2) MHz
01	10	100 MHz	100 MHz
10	14	100 MHz	100 MHz
11	18	100 MHz	100 MHz

-40 ~ +105C：

DC bit	Numbers of Dummy Cycles(1)	DTR Fast Read Quad I/O(EDH)	DTR Quad I/O Fast Read with 4- Byte Address (EEh)
00	6	72/84R(2) MHz	72/84R(2) MHz
01	10	100 MHz	100 MHz
10	14	100 MHz	100 MHz
11	18	100 MHz	100 MHz

-40 ~ +125C：

DC bit	Numbers of Dummy Cycles(1)	DTR Fast Read Quad I/O(EDH)	DTR Quad I/O Fast Read with 4- Byte Address (EEh)
00	6	72/84R(2) MHz	72/84R(2) MHz
01	10	100 MHz	100 MHz
10	14	100 MHz	100 MHz
11	18	100 MHz	100 MHz

Notes:
1. The number of dummy includes M7-0.
2. "R" mean VCC range= 3.0V-3.6V.

5.6.2.14 DRV1/DRV0 bits

The Output Driver Strength (DRV1&DRV0) bits are used to determine the output driver strength for the Read instruction.

Table 6. The Output Driver Strength

DRV1,DRV0	Driver Strength
00	100%(default)
01	75%
10	50%
11	25%

5.7 Array Memory Protection

5.7.1 Block Protect Table (WPS=0)

Table 7. BY25FQ256 Block Memory Protection (WPS=0, CMP=0)

Status Register Content					Memory Content			
BP4	BP3	BP2	BP1	BP0	Blocks	Addresses	Density	Portion
X	0	0	0	0	NONE	NONE	NONE	NONE
0	0	0	0	1	511	01FF0000h -01FFFFFFh	64KB	Upper 1/512
0	0	0	1	0	510 to 511	01FE0000h -01FFFFFFh	128KB	Upper 1/256
0	0	0	1	1	508 to 511	01FC0000h -01FFFFFFh	256KB	Upper 1/128
0	0	1	0	0	504 to 511	01F80000h - 01FFFFFFh	512KB	Upper 1/64
0	0	1	0	1	496 to 511	01F00000h - 01FFFFFFh	1MB	Upper 1/32
0	0	1	1	0	480 to 511	01E00000h -01FFFFFFh	2MB	Upper 1/16
0	0	1	1	1	448 to 511	01C00000h -01FFFFFFh	4MB	Upper 1/8
0	1	0	0	0	384 to 511	01800000h - 01FFFFFFh	8MB	Upper 1/4
0	1	0	0	1	256 to 511	01000000h - 01FFFFFFh	16MB	Upper 1/2
1	0	0	0	1	0	00000000h - 0000FFFFh	64KB	Lower 1/512
1	0	0	1	0	0 to 1	00000000h - 0001FFFFh	128KB	Lower 1/256
1	0	0	1	1	0 to 3	00000000h - 0003FFFFh	256KB	Lower 1/128
1	0	1	0	0	0 to 7	00000000h - 0007FFFFh	512KB	Lower 1/64
1	0	1	0	1	0 to 15	00000000h - 000FFFFFh	1MB	Lower 1/32
1	0	1	1	0	0 to 31	00000000h - 001FFFFFh	2MB	Lower 1/16
1	0	1	1	1	0 to 63	00000000h - 003FFFFFh	4MB	Lower 1/8
1	1	0	0	0	0 to 127	00000000h - 007FFFFFh	8MB	Lower 1/4
1	1	0	0	1	0 to 255	00000000h - 00FFFFFFh	16MB	Lower 1/2
X	1	1	0	X	0 to 511	00000000h - 01FFFFFFh	32MB	ALL
X	1	X	1	X	0 to 511	00000000h - 01FFFFFFh	32MB	ALL

Table 8. BY25FQ256 Block Memory Protection (WPS=0, CMP=1)

Status Register Content					Memory Content			
BP4	BP3	BP2	BP1	BP0	Blocks	Addresses	Density	Portion
X	0	0	0	0	ALL	00000000h - 01FFFFFFh	ALL	ALL
0	0	0	0	1	0 to 510	00000000h - 01FEFFFFh	32,704KB	Lower 511/512
0	0	0	1	0	0 to 509	00000000h - 01FDFFFFh	32,640KB	Lower 255/256
0	0	0	1	1	0 to 507	00000000h - 01FBFFFFh	32,512KB	Lower 127/128
0	0	1	0	0	0 to 503	00000000h - 01F7FFFFh	32,256KB	Lower 63/64
0	0	1	0	1	0 to 495	00000000h - 01EFFFFFh	31MB	Lower 31/32
0	0	1	1	0	0 to 479	00000000h - 01DFFFFFh	30MB	Lower 15/16
0	0	1	1	1	0 to 447	00000000h - 01BFFFFFh	28MB	Lower 7/8
0	1	0	0	0	0 to 383	00000000h - 017FFFFFh	24MB	Lower 3/4
0	1	0	0	1	0 to 255	00000000h - 00FFFFFFh	16MB	Lower 1/2
1	0	0	0	1	1 to 511	00010000h - 01FFFFFFh	32,704KB	Upper 511/512
1	0	0	1	0	2 to 511	00020000h - 01FFFFFFh	32,640KB	Upper 255/256
1	0	0	1	1	4 to 511	00040000h - 01FFFFFFh	32,512KB	Upper 127/128
1	0	1	0	0	8 to 511	00080000h - 01FFFFFFh	32,256KB	Upper 63/64
1	0	1	0	1	16 to 511	00100000h - 01FFFFFFh	31MB	Upper 31/32
1	0	1	1	0	32 to 511	00200000h - 01FFFFFFh	30MB	Upper 15/16
1	0	1	1	1	64 to 511	00400000h - 01FFFFFFh	28MB	Upper 7/8
1	1	0	0	0	128 to 511	00800000h - 01FFFFFFh	24MB	Upper 3/4
1	1	0	0	1	256 to 511	01000000h - 01FFFFFFh	16MB	Upper 1/2
X	1	1	0	X	NONE	NONE	NONE	NONE
X	1	X	1	X	NONE	NONE	NONE	NONE

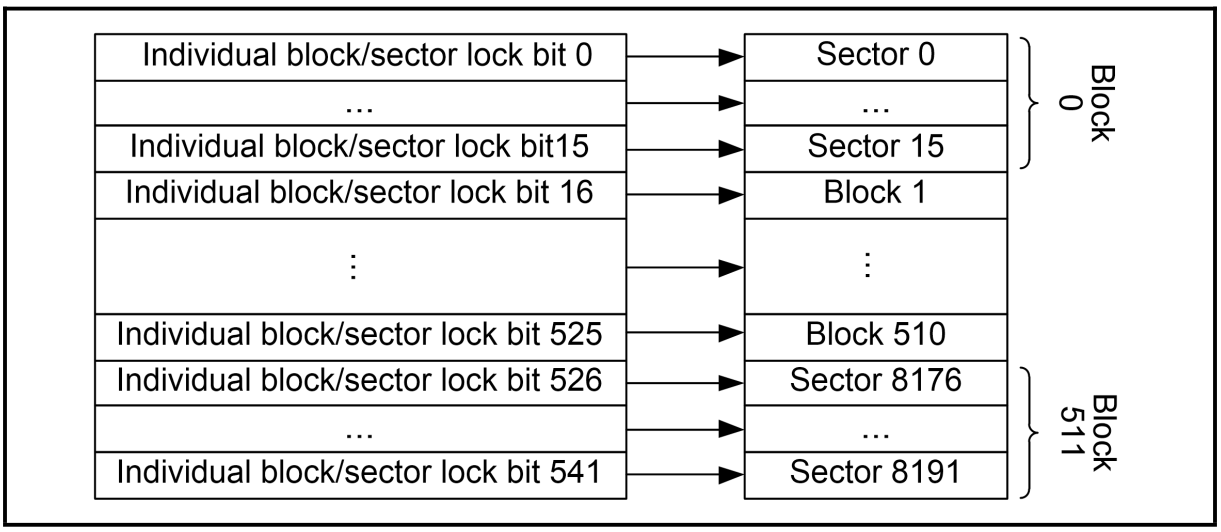
5.7.2 Individual Block Memory Protection (WPS=1)

Individual Block Memory Protection can protect individual 4KB sectors in the bottom and top 64KB of memory and protect individual 64KB blocks in the rest of memory.

There is one volatile individual block/sector lock bit assigned to each 4KB sector at the bottom and top 64KB of memory and to each 64KB block in the rest of memory. A sector or block is write-protected from programming or erasing when its associated individual block/sector lock bit is set to “1”.

Please note that if WPS=0, all Individual Block Memory Protection instructions (***7.5.1-0***) are not available.

Figure 8. Individual block/sector lock bit for Block/Sector Array



Notes:
1. Individual Block/Sector protection is only valid when WPS=1.
2. All individual block/sector lock bits are set to 1 by default after power up, all memory array is protected.

5.7.2.1 Individual Block/Sector Lock bit

The Individual Block/Sector Lock bits are volatile bits for quickly and easily enabling or disabling write-protection to sectors and blocks. A Individual Block/Sector Lock bit is assigned to each 4KB sector in the bottom and top 64KB of memory and to each 64KB block in the rest of the memory.

When a Individual Block/Sector Lock bit is “1”, the associated sector or block will be write-protected, preventing any program or erase operation on the sector or block. All Individual Block/Sector Lock bits default to “1” after power-on or reset.

Individual Block/Sector Lock bits can be individually set to “1” or “0” by the Individual Block/Sector Lock/ Individual Block/Sector Unlock instruction. The Individual Block/Sector Lock bits can also be globally cleared to “0” with the Global Block/Sector Unlock instruction or globally set to “1” with the Global Block/Sector Lock instruction. A Write Enable instruction must be executed to set the WEL bit before sending the Individual Block/Sector Lock, Individual Block/Sector Unlock, Global Block/Sector Lock, or Global Block/Sector Unlock instruction.

The Read Block/Sector Lock instruction reads the status of the Individual Block/Sector Lock bit of a sector or block. The Read Block/Sector Lock instruction returns 00h if the Individual Block/Sector Lock bit is “0”, indicating write-protection is disabled. The Read Block/Sector Lock Status instruction returns FFh if the Individual Block/Sector Lock bit is “1”, indicating write-protection is enabled.

Table 9. Dynamic Protection Bit

Description	Bit Status	Default	Type
Individual Block/Sector Lock bit	0 = Unprotect Sector / Block 1 = Protect Sector / Block	1	Volatile

5.8 Extended Address Register

In addition to the Status Registers, the BY25FQ256 also provides a volatile Extended Address Register that allows the 256M area of the device to be used normally in 3-Byte Address Mode. The value of the Extended Address Register and the 24-bit address input in the 3-Byte Address Mode together form the complete start address of the instruction operation. That is, when A24 = 0, the starting address of the instruction operation selects the lower 128Mb memory array (00000000h-00FFFFFFh). When A24 = 1, the start address of the instruction operation will select the high 128Mb memory array (01000000h-01FFFFFFh).

Please note that:

1. In 3-Byte Address Mode, When A24 = 0/1, the starting address of the instruction operation selects the lower/ high 128Mb memory array. However, as the instruction operation address continues to be carried, the address of the instruction operation can enter the high/lower 128Mb memory array. At this time, the value of the Extended Address Register does not change with the carry of the address, that is, the value of Extended Address Register can only be modified by the Write Extended Address Register instruction.
2. In 4-Byte Address Mode, Extended Address Register is not available. The value of Extended Address Register has no effect on the instruction operation. The device will require 4-Byte address input for all address related instructions, and the Extended Address Register setting will be ignored. The Read Extended Address Register and Write Extended Address Register instructions are not available in the 4-Byte Address Mode. At the same time, during the instruction operation, the same as in the 3-Byte Address Mode, the carry of the address does not have any effect on the Extended Address Register.

Table 10. Extended Address Register

EA7	EA6	EA5	EA4	EA3	EA2	EA1	EA0
A31(1)	A30(1)	A29(1)	A28(1)	A27(1)	A26(1)	A25(1)	A24(2)

Notes:
1. Reserved for higher densities: 512Mb ~ 32Gb.
2. Address Bit #24:A24=0: Select lower 128Mb; A24=1: Select upper 128Mb.

6. Device Identification

Three legacy Instructions are supported to access device identification that can indicate the manufacturer, device type, and capacity (density). The returned data bytes provide the information as shown in the below table.

Table 11. BY25FQ256 ID Definition table (SPI and QPI Mode have the same ID Definition)

Operation Code	M7-M0(SPI)	ID15-ID8(SPI)	ID7-ID0(SPI)
9FH	68	40	19
90H/92H/94H	68		18
ABH			18

7. Instructions Description

All instructions, addresses and data are shifted in and out of the device, beginning with the most significant bit on the first rising edge of SCLK after /CS is driven low. Then, the one byte instruction code must be shifted in to the device, most significant bit first on SI, each bit being latched on the rising edges of SCLK.

See ***Table 12***, every instruction sequence starts with a one-byte instruction code. Depending on the instruction, this might be followed by address bytes, or by data bytes, or by both or none. /CS must be driven high after the last bit of the instruction sequence has been shifted in. For the instruction of Read, Fast Read, Read Status Register or Release from Deep Power Down, and Read Device ID, the shifted-in instruction sequence is followed by a data out sequence. /CS can be driven high after any bit of the data-out sequence is being shifted out.

For the instruction of Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register, Write Enable, Write Disable or Deep Power-Down instruction, etc. /CS must be driven high exactly at a byte boundary, otherwise the instruction is rejected, and is not executed. That is /CS must drive high when the number of clock pulses after /CS being driven low is an exact multiple of eight. For Page Program, if at any time the input byte is not a full byte, nothing will happen and WEL will not be reset.

Table 12. Instruction Set Table

Instruction Set Table-Standard/Dual/Quad SPI Instructions, 3-Byte & 4-Byte Address Mode(1)

Data Input Output	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
Clock Number	**（0-7）**	**（8-15）**	**（16-23）**	**（24-31）**	**（32-39）**	**（40-47）**	**（48-55）**
Write Enable	06h						
Volatile SR Write Enable	50h						
Write Disable	04h						
Read Status Register-1	05h	(S7-S0)(2)					
Write Status Register(4)	01h	(S7-S0)(4)	(S15-S8)				
Read Status Register-2	35h	(S15-S8)(2)					
Write Status Register-2	31h	(S15-S8)					
Read Status Register-3	15h	(S23-S16)(2)					
Write Status Register-3	11h	(S23-S16)					
Chip Erase	C7h/60h						
Program/Erase Suspend	75h						
Program/Erase Resume	7Ah						
Deep Power-down	B9h						
Release Power-down / ID	ABh	Dummy	Dummy	Dummy	(ID7-ID0)(2)		
Release Power-down	ABH						
Manufacturer/Device ID	90h	Dummy	Dummy	00/01h	(MF7-MF0)/ (ID7-ID0)	(ID7-ID0))/ (MF7-MF0)	
Read JEDEC ID	9Fh	(MF7-MF0)	(ID15-ID8)	(ID7-ID0)(9)			
Read Serial Flash Discoverable Parameter	5Ah	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)	
Enter QPI Mode	38h						
Enable Reset	66h						
Reset Device	99h						
Read Data with 4-Byte Address	13h	A31-A24	A23-A16	A15-A8	A7-A0	(D7-D0)	
Fast Read with 4-Byte Address	0Ch	A31-A24	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)
Fast Read Dual Output with 4-Byte Address	3Ch	A31-A24	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0, …)(7)
Fast Read Quad Outpu with 4-Byte Address	6Ch	A31-A24	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0, …)(9)
Data Input Output	**Byte 1**	**Byte 2**	**Byte 3**	**Byte 4**	**Byte 5**	**Byte 6**	**Byte 7**
Clock Number	**（0-7）**	**（8-11）**	**（12-15）**	**（16-19）**	**（20-23）**	**（24-27）**	**（28-31）**
Fast Read Dual I/O with 4-Byte Address	BCh	A31-A24	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)

Data Input Output	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7	Byte 8	Byte 9
Clock Number	**（0-7）**	**（8-9）**	**（10-11）**	**（12-13）**	**（14-15）**	**（16-17）**	**（18-19）**	**（20-21）**	**（22-23）**
Fast Read Quad I/O with 4-Byte Address	ECh	A31-A24	A23-A16	A15-A8	A7-A0	M7-M0	Dummy	Dummy	(D7-D0)

Data Input Output	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
Clock Number	**（0-7）**	**（8-9）**	**（10-11）**	**（12-13）**	**（14-15）**	**（16-17）**	**（18-19）**
Page Program with 4-Byte Address	12h	A31-A24	A23-A16	A15-A8	A7-A0	(D7-D0)	(D7-D0)(3)
Quad Page Program with 4-Byte Address	34h	A31-A24	A23-A16	A15-A8	A7-A0	(D7-D0)	
Sector Erase (4KB) with 4-Byte Address	21h	A31-A24	A23-A16	A15-A8	A7-A0		
Block Erase(32K) with 4-Byte Address	5Ch	A31-A24	A23-A16	A15-A8	A7-A0		

Block Erase(64K) with 4-Byte Address	DCh	A31-A24	A23-A16	A15-A8	A7-A0		
Global Block/Sector Lock	7Eh						
Global Block/Sector Unlock	98h						

Instruction Set Table-Standard/Dual/Quad SPI Instructions, 3-Byte Address Mode (1)

Data Input Output	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6
Clock Number	**(0-7)**	**(8-15)**	**(16-23)**	**(24-31)**	**(32-39)**	**(40-55)**
Read Unique ID Number	4Bh	Dummy	Dummy	Dummy	Dummy	(ID127-ID0)
Clock Number	**(0-7)**	**(8-15)**	**(16-23)**	**(24-31)**	**(32-39)**	**(40-47)**
Page Program	02h	A23-A16	A15-A8	A7-A0	(D7-D0)	(D7-D0)(3)
Quad Page Program	32h	A23-A16	A15-A8	A7-A0	(D7-D0, …)(9)	(D7-D0, …)(3)
Sector Erase (4KB)	20h	A23-A16	A15-A8	A7-A0		
Block Erase (32KB)	52h	A23-A16	A15-A8	A7-A0		
Block Erase (64KB)	D8h	A23-A16	A15-A8	A7-A0		
Normal Read Data	03h	A23-A16	A15-A8	A7-A0	(D7-D0)	(Next Byte)
Fast Read	0Bh	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)
Dual Output Fast read	3Bh	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)(7)
Quad Output Fast read	6Bh	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)(9)
Erase Security Registers(5)	44h	A23-A16(8)	A15-A8(8)	A7-A0(8)		
Program Security Registers(5)	42h	A23-A16(8)	A15-A8(8)	A7-A0(8)	D7-D0	Next Byte
Read Security Registers(5)	48h	A23-A16(8)	A15-A8(8)	A7-A0(8)	Dummy	D7-D0

Data Input Output	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
Clock Number	**(0-7)**	**(8-11)**	**(12-15)**	**(16-19)**	**(20-23)**	**(24-27)**	**(28-31)**
Dual I/O Fast read	BBh	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)	
Mftr./Device ID Dual I/O	92h	A23-A16	A15-A8	A7-A0	Dummy	(MF7-MF0)	(ID7-ID0)

Data Input Output	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7	Byte 8	Byte 9
Clock Number	**(0-7)**	**(8-9)**	**(10-11)**	**(12-13)**	**(14-15)**	**(16-17)**	**(18-19)**	**(20-21)**	**(22-23)**
Set Burst With Wrap	77h	Dummy	Dummy	Dummy	W6-W4				
Quad I/O Fast read	EBh	A23-A16	A15-A8	A7-A0	M7-M0	Dummy	Dummy	(D7-D0)	(D7-D0)
Mftr./Device ID Quad I/O	94h	A23-A16	A15-A8	A7-A0	M7-M0	Dummy	Dummy	(MF7-MF0)	(ID7-ID0)
Read Block/Sector Lock	3Dh	A23-A16	A15-A8	A7-A0	(D7-D0)				
Individual Block/Sector Lock	36h	A23-A16	A15-A8	A7-A0					
Individual Block/Sector Unlock	39h	A23-A16	A15-A8	A7-A0					
Enter 4-Byte Address Mode	B7h								
Read Extended Addr. Register	C8h	(EA7-EA0)(2)							
Write Extended Addr. Register	C5h	(EA7-EA0)							

Instruction Set Table-Standard/Dual/Quad SPI Instructions, 4-Byte Address Mode (1)

Data Input Output	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
Clock Number	**(0-7)**	**(8-15)**	**(16-23)**	**(24-31)**	**(32-39)**	**(40-47)**	**(48-63)**
Read Unique ID Number	4Bh	Dummy	Dummy	Dummy	Dummy	Dummy	(ID127-ID0)
Clock Number	**(0-7)**	**(8-15)**	**(16-23)**	**(24-31)**	**(32-39)**	**(40-47)**	**(48-55)**
Page Program	02h	A31-A24	A23-A16	A15-A8	A7-A0	(D7-D0)	(D7-D0)(3)
Quad Page Program	32h	A31-A24	A23-A16	A15-A8	A7-A0	(D7-D0, …)(9)	(D7-D0, …)(3)
Sector Erase (4KB)	20h	A31-A24	A23-A16	A15-A8	A7-A0		
Block Erase (32KB)	52h	A31-A24	A23-A16	A15-A8	A7-A0		
Block Erase (64KB)	D8h	A31-A24	A23-A16	A15-A8	A7-A0		
Normal Read Data	03h	A31-A24	A23-A16	A15-A8	A7-A0	(D7-D0)	(Next Byte)
Fast Read	0Bh	A31-A24	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)
Dual Output Fast read	3Bh	A31-A24	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)(7)
Quad Output Fast read	6Bh	A31-A24	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)(9)
Erase Security Registers(5)	44h	A31-A24	A23-A16(8)	A15-A8(8)	A7-A0(8)		
Program Security Registers(5)	42h	A31-A24	A23-A16(8)	A15-A8(8)	A7-A0(8)	D7-D0	Next Byte
Read Security Registers(5)	48h	A31-A24	A23-A16(8)	A15-A8(8)	A7-A0(8)	Dummy	D7-D0

Data Input Output	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7	Byte 8
Clock Number	**(0-7)**	**(8-11)**	**(12-15)**	**(16-19)**	**(20-23)**	**(24-27)**	**(28-31)**	**(22-35)**
Dual I/O Fast read	BBh	A31-A24	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)	(D7-D0)
Mftr./Device ID Dual I/O	92h	A31-A24	A23-A16	A15-A8	A7-A0	Dummy	(MF7-MF0)	(ID7-ID0)

Data Input Output	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7	Byte 8	Byte 9	Byte 10
Clock Number	**(0-7)**	**(8-9)**	**(10-11)**	**(12-13)**	**(14-15)**	**(16-17)**	**(18-19)**	**(20-21)**	**(22-23)**	**(24-25)**
Set Burst With Wrap	77h	Dummy	Dummy	Dummy	Dummy	W6-W4				
Quad I/O Fast read	EBh	A31-A24	A23-A16	A15-A8	A7-A0	M7-M0	Dummy	Dummy	(D7-D0)	(D7-D0)
Word Read Quad I/O(12)	E7h	A31-A24	A23-A16	A15-A8	A7-A0	M7-M0	Dummy	(D7-D0)	(D7-D0)	(D7-D0)
Mftr./Device ID Quad I/O	94h	A31-A24	A23-A16	A15-A8	A7-A0	M7-M0	Dummy	Dummy	(MF7-MF0)	(D7-D0)
Read Block/Sector Lock	3Dh	A31-A24	A23-A16	A15-A8	A7-A0	(D7-D0)				
Individual Block/Sector Lock	36h	A31-A24	A23-A16	A15-A8	A7-A0					
Individual Block/Sector Unlock	39h	A31-A24	A23-A16	A15-A8	A7-A0					
Exit 4-Byte Address Mode	E9h									

Instruction Set Table-QPI Instructions, 3-Byte & 4-Byte Address Mode (14)

Data Input Output	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7	Byte 8
Clock Number	**(0-1)**	**(2-3)**	**(4- 5)**	**(6- 7)**	**(8-9)**	**(10-11)**	**(12-13)**	**(14-15)**
Write Enable	06h							
Volatile SR Write Enable	50h							
Write Disable	04h							
Read Status Register-1	05h	(S7-S0)(2)						
Write Status Register(4)	01h	(S7-S0)(4)	(S15-S8)					
Read Status Register-2	35h	(S15-S8)(2)						
Write Status Register-2	31h	(S15-S8)						
Read Status Register-3	15h	(S23-S16)(2)						
Write Status Register-3	11h	(S23-S16)						
Chip Erase	C7h/60h							
Erase / Program Suspend	75h							
Erase / Program Resume	7Ah							
Power-down	B9h							
Set Read Parameters	C0h	P7-P0						
Release Powerdown / ID	ABh	Dummy	Dummy	Dummy	(ID7-ID0)(2)			
Manufacturer/Device ID	90h	Dummy	Dummy	00h	(MF7-MF0)	(ID7-ID0)		
JEDEC ID	9Fh	(MF7-MF0)	(ID15-ID8)	(ID7-ID0)				
Exit QPI Mode	FFh							
Enable Reset	66h							
Reset Device	99h							
Fast Read Quad I/O with 4-Byte Address	ECh	A31-A24	A23-A16	A15-A8	A7-A0	M7-M0(15)	Dummy	(D7-D0)
Read Serial Flash Discoverable Parameter	5Ah	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)		
Page Program with 4-Byte Address	12h	A31-A24	A23-A16	A15-A8	A7-A0	(D7-D0)	(D7-D0)(3)	
Sector Erase (4KB) with 4-Byte Address	21h	A31-A24	A23-A16	A15-A8	A7-A0			
Block Erase(32K) with 4-Byte Address	5Ch	A31-A24	A23-A16	A15-A8	A7-A0			
Block Erase(64K) with 4-Byte Address	DCh	A31-A24	A23-A16	A15-A8	A7-A0			

Instruction Set Table-QPI Instructions, 3-Byte Address Mode (14)

Data Input Output	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
Clock Number	**(0-1)**	**(2-3)**	**(4-5)**	**(6-7)**	**(8-9)**	**(10-11)**	**(12-13)**
Page Program	02h	A23-A16	A15-A8	A7-A0	D7-D0(9)	D7-D0(3)	
Sector Erase (4KB)	20h	A23-A16	A15-A8	A7-A0			
Block Erase (32KB)	52h	A23-A16	A15-A8	A7-A0			
Block Erase (64KB)	D8h	A23-A16	A15-A8	A7-A0			
Fast Read	0Bh	A23-A16	A15-A8	A7-A0	Dummy(15)	(D7-D0)	
Burst Read with Wrap(16)	0Ch	A23-A16	A15-A8	A7-A0	Dummy(15)	(D7-D0)	
Fast Read Quad I/O	EBh	A23-A16	A15-A8	A7-A0	M7-M0(15)	Dummy	(D7-D0)
Read Unique ID Number	4Bh	Dummy	Dummy	Dummy	Dummys*	(ID127-ID0)	
Read Security Registers(5)	48h	A23-A16(8)	A15-A8(8)	A7-A0(8)	Dummy	D7-D0	
Erase Security Registers(5)	44h	A23-A16(8)	A15-A8(8)	A7-A0(8)			
Program Security Registers(5)	42h	A23-A16(8)	A15-A8(8)	A7-A0(8)	D7-D0	Next Byte	
Read Block/Sector Lock	3Dh	A23-A16	A15-A8	A7-A0	(D7-D0)		
Individual Block/Sector Lock	36h	A23-A16	A15-A8	A7-A0			
Individual Block/Sector Unlock	39h	A23-A16	A15-A8	A7-A0			
Enter 4-Byte Address Mode	B7h						
Read Extended Addr. Register	C8h	(EA7-EA0)(2)					
Write Extended Addr. Register	C5h	(EA7-EA0)					

Instruction Set Table-QPI Instructions, 4-Byte Address Mode (14)

Data Input Output	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7	Byte 8
Clock Number	**(0-1)**	**(2-3)**	**(4-5)**	**(6-7)**	**(8-9)**	**(10-11)**	**(12-13)**	**(13-14)**
Page Program	02h	A31-A24	A23-A16	A15-A8	A7-A0	D7-D0(9)	D7-D0(3)	
Sector Erase (4KB)	20h	A31-A24	A23-A16	A15-A8	A7-A0			
Block Erase (32KB)	52h	A31-A24	A23-A16	A15-A8	A7-A0			
Block Erase (64KB)	D8h	A31-A24	A23-A16	A15-A8	A7-A0			
Fast Read	0Bh	A31-A24	A23-A16	A15-A8	A7-A0	Dummy(15)	(D7-D0)	
Burst Read with Wrap(16)	0Ch	A31-A24	A23-A16	A15-A8	A7-A0	Dummy(15)	(D7-D0)	
Fast Read Quad I/O	EBh	A31-A24	A23-A16	A15-A8	A7-A0	M7-M0(15)	Dummy	(D7-D0)
Read Unique ID Number	4Bh	Dummy	Dummy	Dummy	Dummy	Dummys*	(ID127-ID0)	
Read Security Registers(5)	48h	A31-A24	A23-A16(8)	A15-A8(8)	A7-A0(8)	Dummy	D7-D0	
Erase Security Registers(5)	44h	A31-A24	A23-A16(8)	A15-A8(8)	A7-A0(8)			
Program Security Registers(5)	42h	A31-A24	A23-A16(8)	A15-A8(8)	A7-A0(8)	D7-D0	Next Byte	
Read Block/Sector Lock	3Dh	A31-A24	A23-A16	A15-A8	A7-A0	(D7-D0)		
Individual Block/Sector Lock	36h	A31-A24	A23-A16	A15-A8	A7-A0			
Individual Block/Sector Unlock	39h	A31-A24	A23-A16	A15-A8	A7-A0			
Exit 4-Byte Address Mode	E9h							

Instruction Set Table-DTR with SPI Instructions, 3-Byte & 4-Byte Address Mode (14)

Data Input Output	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
Clock Number(1-1-1)	**8**	**4**	**4**	**4**	**6**	**4**	**4**
DTR Quad I/O Fast Read with 4- Byte Address	EEh	A31-A24	A23-A16	A15-A8	A7-A0	M7-M0	(D7-D0)

Instruction Set Table-DTR with QPI Instructions, 3-Byte & 4-Byte Address Mode (14)

Data Input Output	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
Clock Number(1-1-1)	**8**	**4**	**4**	**4**	**6**	**4**	**4**
DTR Quad I/O Fast Read with 4- Byte Address	EEh	A31-A24	A23-A16	A15-A8	A7-A0	M7-M0	(D7-D0)

Instruction Set Table-DTR with SPI Instructions, 3-Byte Address Mode (14)

Data Input Output	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
Clock Number(1-4-4)	**8**	**1**	**1**	**1**	**1**	**7**	**1**
DTR Fast Read Quad I/O	EDh	A23-A16	A15-A8	A7-A0	M7-M0	Dummy	(D7-D0)

Instruction Set Table-DTR with SPI Instructions, 4-Byte Address Mode (14)

Data Input Output	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
Clock Number(1-4-4)	**8**	**1**	**1**	**1**	**1**	**7**	**1**
DTR Fast Read Quad I/O	EDh	A31-A16	A15-A0	M7-M0	Dummy	(D7-D0)	

Instruction Set Table-DTR with QPI Instructions, 3-Byte Address Mode (14)

Data Input Output	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
Clock Number(4-4-4)	**2**	**1**	**1**	**1**	**8**	**1**	**1**
DTR Read with Wrap(13)	0Eh	A23-A16	A15-A8	A7-A0	Dummy	D7-D0	
Clock Number(4-4-4)	**2**	**1**	**1**	**1**	**1**	**7**	**1**
DTR Fast Read Quad I/O	EDh	A23-A16	A15-A8	A7-A0	M7-M0	Dummy	(D7-D0)

Instruction Set Table-DTR with QPI Instructions, 4-Byte Address Mode (14)

Data Input Output	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7	Byte 8
Clock Number(4-4-4)	**2**	**1**	**1**	**1**	**61**	**8**	**1**	**1**
DTR Read with Wrap(13)	0Eh	A31-A24	A23-A16	A15-A8	A7-A0	Dummy	D7-D0	
Clock Number(4-4-4)	**2**	**1**	**1**	**1**	**1**	**1**	**7**	**1**
DTR Fast Read Quad I/O	EDh	A31-A24	A23-A16	A15-A8	A7-A0	M7-M0	Dummy	(D7-D0)

Notes:

1. Data bytes are shifted with Most Significant Bit first. Byte fields with data in parenthesis "( )" indicate data output from the device on either 1, 2 or 4 IO pins.

2. The Status Register contents and Device ID will repeat continuously until /CS terminates the instruction.

3. At least one byte of data input is required for Page Program, Quad Page Program and Program Security Registers, up to 256 bytes of data input. If more than 256 bytes of data are sent to the device, the addressing will wrap to the beginning of the page and overwrite previously sent data.

4. When the Write Status Register instruction 01h is followed by 1 byte data, the data will be written to Status Register-1. When the Write Status Register instruction 01h is followed by 2 bytes of data, the first byte data will be written to Status Register-2, see ***Write Status Register (01H or 31H or 11H)***.

5. Security Register Address:
Security Register 1: A23-16=00h; A15-12=0001; A11-9=000; A8-0=byte address
Security Register 2: A23-16=00h; A15-12=0010; A11-9=000; A8-0=byte address
Security Register 3: A23-16=00h; A15-12=0011; A11-9=000; A8-0=byte address

6. Dual SPI address input format:
IO0 = A22, A20, A18, A16, A14, A12, A10, A8 A6, A4, A2, A0, M6, M4, M2, M0
IO1 = A23, A21, A19, A17, A15, A13, A11, A9 A7, A5, A3, A1, M7, M5, M3, M1

7. Dual SPI data output format:
IO0 = (D6, D4, D2, D0)
IO1 = (D7, D5, D3, D1)

8. Quad SPI address input format:
IO0 = A20, A16, A12, A8, A4, A0, M4, M0
IO1 = A21, A17, A13, A9, A5, A1, M5, M1
IO2 = A22, A18, A14, A10, A6, A2, M6, M2
IO3 = A23, A19, A15, A11, A7, A3, M7, M3

Set Burst with Wrap input format:
IO0 = x, x, x, x, x, x, W4, x
IO1 = x, x, x, x, x, x, W5, x
IO2 = x, x, x, x, x, x, W6, x
IO3 = x, x, x, x, x, x, x, x

9. Quad SPI data input/output format:

IO0 = (D4, D0, …..)
IO1 = (D5, D1, …..)
IO2 = (D6, D2, …..)
IO3 = (D7, D3, …..)

10. Fast Read Quad I/O data output format:

IO0 = (x, x, x, x, D4, D0, D4, D0)

IO1 = (x, x, x, x, D5, D1, D5, D1)

IO2 = (x, x, x, x, D6, D2, D6, D2)

IO3 = (x, x, x, x, D7, D3, D7, D3)

11. Word Read Quad I/O data output format:

IO0 = (x, x, D4, D0, D4, D0, D4, D0)
IO1 = (x, x, D5, D1, D5, D1, D5, D1)
IO2 = (x, x, D6, D2, D6, D2, D6, D2)
IO3 = (x, x, D7, D3, D7, D3, D7, D3)

12. For Word Read Quad I/O, the lowest address bit must be 0. (A0 = 0)

13. For Octal Word Read Quad I/O, the lowest four address bits must be 0. (A3, A2, A1, A0 = 0)

14. QPI Instruction, Address, Data input/output format:

CLK # 0	1	2	3	4	5	6	7	8	9	10	11
IO0 = C4, C0,	A20, A16,		A12, A8,		A4, A0,		D4, D0,		D4, D0		
IO1 = C5, C1,	A21, A17,		A13, A9,		A5, A1,		D5, D1,		D5, D1		
IO2 = C6, C2,	A22, A18,		A14, A10,		A6, A2,		D6, D2,		D6, D2		
IO3 = C7, C3,	A23, A19,		A15, A11,		A7, A3,		D7, D3,		D7, D3		

15. The number of dummy clocks for QPI Fast Read, QPI Fast Read Quad I/O & QPI Burst Read with Wrap is controlled by read parameter P7 – P4.

16. The wrap around length for QPI Burst Read with Wrap is controlled by read parameter P3 – P0.

Table 13. Instructions that need to send the Write Enable/Write Enable for Volatile Status Register instruction

Mode	Instruction		Write
SPI/QPI	Write Status Register	01h/31h/11h	06H/50H
	Write Extended Address Register	C5h	06H
	Erase Security Registers	44h	06H
	Program Security Registers	42h	06H
	Page Program	02h	06H
	Page Program with 4-Byte Address	12h	06H
SPI	Quad Page Program	32h	06H
	Quad Input Page Program with 4-Byte Address	34h	06H
SPI/QPI	Sector Erase	20h	06H
	Sector Erase with 4-Byte Address	21h	06H
	32KB Block Erase	52h	06H
	32KB Block Erase with 4-Byte Address	5Ch	06H
	64KB Block Erase	D8h	06H
	64KB Block Erase with 4-Byte Address	DCh	06H
	Chip Erase	60h/C7h	06H
	Individual Block/Sector Lock	36h	06H
	Individual Block/Sector Unlock	39h	06H
	Global Block/Sector Lock	7Eh	06H
	Global Block/Sector Unlock	98h	06H

7.1 Configuration and Status Instructions

7.1.1 Write Enable (06H)

See ***Figure 9-Figure 10***，the Write Enable instruction is for setting the Write Enable Latch bit. The Write Enable Latch bit must be set prior to every Write Status Register, Program, Erase and some Individual Block Memory Protection instruction (see Table 13***)***. The Write Enable instruction sequence: /CS goes low sending the Write Enable instruction, /CS goes high.

Please note that the Write Enable instruction sent when the Write Enable for Volatile Status Register instruction is valid is not accepted. Therefore, when need to send the Write Enable instruction, but do not know if the Write Enable for Volatile Status Register instruction is valid, please send the Write Disable instruction first.

Figure 9. Write Enable Sequence Diagram (SPI Mode)

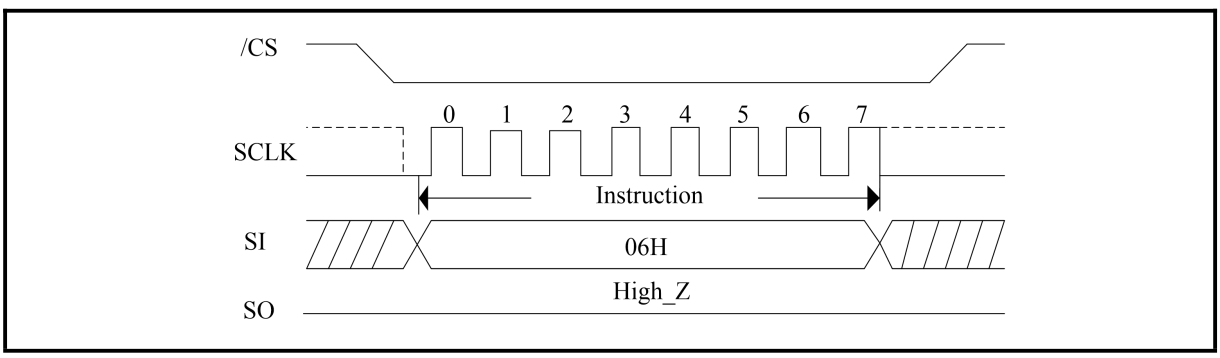
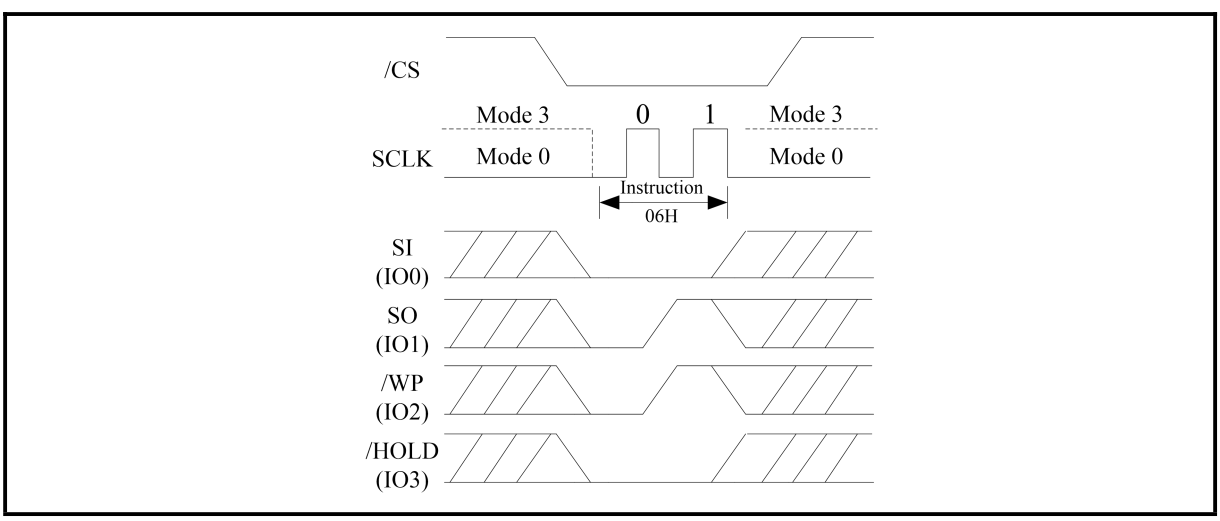


Figure 10. Write Enable Sequence Diagram (QPI Mode)



7.1.2 Write Enable for Volatile Status Register (50H)

See ***Figure 11-Figure 12***, the non-volatile Status Register bits can also be written to as volatile bits (HOLD/RES, DRV1, DRV0, DC1, DC0, CMP, QE, SRP1, SRP0, BP4, BP3, BP2, BP1, BP0). This gives more flexibility to change the system configuration and memory protection schemes quickly without waiting for the typical non-volatile bit write cycles or affecting the endurance of the Status Register non-volatile bits. Write Enable for Volatile Status Register instruction will not set the Write Enable Latch bit, it is only valid for the Write Status Registers instruction to change the volatile Status Register bit values (After the software/hardware reset or re-powered, the volatile Status Register bit values will be restored to the default value or the value input by the Write Enable instruction).

Please note that the Write Enable for Volatile Status Register instruction sent when the Write Enable instruction is valid is not accepted. Therefore, when need to send the Write Enable for Volatile Status Register instruction, please first determine whether the Write Enable instruction is not valid.

Figure 11. Write Enable for Volatile Status Register (SPI Mode)

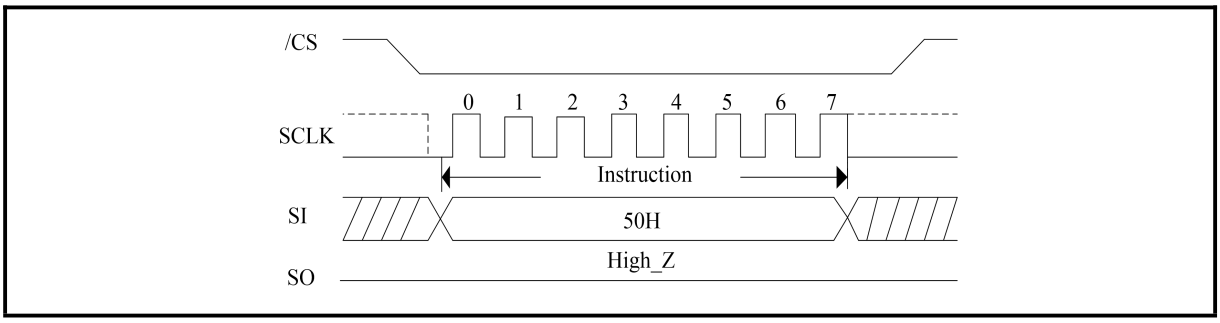
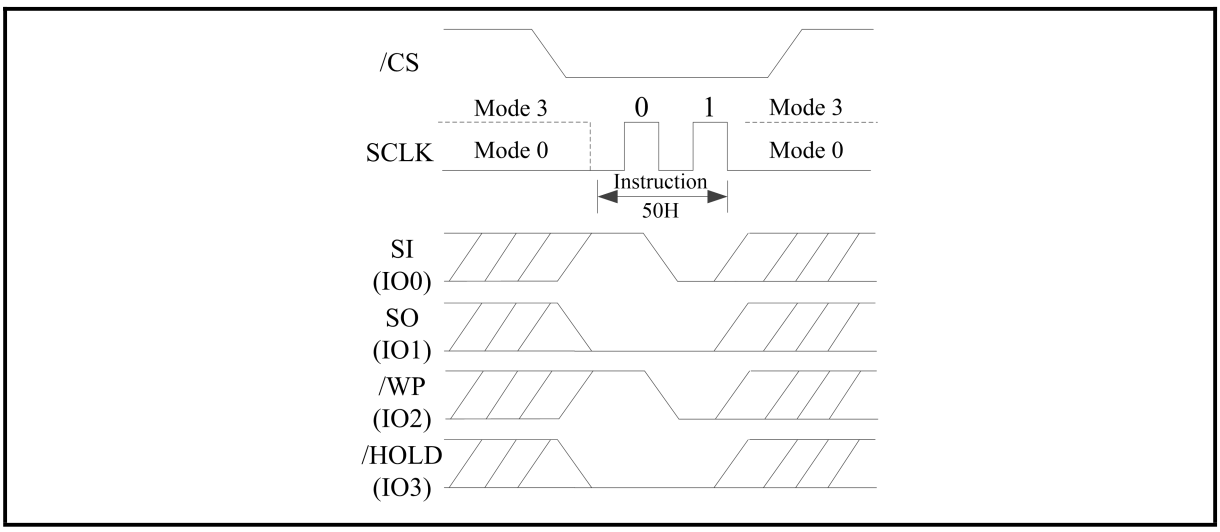


Figure 12. Write Enable for Volatile Status Register (QPI Mode)



7.1.3 Write Disable (04H)

See ***Figure 13-Figure 14***, the Write Disable instruction is for resetting the Write Enable Latch bit or invalidate the Write Enable for Volatile Status Register instruction. The Write Disable instruction sequence: /CS goes low -> sending the Write Disable instruction -> /CS goes high. The WEL bit is reset by following condition: Power-up and upon completion of the Write Status Register, Page Program, Sector Erase, Block Erase and Chip Erase, Program/Erase Security Registers and Reset instructions.

Figure 13. Write Disable Sequence Diagram (SPI Mode)

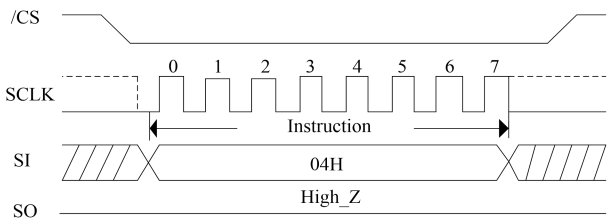
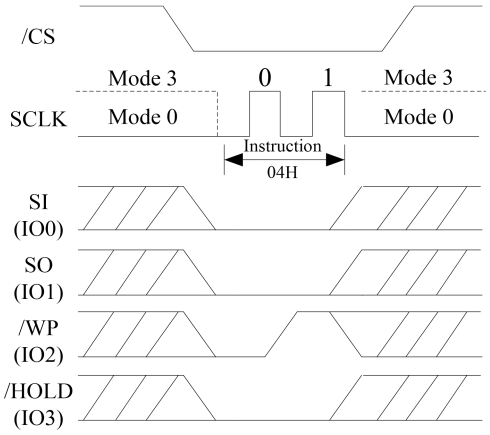


Figure 14. Write Disable Sequence Diagram (QPI Mode)



7.1.4 Read Status Register (05H or 35H or 15H)

See ***Figure 15-Figure 16***, the Read Status Register (RDSR) instruction is for reading the Status Register. The Status Register may be read at any time, even while a Program, Erase or Write Status Register cycle is in progress. When one of these cycles is in progress, it is recommended to check the Write in Progress (WIP) bit before sending a new instruction to the device. It is also possible to read the Status Register continuously. For instruction code “05H”, the SO will output Status Register bits S7~S0. The instruction code “35H”, the SO will output Status Register bits S15~S8, The instruction code “15H”, the SO will output Status Register bits S23~16.

Figure 15. Read Status Register Sequence Diagram (SPI Mode)

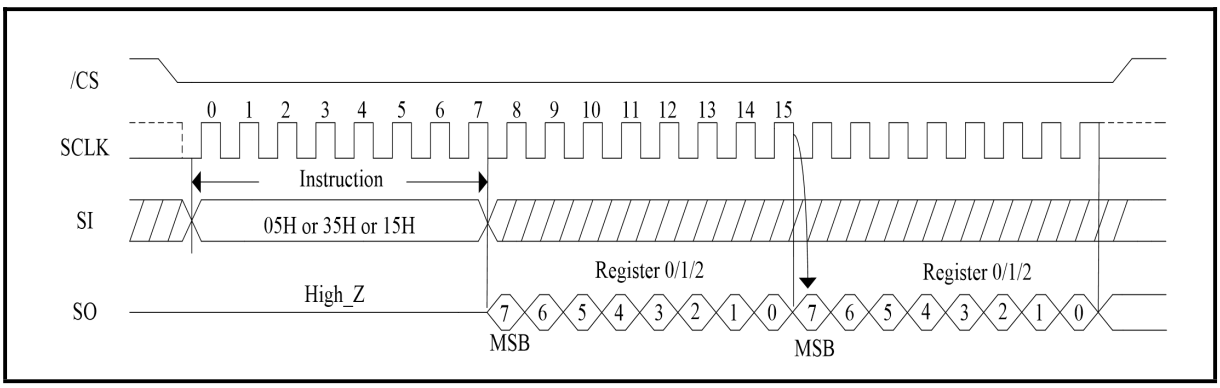
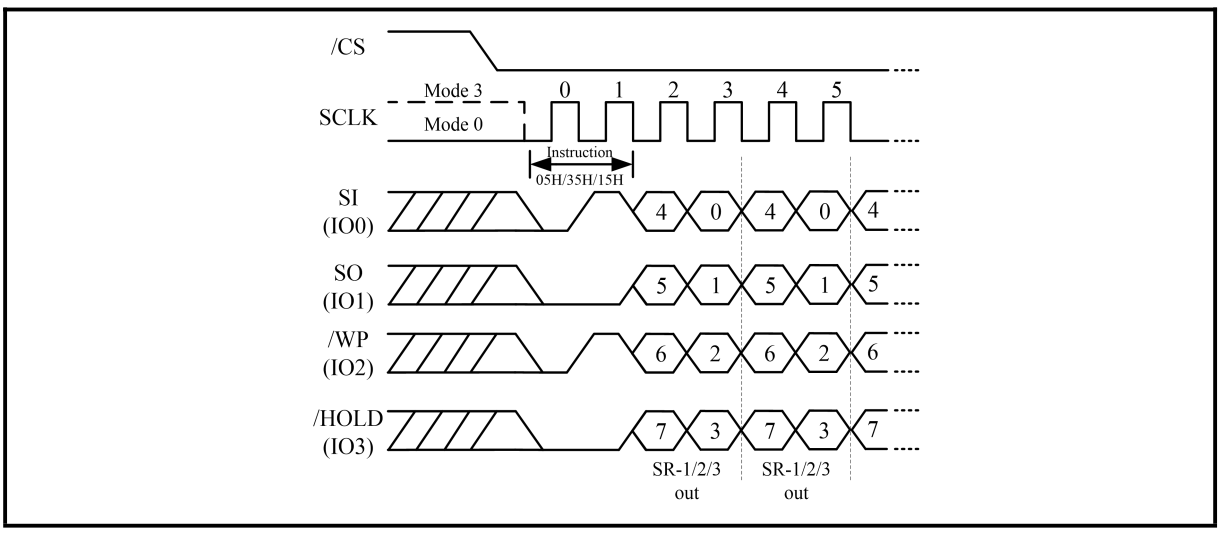


Figure 16. Read Status Register Sequence Diagram (QPI Mode)



7.1.5 Write Status Register (01H or 31H or 11H)

The Write Status Register instruction allows the Status Registers to be written. The Status Register-1 can be written by the Write Status Register 01h instruction; The Status Register-2 be written by the Write Status Register 01h or 31h instruction; Status Register-3 can be written by the Write Status Register 11h instruction. When the Write Status Register instruction 01h is followed by 1 byte data, the data will be written to Status Register-1. When the Write Status Register instruction 01h is followed by 2 bytes of data, the first byte data will be written to Status Register-1, and the second byte data will be written to Status Register-2; And Write Status Register instruction 31h or 11h can only follow 1 byte data, the data will be written to Status Register-2、Status Register-3 respectively. The writable Status Register bits include: SRP0, BP[4:0] in Status Register-1; CMP, LB[3:1], QE, SRP1 in Status Register- 2; ADS, ADP, DRV1, DRV0, Hold/RES in Status Register- 3. All other Status Register bit locations are read-only and will not be affected by the Write Status Register instruction. LB[3:1] are non-volatile OTP bits, once it is set to 1, it cannot be cleared to 0.

The Write Status Register instruction allows new values to be written to the Status Register. Before it can be accepted, a Write Enable or Write Enable For Volatile SR instruction must previously have been executed After the Write Enable instruction has been decoded and executed, the device sets the Write Enable Latch (WEL).

The Write Status Register instruction has no effect on S15 (SUS1), S10 (SUS2), S1 (WEL) and S0 (WIP) of the Status Register. /CS must be driven high after the 8 or 16 bit of the data byte has been latched in. If not, the Write Status Register (WRSR) instruction is not executed. As soon as /CS is driven high, the self-timed Write Status Register cycle (whose duration is tW) is initiated. While the Write Status Register cycle is in progress, the Status Register may still be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Write Status Register cycle, and is 0 when it is completed. When the cycle is completed, the Write Enable Latch (WEL) is reset.

The Write Status Register instruction allows the user to change the values of the Block Protect (BP4, BP3, BP2, BP1, and BP0) bits, to define the size of the area that is to be treated as read-only, as defined in ***Table 7*** and ***Table 8***. The Write Status Register (WRSR) instruction also allows the user to set or reset the Status Register Protect (SRP1 and SRP0) bits in accordance with the Write Protect (/WP) signal. The Status Register Protect (SRP1 and SRP0) bits and Write Protect (/WP) signal allow the device to be put in the Hardware Protected Mode. The Write Status Register instruction is not executed once the Hardware Protected Mode is entered.

The sequence of issuing WRSR instruction is: /CS goes low→ sending WRSR instruction code→ Status Register data on SI→/CS goes high.

The /CS must go high exactly at the 8 bits or 16 bits data boundary; otherwise, the instruction will be rejected and not executed. The self-timed Write Status Register cycle time (tW) is initiated as soon as Chip Select (/CS) goes high. The Write in Progress (WIP) bit still can be checked during the Write Status Register cycle is in progress. The WIP is set 1 during the tW timing, and is set 0 when Write Status Register Cycle is completed, and the Write Enable Latch (WEL) bit is reset.

Figure 17. Write Status Register Sequence Diagram-01H 2byte (SPI Mode)

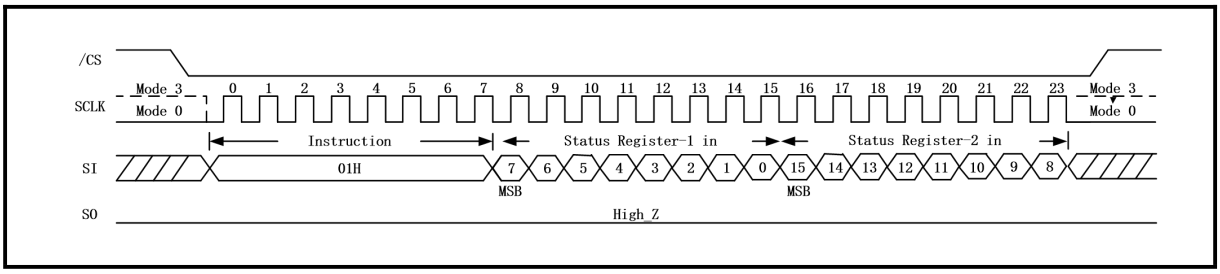


Figure 18. Write Status Register Sequence Diagram-01H 2byte (QPI Mode)

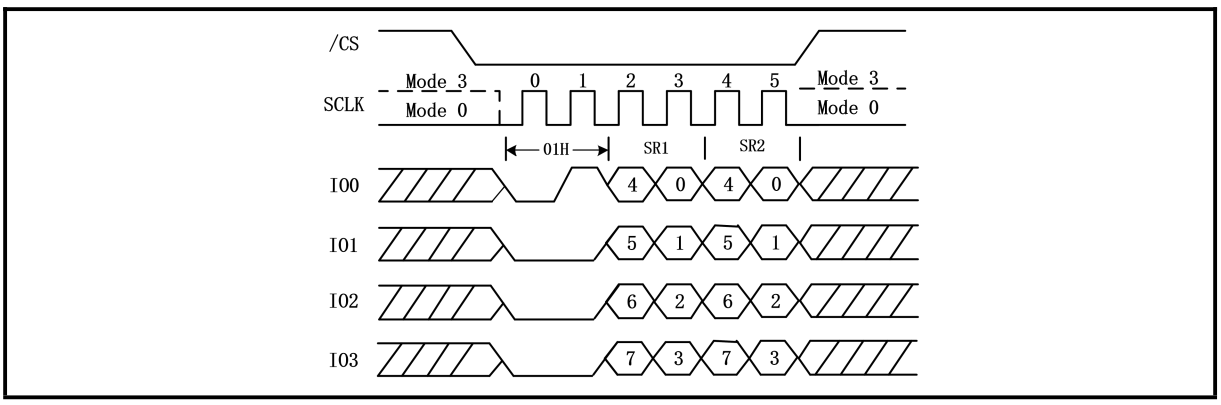


Figure 19. Write Status Register Sequence Diagram-01/31/11H 1byte (SPI Mode)

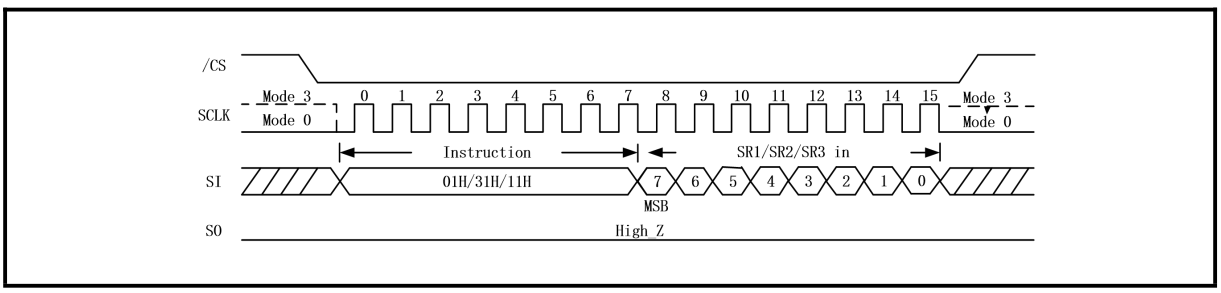
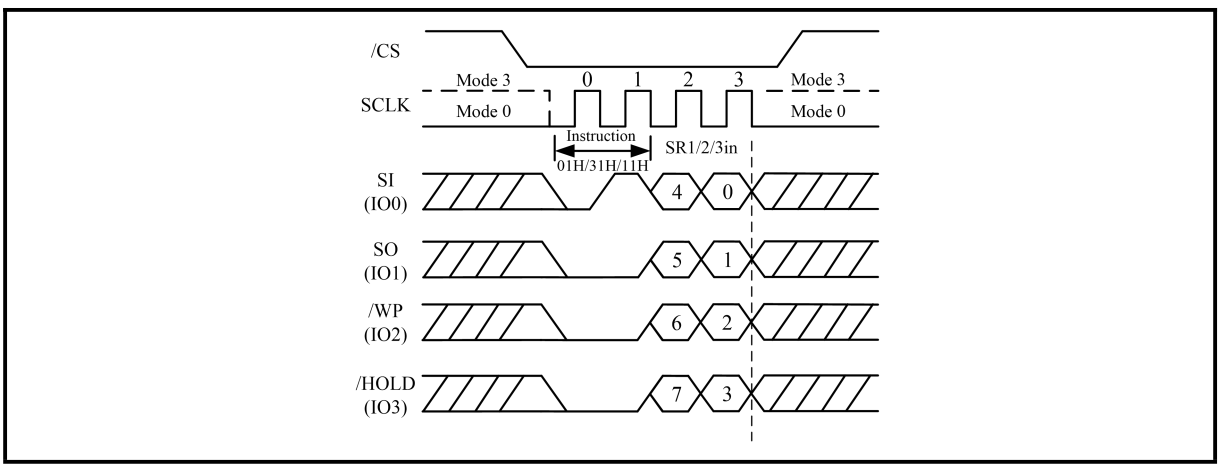


Figure 20. Write Status Register Sequence Diagram-01/31/11H 1byte (QPI Mode)



7.1.6 Read Extended Address Register (C8H)

When the device is in the 3-Byte Address Mode, the Extended Address Register is used as the 4th address byte A[31:24] to access memory regions beyond 128Mb. The Read Extended Address Register instruction is entered by driving /CS low and shifting the instruction code “C8h” into the SI pin on the rising edge of CLK. The Extended Address Register bits are then shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first as shown in ***Figure 21-Figure 22***.

When the device is in the 4-Byte Address Mode, the Extended Address Register is not used.

Figure 21. Read Extended Address Register (SPI Mode)

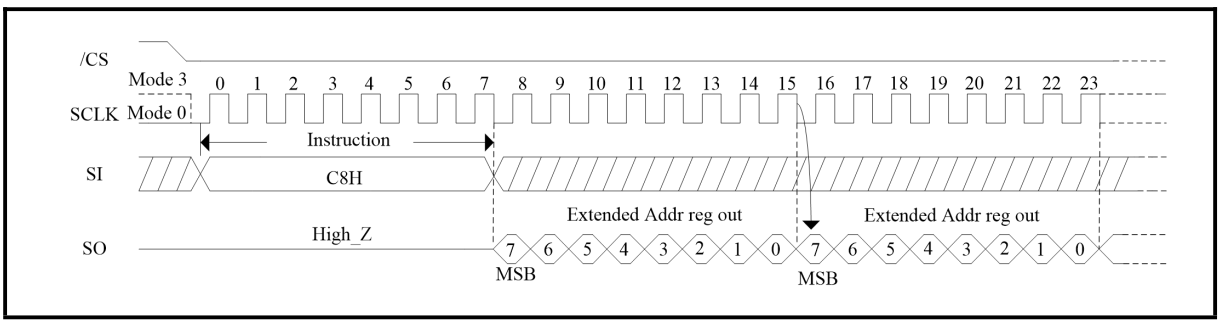
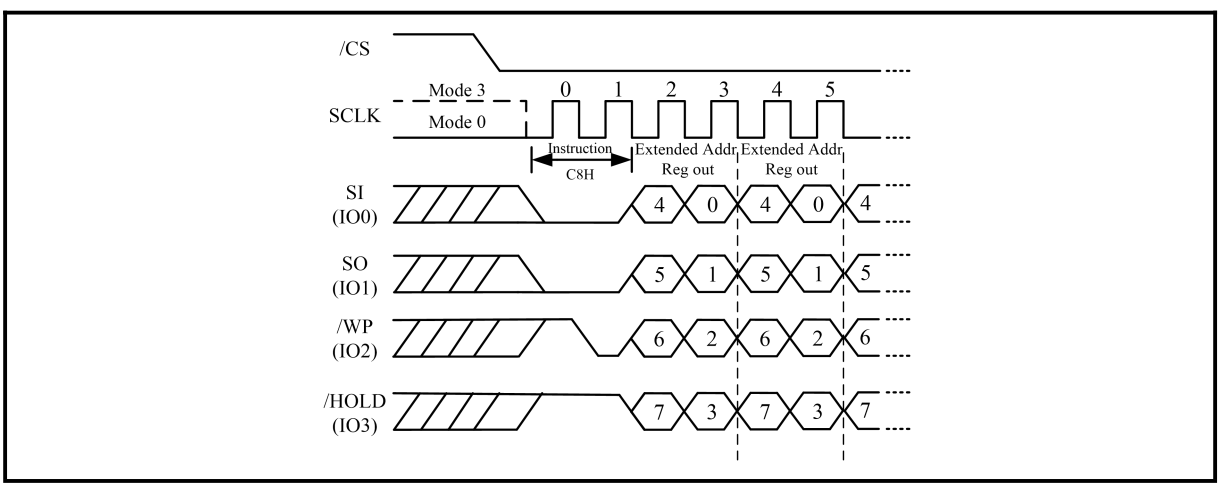


Figure 22. Read Extended Address Register (QPI Mode)



7.1.7 Write Extended Address Register (C5H)

The Extended Address Register is a volatile register that stores the 4th byte address (A31-A24) when the device is operating in the 3-Byte Address Mode (ADS=0). To write the Extended Address Register bits, a Write Enable (06h) instruction must previously have been executed for the device to accept the Write Extended Address Register instruction (Status Register bit WEL must equal 1). Once write enabled, the instruction is entered by driving /CS low, sending the instruction code "C5h", and then writing the Extended Address Register data byte as illustrated in ***Figure 23-Figure 24***.

Upon power up or the execution of a Software reset, the Extended Address Register bit values will be cleared to 0.

The Extended Address Register is only effective when the device is in the 3-Byte Address Mode. When the device operates in the 4-Byte Address Mode (ADS=1), any instruction with address input of A31-A24 will replace the Extended Address Register values. It is recommended to check and update the Extended Address Register if necessary when the device is switched from 4-Byte to 3-Byte Address Mode.

Figure 23. Write Extended Address Register (SPI Mode)

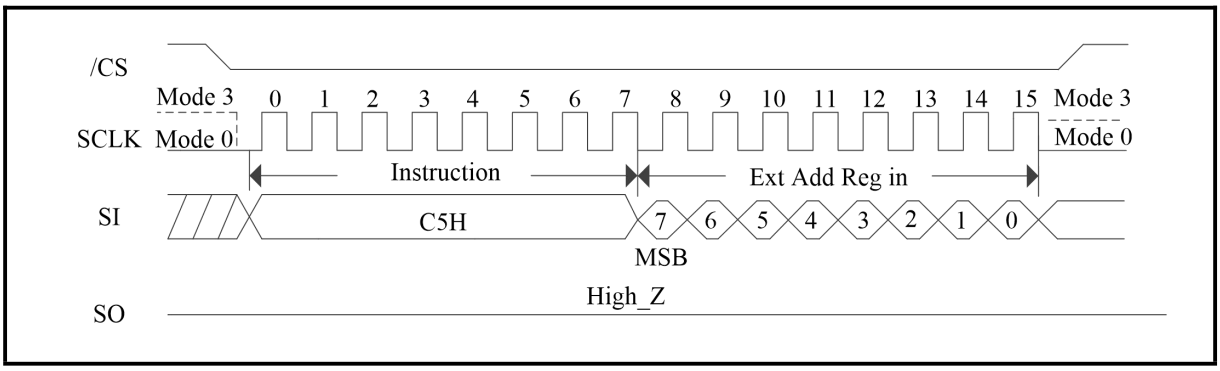
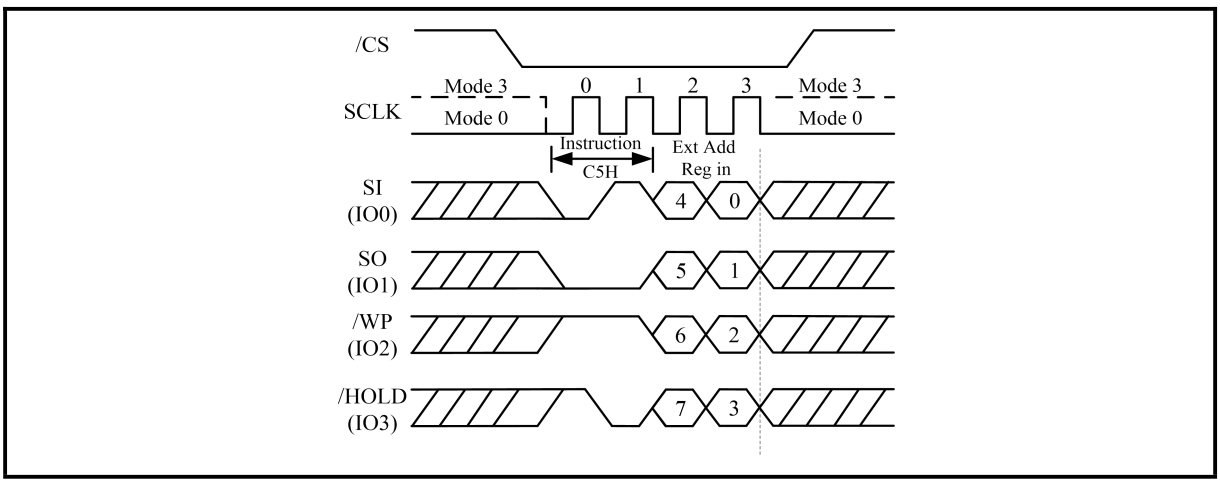


Figure 24. Write Extended Address Register (QPI Mode)



7.1.8 Enter 4-Byte Address Mode (B7H)

The Enter 4-Byte Address Mode instruction (***Figure 25-Figure 26***) will allow 32-bit address (A31-A0) to be used to access the memory array beyond 128Mb. The Enter 4-Byte Address Mode instruction is entered by driving /CS low, shifting the instruction code “B7h” into the SI pin and then driving /CS high.

Figure 25. Enter 4-Byte Address Mode instruction (SPI Mode)

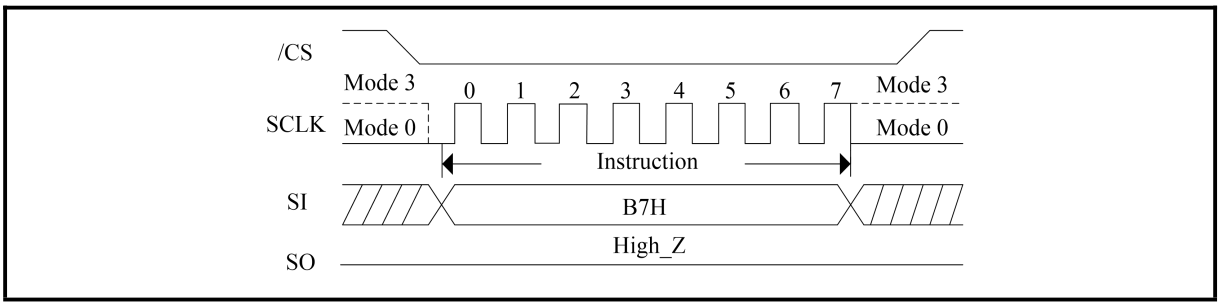
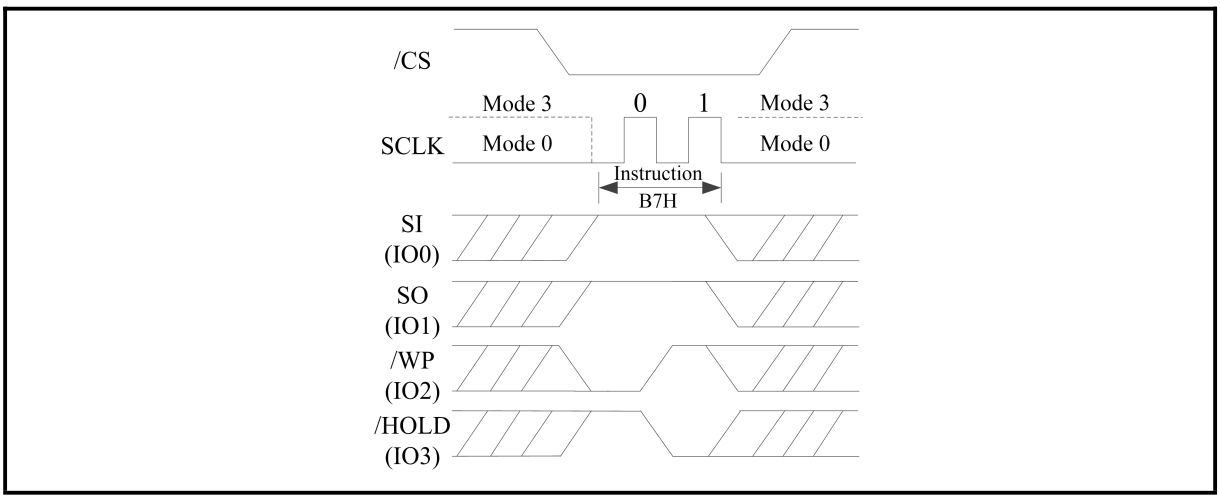


Figure 26. Enter 4-Byte Address Mode instruction (QPI Mode)



7.1.9 Exit 4-Byte Address Mode (E9H)

In order to be backward compatible, the Exit 4-Byte Address Mode instruction (***Figure 27-Figure 28***) will only allow 24-bit address (A23-A0) to be used to access the memory array up to 128Mb. The Extended Address Register must be used to access the memory array beyond 128Mb. The Exit 4-Byte Address Mode instruction is entered by driving /CS low, shifting the instruction code "E9h" into the SI pin and then driving /CS high.

Figure 27. Exit 4-Byte Address Mode (SPI Mode)

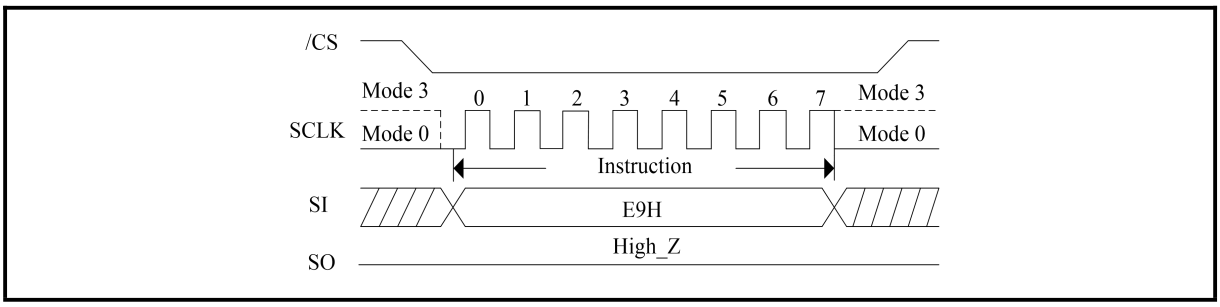
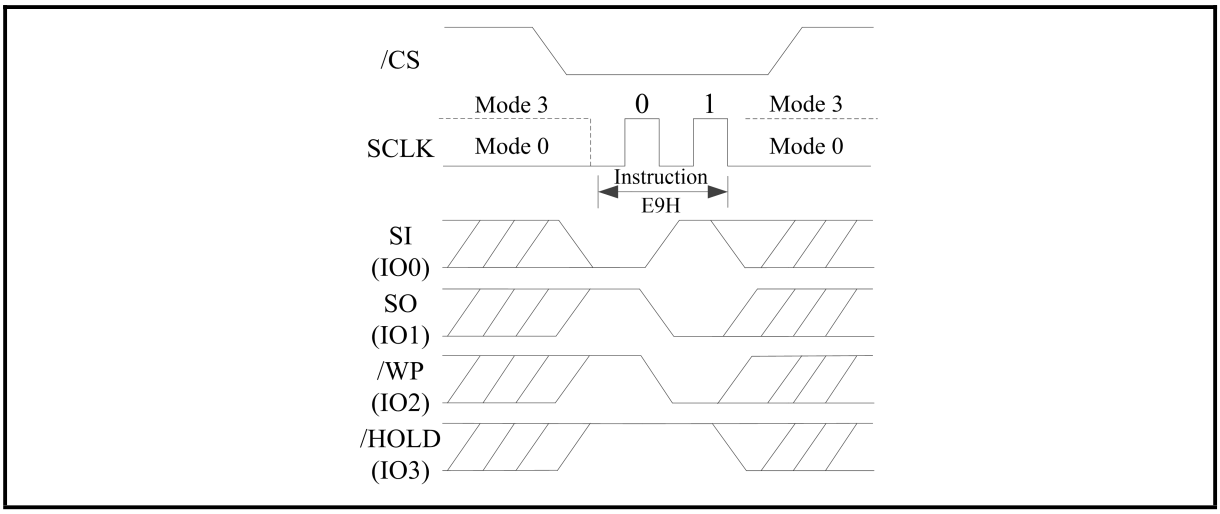


Figure 28. Exit 4-Byte Address Mode (QPI Mode)



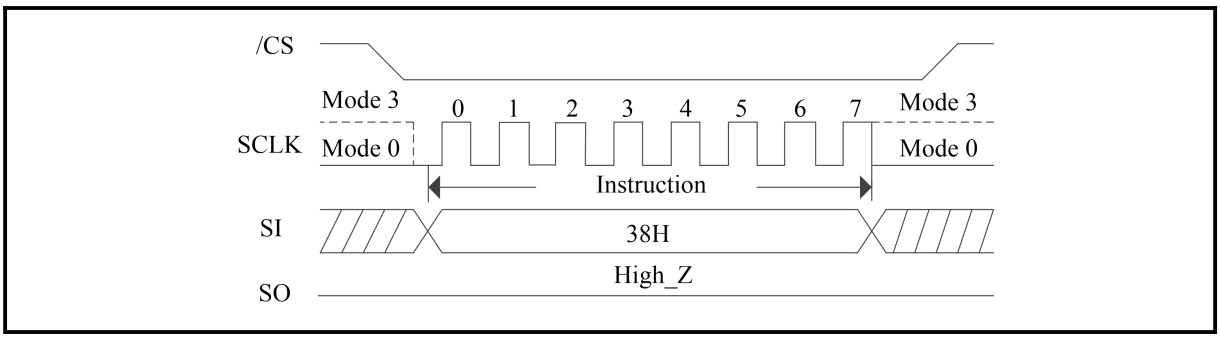
7.1.10 Enter QPI Mode (38H)

The BY25FQ256 support both Standard/Dual/Quad Serial Peripheral Interface (SPI) and Quad Peripheral Interface (QPI). However, SPI mode and QPI mode cannot be used at the same time. “Enter QPI (38h)” instruction is the only way to switch the device from SPI mode to QPI mode.

Upon power-up, the default state of the device upon is Standard/Dual/Quad SPI mode. This provides full backward compatibility with earlier generations of BoyaMicro serial flash memories. See Instruction Set ***Table 12*** for all supported SPI instructions. In order to switch the device to QPI mode, the Quad Enable (QE) bit in Status Register-2 must be set to 1 first, and an “Enter QPI (38h)” instruction must be issued. If the Quad Enable (QE) bit is 0, the “Enter QPI (38h)” instruction will be ignored and the device will remain in SPI mode.

When the device is switched from SPI mode to QPI mode, the existing Write Enable and Program/Erase Suspend status, and the Wrap Length setting will remain unchanged.

Figure 29. Enter QPI Mode (SPI Mode)

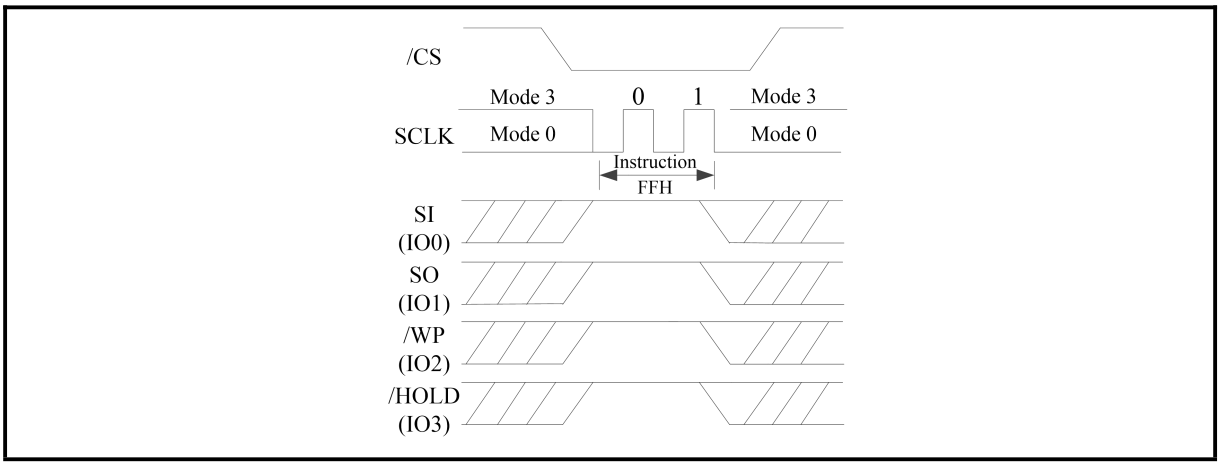


7.1.11 Exit QPI Mode (FFH)

In order to exit the QPI mode and return to the Standard/Dual/Quad SPI mode, an “Exit QPI (FFh)” instruction must be issued.

When the device is switched from QPI mode to SPI mode, the existing Write Enable Latch (WEL) and Program/Erase Suspend status, and the Wrap Length setting will remain unchanged.

Figure 30. Exit QPI Mode (QPI Mode)



7.1.12 Enable Reset (66H) and Reset Device (99H)

Because of the small package and the limitation on the number of pins, the BY25FQ256 provides a software reset instruction instead of a dedicated RESET pin. Once the software reset instruction is accepted, any on-going internal operations will be terminated and the device will return to its default power-on state and lose all the current volatile settings, such as Volatile Status Register bits, Write Enable Latch (WEL) status, Program/Erase Suspend status, Continuous Read Mode bit setting (M7-M0) and Wrap Bit setting (W6-W4).

To avoid accidental reset, both “Enable Reset (66h)” and “Reset (99h)” instructions must be issued in sequence. Any other instructions other than “Reset (99h)” after the “Enable Reset (66h)” instruction will disable the “Reset Enable” state. A new sequence of “Enable Reset (66h)” and “Reset (99h)” is needed to reset the device. Once the Reset instruction is accepted by the device, the device will take approximately tRST to reset. During this period, no instruction will be accepted.

The Enable Reset (66h) and Reset (99h) instruction sequence is shown in ***Figure 31-Figure 32***.

Data corruption may happen if there is an on-going or suspended internal Erase or Program operation when Reset instruction sequence is accepted by the device. It is recommended to check the BUSY bit and the SUS bit in Status Register before issuing the Reset instruction sequence.

Figure 31. Enable Reset (66h) and Reset (99h) Instruction Sequence (SPI Mode)

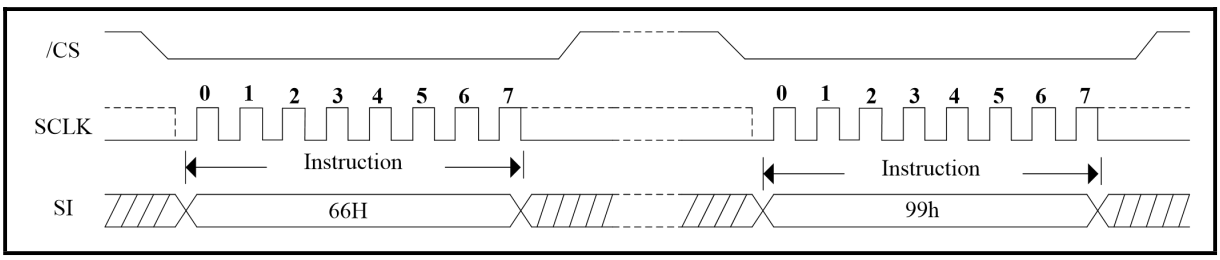
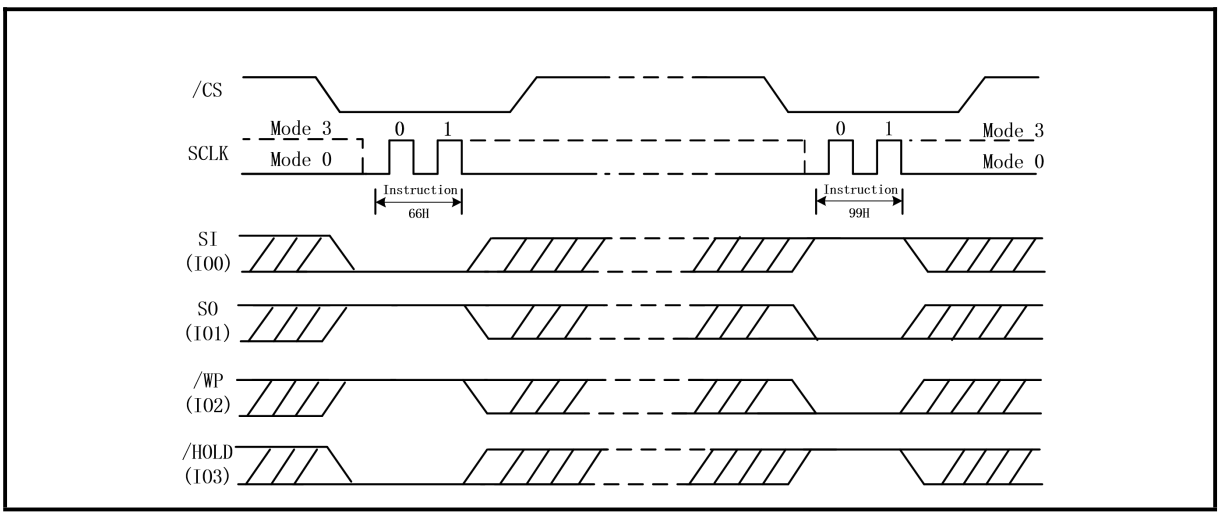


Figure 32. Enable Reset (66h) and Reset (99h) Instruction Sequence (QPI Mode)



7.2 Read Instructions

7.2.1 Read Data (03H)

See ***Figure 33-Figure 34***, the Read Data Bytes (READ) instruction is followed by a 3-byte/4-byte address (A23/31-A0), each bit being latched-in during the rising edge of SCLK. Then the memory content, at that address, is shifted out on SO, each bit being shifted out, at a Max frequency fR, during the falling edge of SCLK. The address is automatically incremented to the next higher address after each byte of data is shifted out allowing for a continuous stream of data. This means that the entire memory can be accessed with a single instruction as long as the clock continues. The instruction is completed by driving /CS high. The whole memory can be read with a single Read Data Bytes (READ) instruction. Any Read Data Bytes (READ) instruction, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

Figure 33. Read Data Bytes Sequence Diagram (SPI Mode/3-Byte Address Mode)

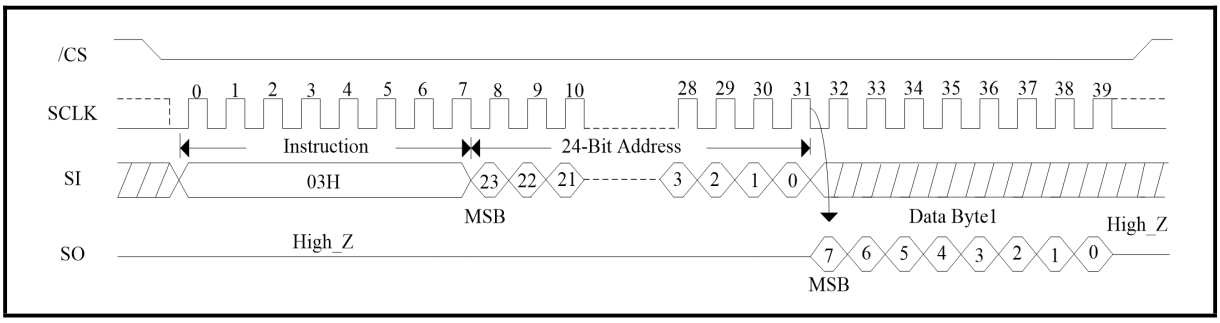
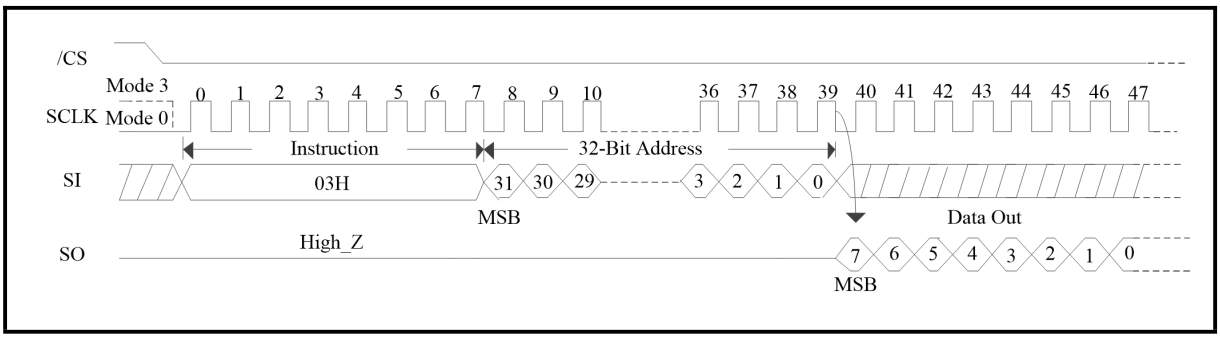


Figure 34. Read Data Bytes Sequence Diagram (SPI Mode/4-Byte Address Mode)



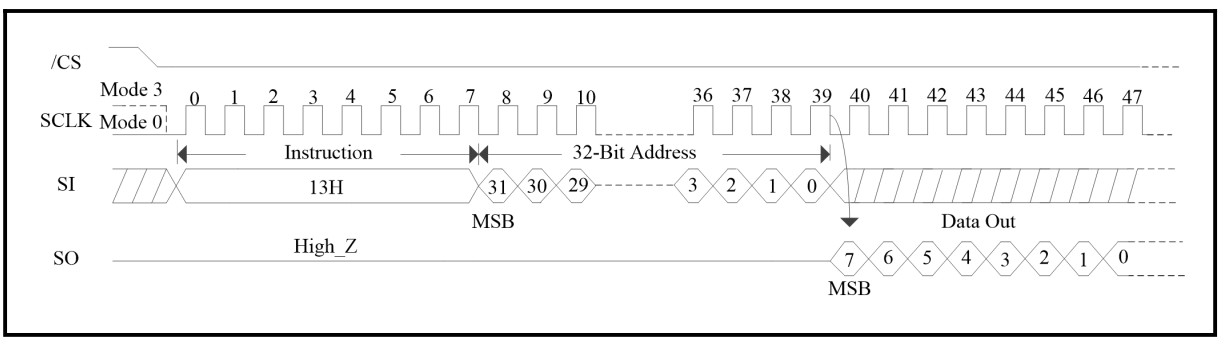
7.2.2 Read Data with 4-Byte Address (13H)

The Read Data with 4-Byte Address instruction is similar to the Read Data (03h) instruction. Instead of 24- bit address, 32-bit address is needed following the instruction code 13h. No matter the device is operating in 3-Byte Address Mode or 4-byte Address Mode, the Read Data with 4-Byte Address instruction will always require 32-bit address to access the entire 256Mb memory.

The Read Data with 4-Byte Address instruction sequence is shown in ***Figure 35***. If this instruction is issued while an Erase, Program or Write cycle is in process (WIP=1) the instruction is ignored and will not have any effects on the current cycle. The Read Data with 4-Byte Address instruction allows clock rates from D.C. to a maximum of fR (see AC Electrical Characteristics).

The Read Data with 4-Byte Address (13h) instruction is only supported in Standard SPI mode.

Figure 35. Read Data with 4-Byte Address Sequence Diagram (SPI Mode)



7.2.3 Fast Read (0BH)

See ***Figure 36-Figure 39***, the Read Data Bytes at Higher Speed (Fast Read) instruction is for quickly reading data out. It is followed by a 3-byte/4-byte address (A23/31-A0) and a dummy byte, each bit being latched-in during the rising edge of SCLK. Then the memory content, at that address, is shifted out on SO, each bit being shifted out, at a Max frequency fc, during the falling edge of SCLK. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out.

Figure 36. Fast Read Sequence Diagram (SPI Mode/3-Byte Address Mode)

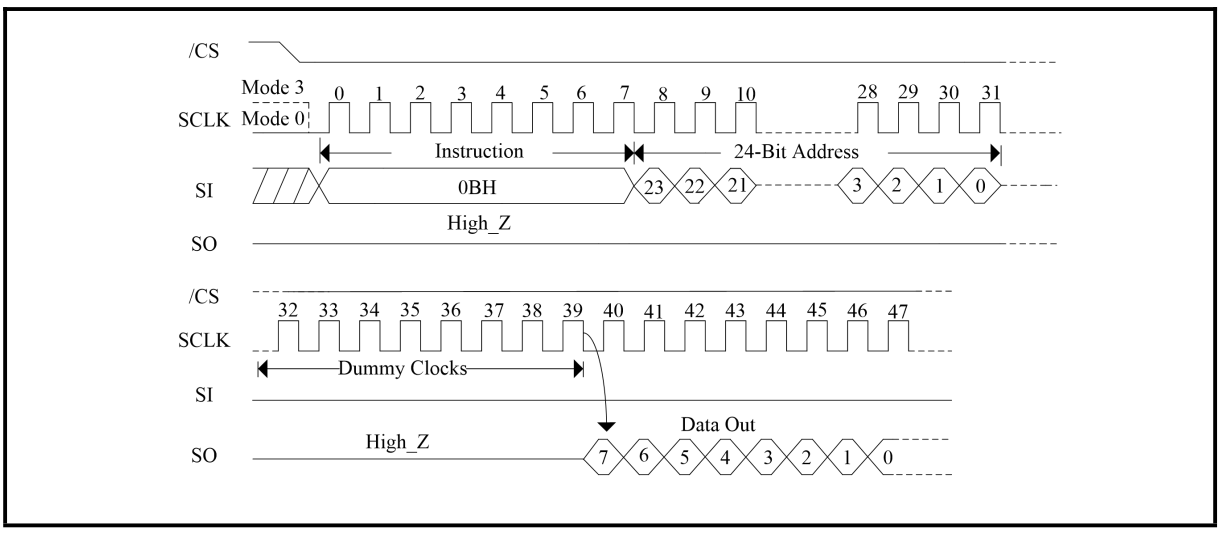
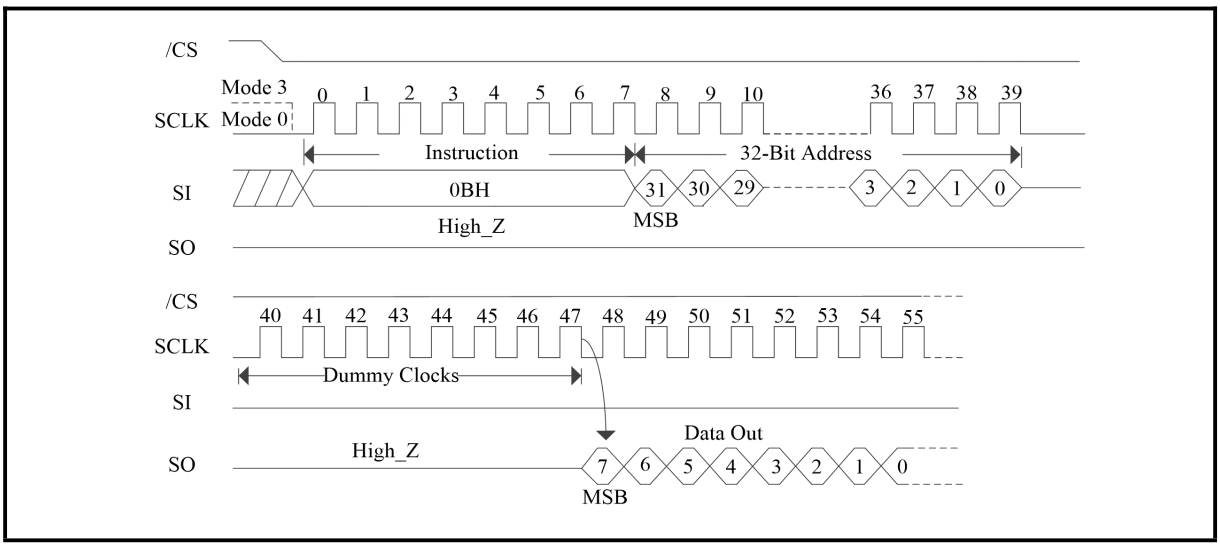


Figure 37. Fast Read Sequence Diagram (SPI Mode/4-Byte Address Mode)



Fast Read (0Bh) in QPI Mode

The Fast Read instruction is also supported in QPI mode. When QPI mode is enabled, the number of dummy clocks is configured by the “Set Read Parameters (C0h)” instruction to accommodate a wide range of applications with different needs for either maximum Fast Read frequency or minimum data access latency. Depending on the Read Parameter Bits P[6:4] setting, the number of dummy clocks can be configured as either 4-18. The default number of dummy clocks upon power up or after a Reset instruction is 4.

Figure 38. Fast Read Sequence Diagram (QPI Mode/3-Byte Address Mode)

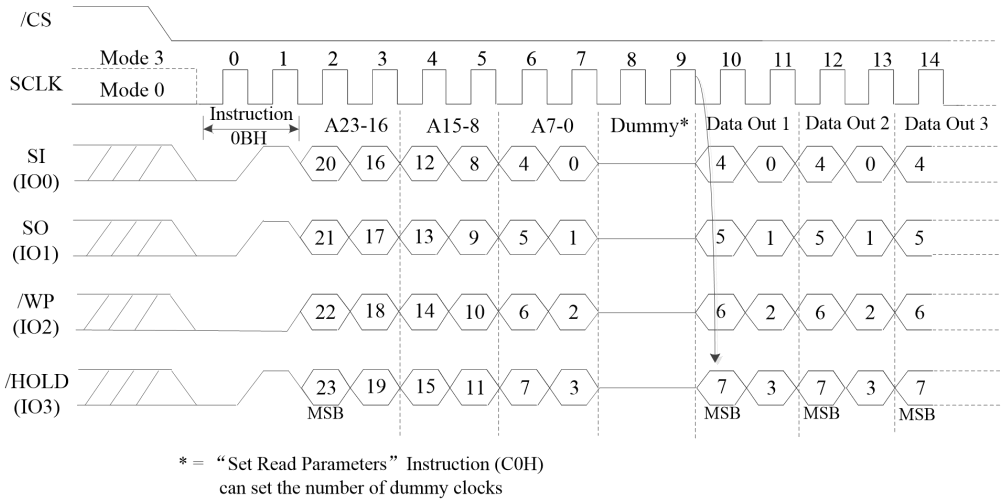
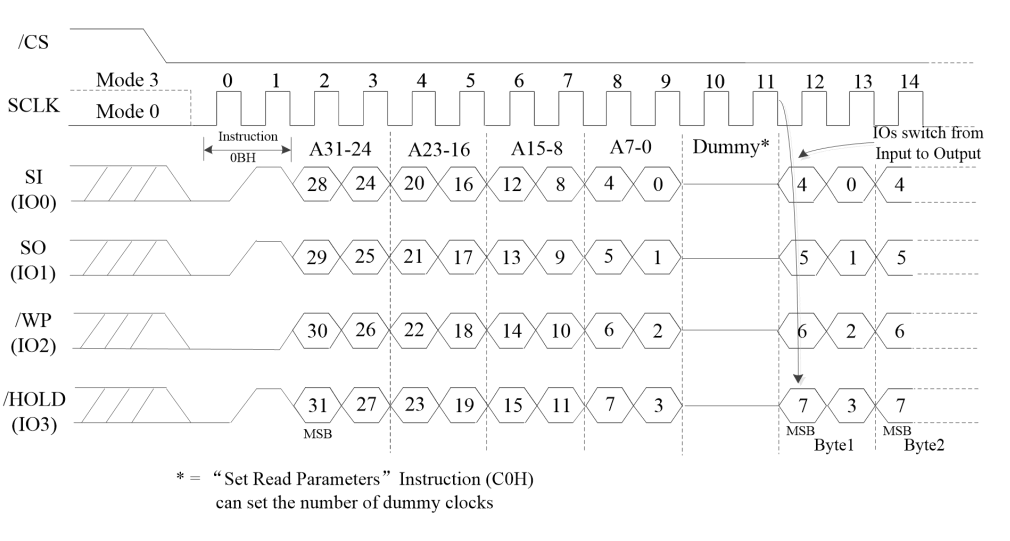


Figure 39. Fast Read Sequence Diagram (QPI Mode/4-Byte Address Mode)

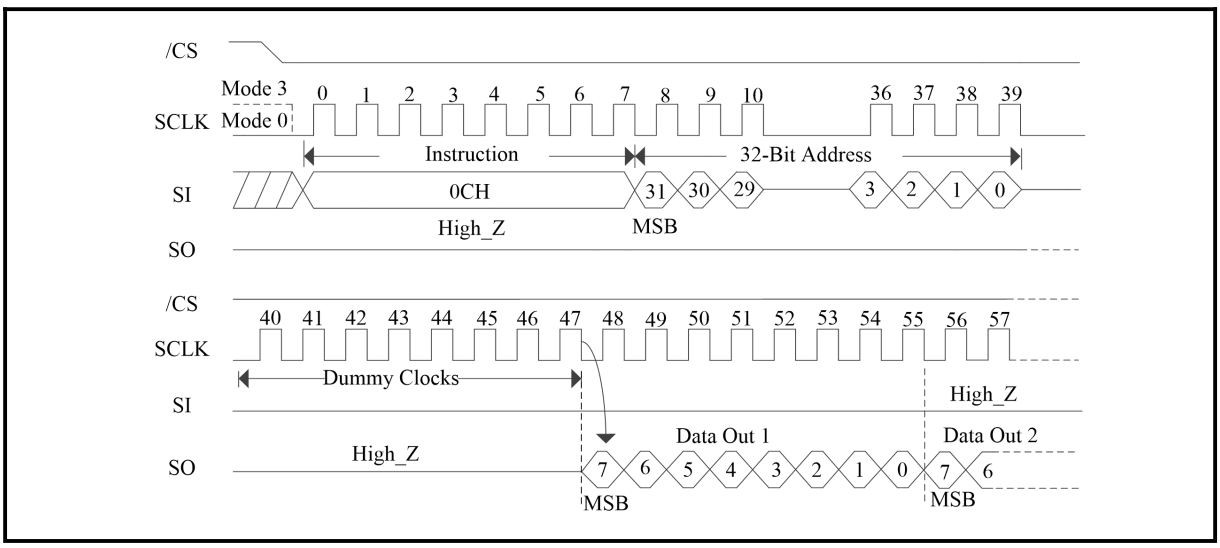


7.2.4 Fast Read with 4-Byte Address (0CH)

The Fast Read with 4-Byte Address (0Ch) instruction is similar to the Fast Read instruction except that it requires 32-bit address instead of 24-bit address. No matter the device is operating in 3-Byte Address Mode or 4-byte Address Mode, the Read Data with 4-Byte Address instruction will always require 32-bit address to access the entire 256Mb memory.

The Fast Read with 4-Byte Address instruction is only supported in Standard SPI mode. In QPI mode, the instruction code 0Ch is used for the “Burst Read with Wrap” instruction.

Figure 40. Fast Read with 4-Byte Address



7.2.5 Dual Output Fast Read (3BH)

See ***Figure 41-Figure 42***, the Dual Output Fast Read instruction is followed by 3/4-byte address (A23/31-A0) and a dummy byte, each bit being latched in during the rising edge of SCLK, then the memory contents are shifted out 2-bit per clock cycle from SI and SO. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out.

Figure 41. Dual Output Fast Read Sequence Diagram (SPI Mode/3-Byte Address Mode)

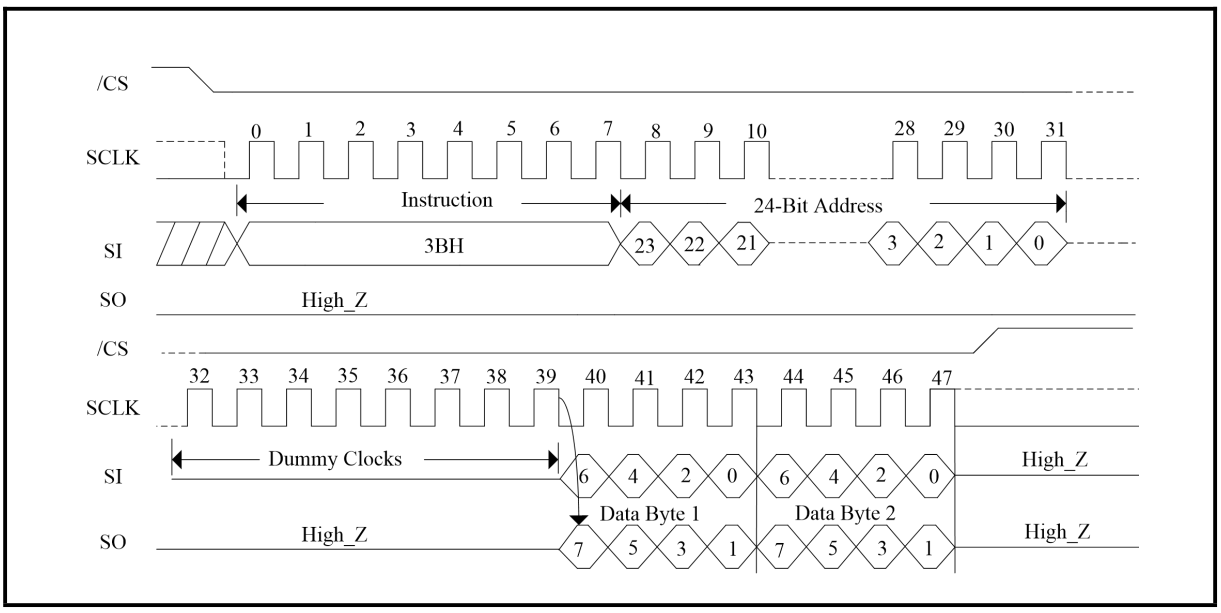
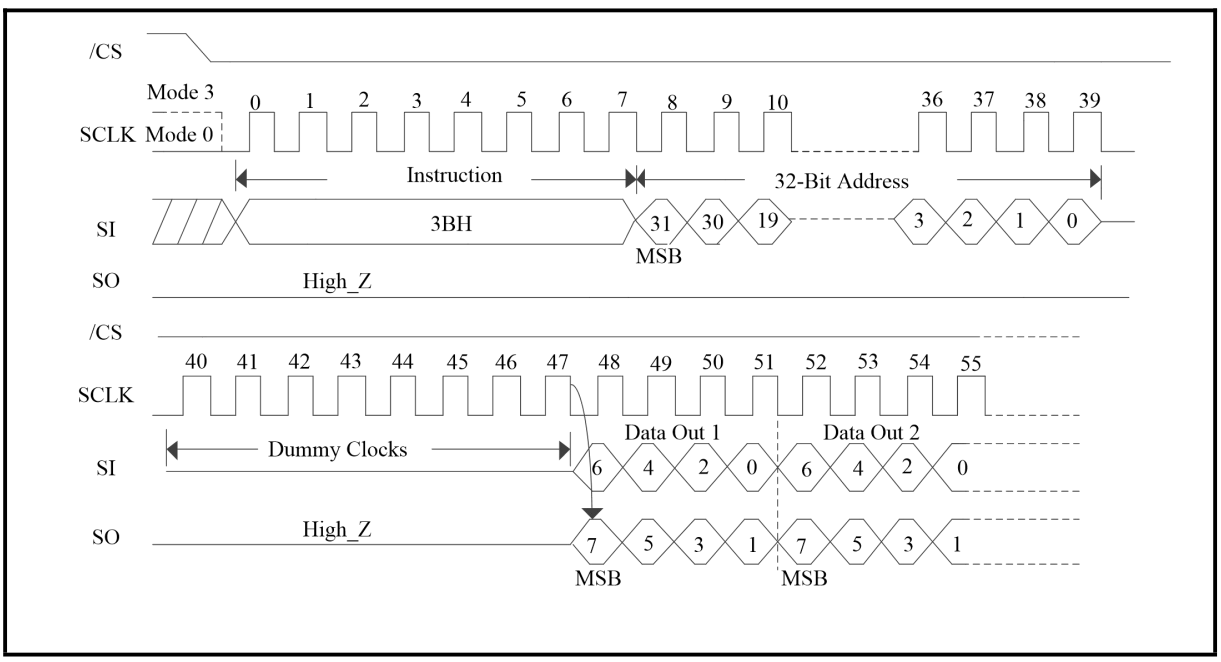


Figure 42. Dual Output Fast Read Sequence Diagram (SPI Mode/4-Byte Address Mode)

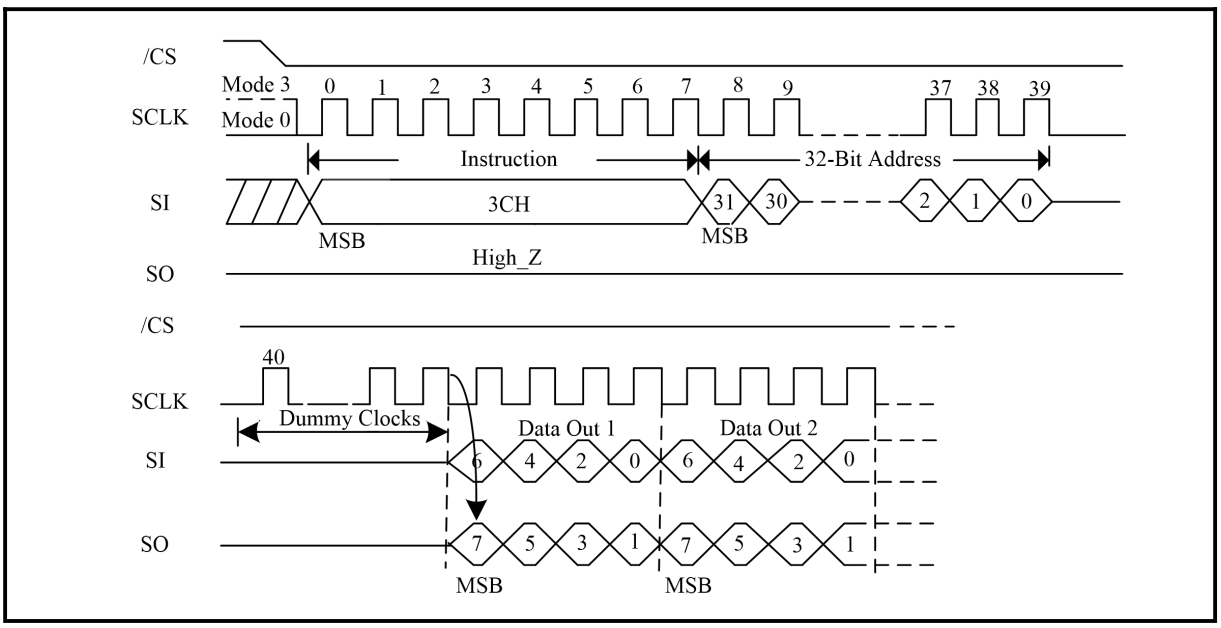


7.2.6 Fast Read Dual Output with 4-Byte Address (3CH)

The Fast Read Dual Output with 4-Byte Address instruction is similar to the Fast Read Dual Output instruction except that it requires 32-bit address instead of 24-bit address. No matter the device is operating in 3-Byte Address Mode or 4-byte Address Mode, the Fast Read Dual Output with 4-Byte Address instruction will always require 32-bit address to access the entire 256Mb memory.

The Fast Read Dual Output with 4-Byte Address (3Ch) instruction is only supported in Standard SPI mode.

Figure 43. Fast Read Dual Output with 4-Byte Address



7.2.7 Quad Output Fast Read (6BH)

See ***Figure 44-Figure 45***, the Quad Output Fast Read instruction is followed by 3/4-byte address (A23/31-A0) and a dummy byte, each bit being latched in during the rising edge of SCLK, then the memory contents are shifted out 4-bit per clock cycle from IO3, IO2, IO1 and IO0. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The Quad Enable bit (QE) of Status Register must be set to enable.

Figure 44. Quad Output Fast Read Sequence Diagram (SPI Mode/3-Byte Address Mode)

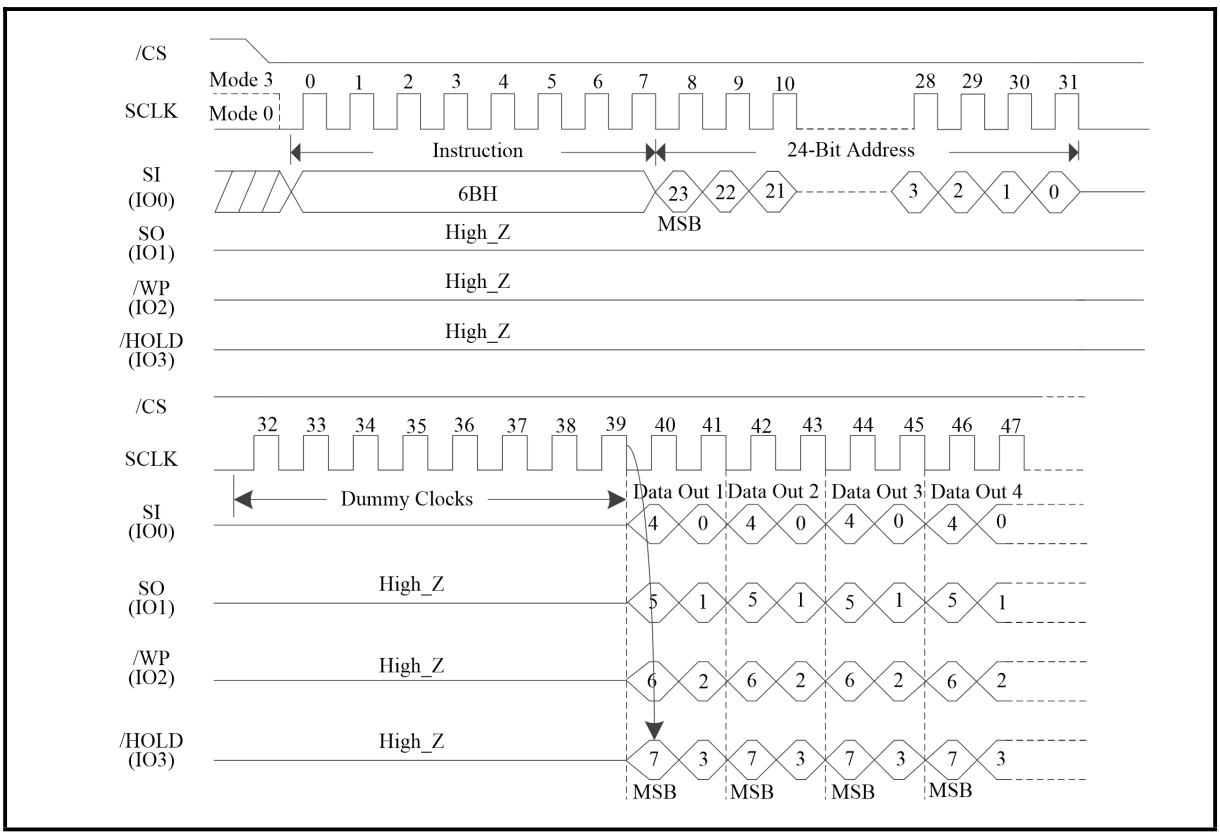
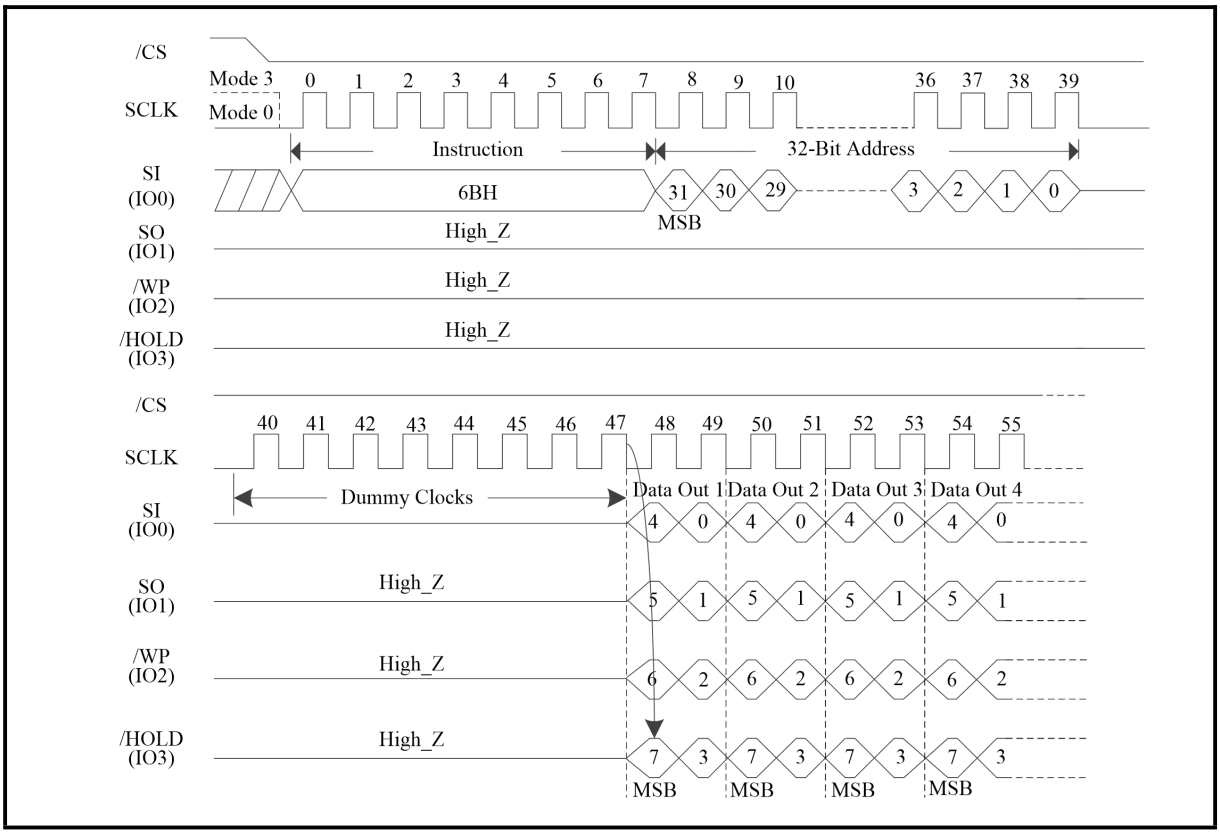


Figure 45. Quad Output Fast Read Sequence Diagram (SPI Mode/4-Byte Address Mode)

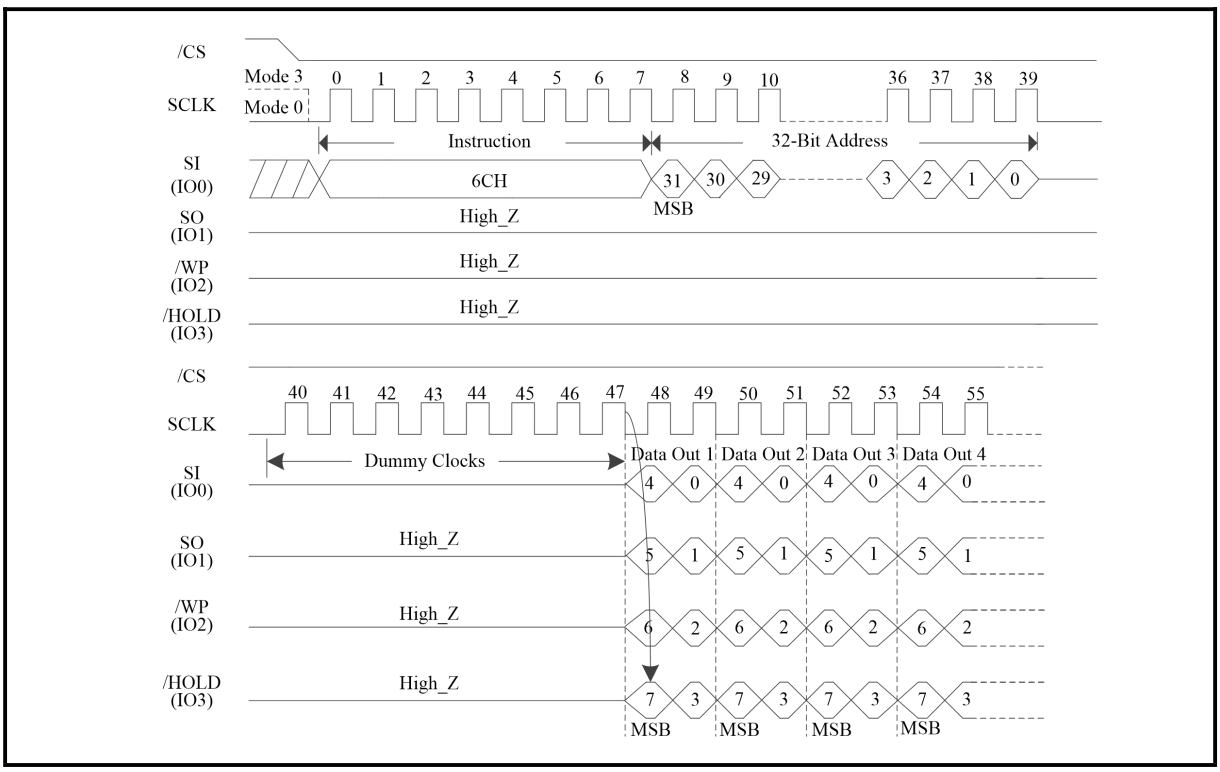


7.2.8 Fast Read Quad Output with 4-Byte Address (6CH)

The Fast Read Quad Output with 4-Byte Address instruction is similar to the Fast Read Quad Output instruction except that it requires 32-bit address instead of 24-bit address. No matter the device is operating in 3-Byte Address Mode or 4-byte Address Mode, the Fast Read Quad Output with 4-Byte Address instruction will always require 32-bit address to access the entire 256Mb memory.

The Fast Read Quad Output with 4-Byte Address (6Ch) instruction is only supported in Standard SPI mode.

Figure 46. Fast Read Quad Output with 4-Byte Address



7.2.9 Dual I/O Fast Read (BBH)

See ***Figure 47-Figure 50***, the Dual I/O Fast Read instruction is similar to the Dual Output Fast Read instruction but with the capability to input the 3/4-byte address (A23/31-0) and a “Continuous Read Mode” byte 2-bit per clock by SI and SO, each bit being latched in during the rising edge of SCLK, then the memory contents are shifted out 2-bit per clock cycle from SI and SO. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out.

Dual I/O Fast Read with “continuous Read Mode”

The Dual I/O Fast Read instruction can further reduce instruction overhead through setting the “continuous Read Mode” bits (M7-4) after the inputs 3-byte address A23-A0).If the “continuous Read Mode” bits(M5-4)=(1,0),then the next Dual I/O fast Read instruction (after CS/ is raised and then lowered) does not require the BBH instruction code. The instruction sequence is shown in the following ***Figure 47-Figure 50***.If the “continuous Read Mode” bits (M5-4) does not equal (1,0), the next instruction requires the first BBH instruction code, thus returning to normal operation. A “continuous Read Mode” Reset instruction can be used to reset (M5-4) before issuing normal instruction.

Figure 47. Dual I/O Fast Read Sequence Diagram (SPI Mode/3-Byte Address Mode; Initial instruction or previous (M5-4)≠(1,0))

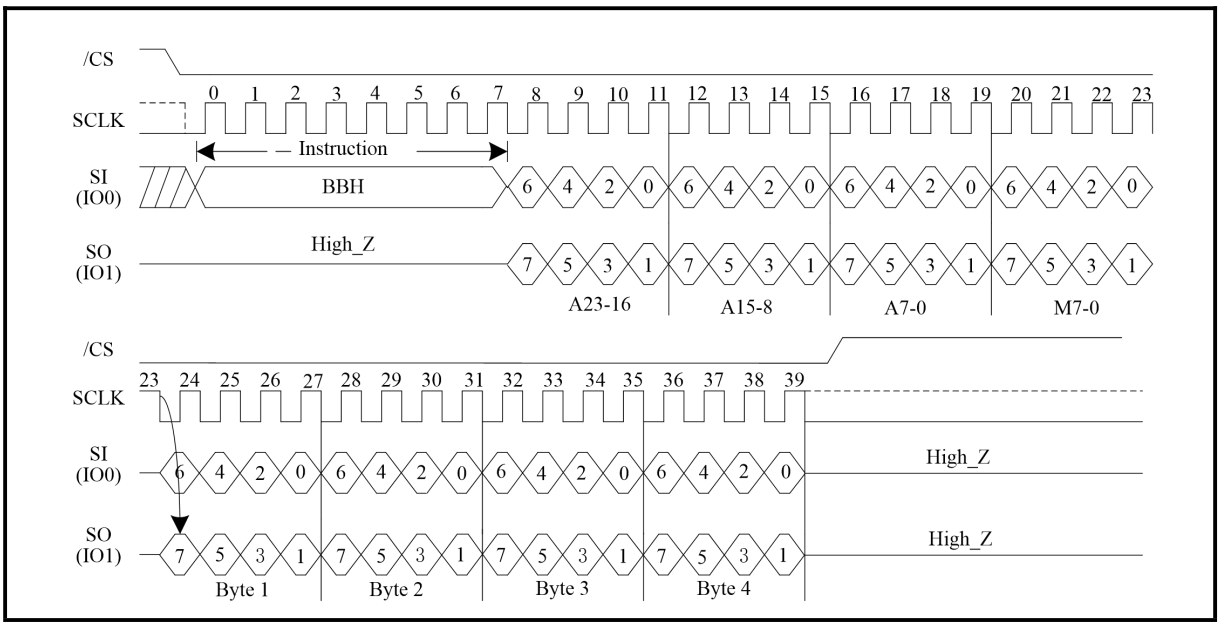


Figure 48. Dual I/O Fast Read Sequence Diagram (SPI Mode/4-Byte Address Mode; Initial instruction or previous (M5-4)≠(1,0))

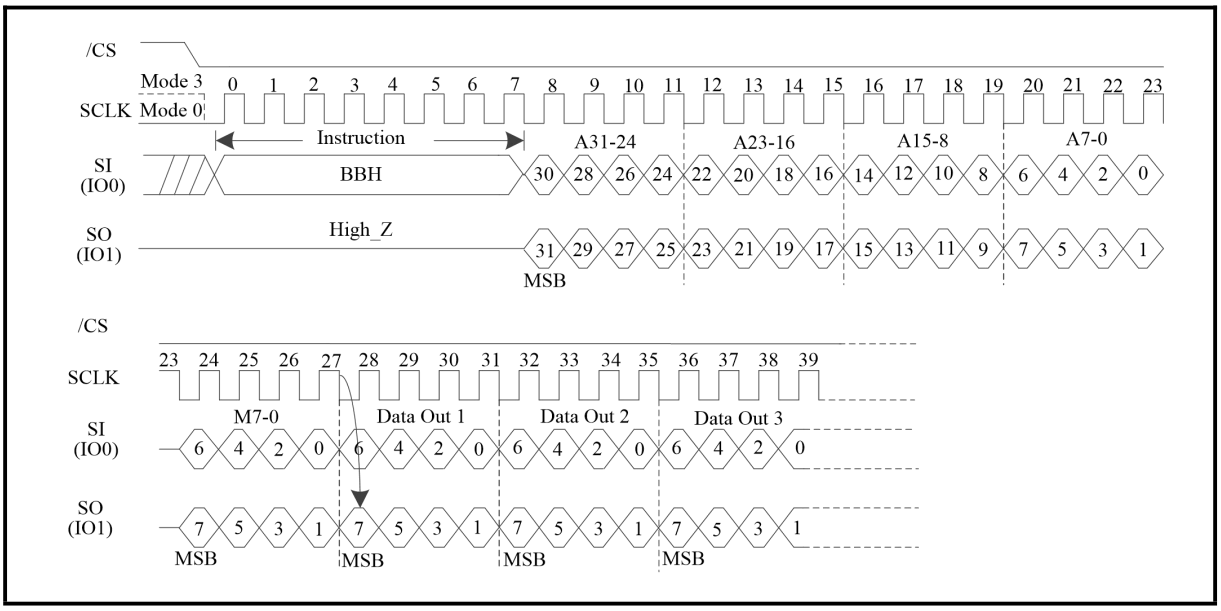


Figure 49. Dual I/O Fast Read Sequence Diagram (SPI Mode/3-Byte Address Mode; Previous instruction set (M5-4) =(1,0))

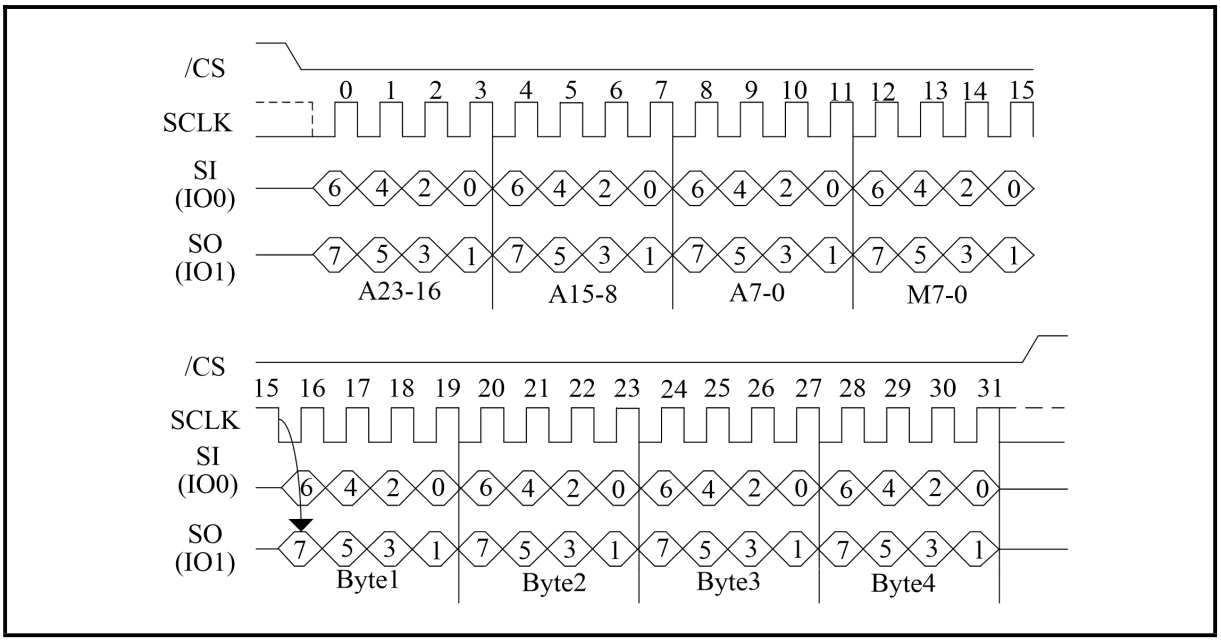
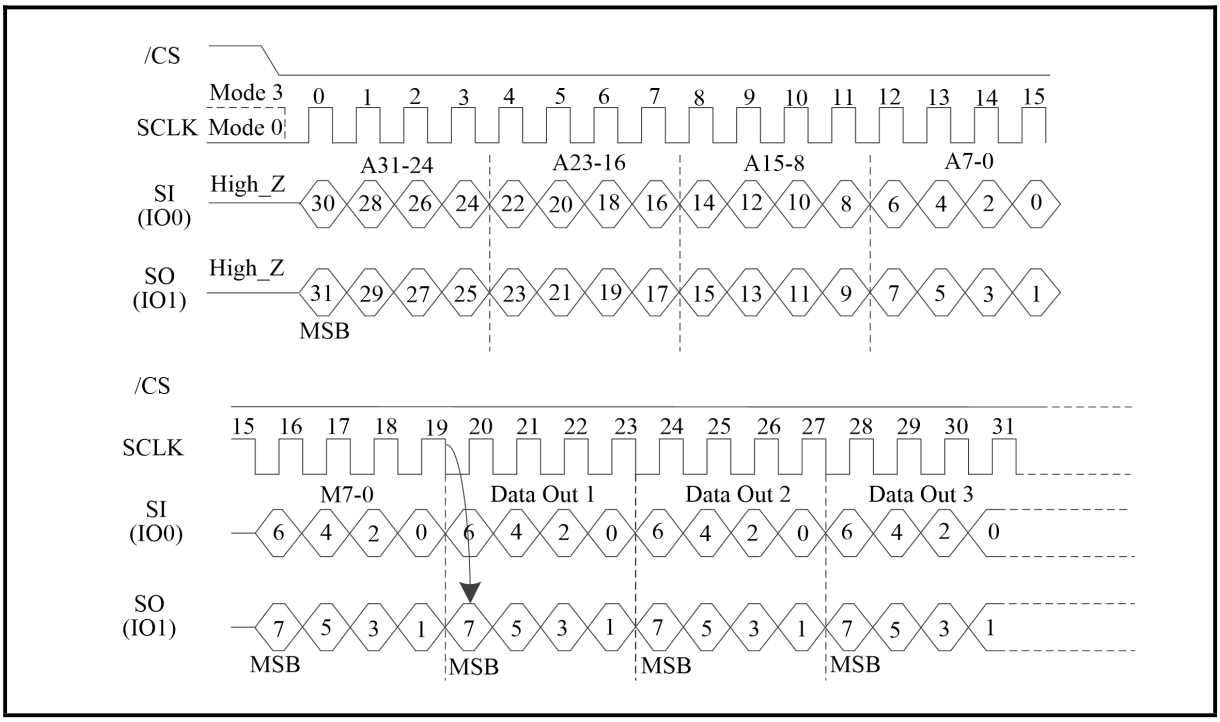


Figure 50. Dual I/O Fast Read Sequence Diagram (SPI Mode/4-Byte Address Mode; Previous instruction set (M5-4) =(1,0))



7.2.10 Fast Read Dual I/O with 4-Byte Address (BCH)

The Fast Read Dual I/O with 4-Byte Address instruction is similar to the Fast Read Dual I/O instruction except that it requires 32-bit address instead of 24-bit address. No matter the device is operating in 3-Byte Address Mode or 4-byte Address Mode, the Fast Read Dual I/O with 4-Byte Address instruction will always require 32-bit address to access the entire 256Mb memory.

The Fast Read Dual I/O with 4-Byte Address (BCh) instruction is only supported in Standard SPI mode.

Figure 51. Fast Read Dual I/O with 4-Byte Address(SPI Mode only; Initial instruction or previous M5-4≠10)

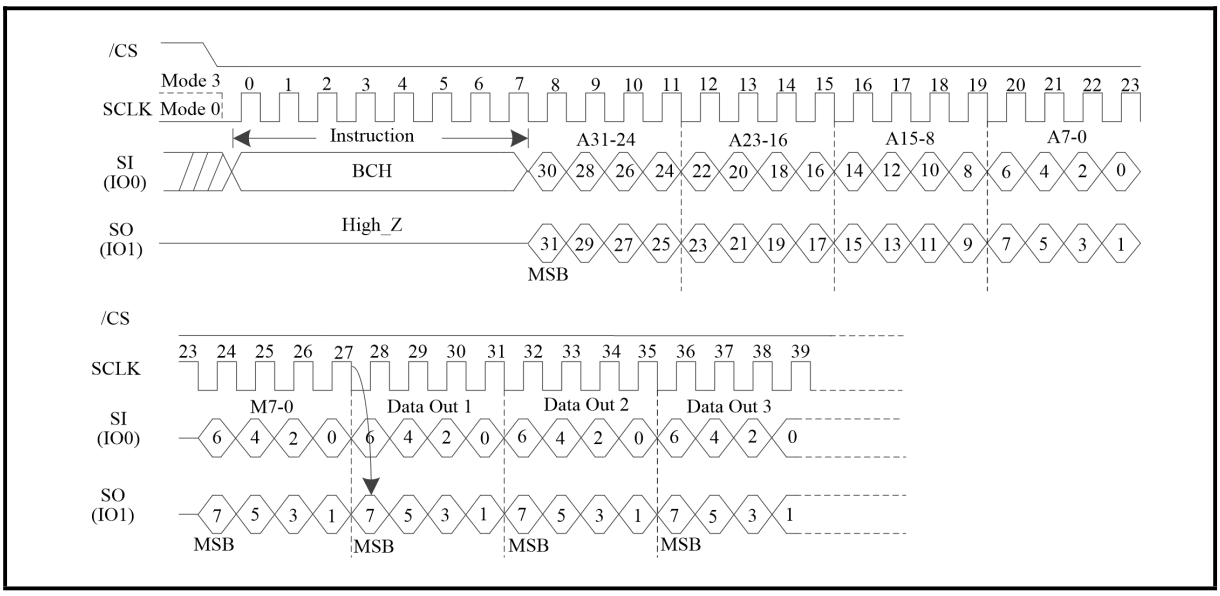
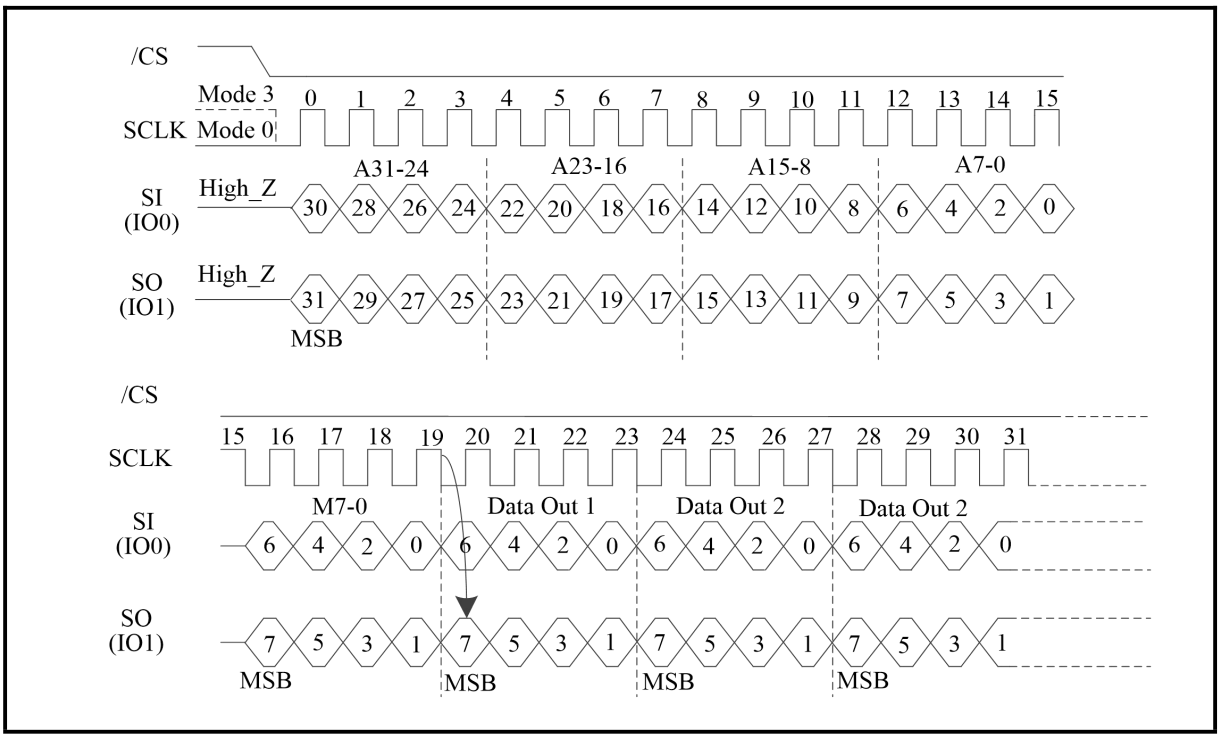


Figure 52. Fast Read Dual I/O with 4-Byte Address(SPI Mode only; Initial instruction or previous M5-4=10)



7.2.11 Quad I/O Fast Read (EBH)

See ***Figure 53-Figure 56***, the Quad I/O Fast Read instruction is similar to the Dual I/O Fast Read instruction but with the capability to input the 3/4-byte address (A23/31-0) and a "Continuous Read Mode" byte and 4-dummy clock 4-bit per clock by IO0, IO1, IO3, IO4, each bit being latched in during the rising edge of SCLK, then the memory contents are shifted out 4-bit per clock cycle from IO0, IO1, IO2, IO3. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The Quad Enable bit (QE) of Status Register must be set to enable for the Quad I/O Fast read instruction, as shown in ***Figure 53-Figure 60.***

Quad I/O Fast Read with "Continuous Read Mode"

The Quad I/O Fast Read instruction can further reduce instruction overhead through setting the "Continuous Read Mode" bits (M7-0) after the input Address bits (A23-0), If the "Continuous Read Mode" bits (M5-4)= (1,0), then the next Fast Read Quad I/O instruction(after /CS is raised and then lowered) does not require the EBH instruction code. If the "Continuous Read Mode" bits M5-4 do not equal to (1,0), the next instruction requires the first EBH instruction code, thus returning to normal operation. A "Continuous Read Mode" Reset instruction can also be used to reset (M5-4) before issuing normal instruction.

Figure 53. Quad I/O Fast Read Sequence Diagram (SPI Mode/3-Byte Address Mode; Initial instruction or previous (M5-4≠(1,0)))

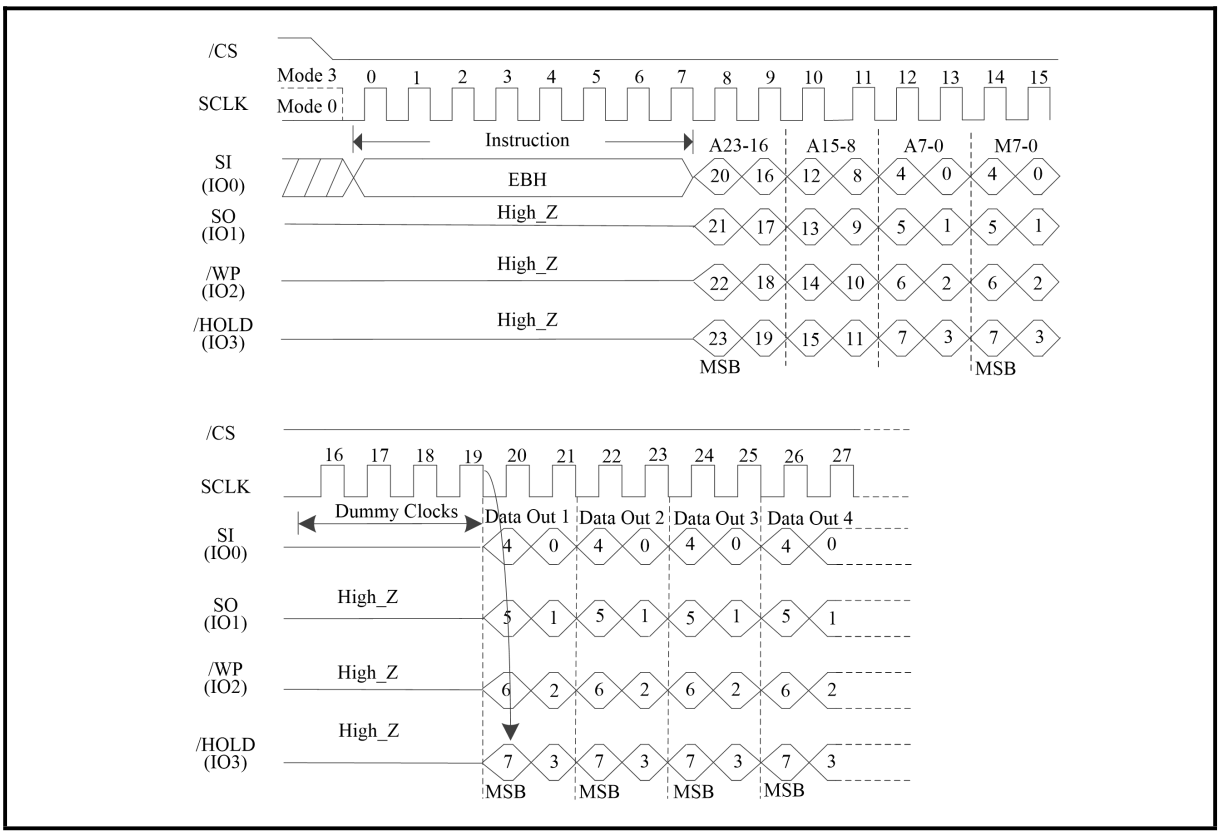


Figure 54. Quad I/O Fast Read Sequence Diagram (SPI Mode/4-Byte Address Mode; Initial instruction or previous (M5-4≠(1,0)))

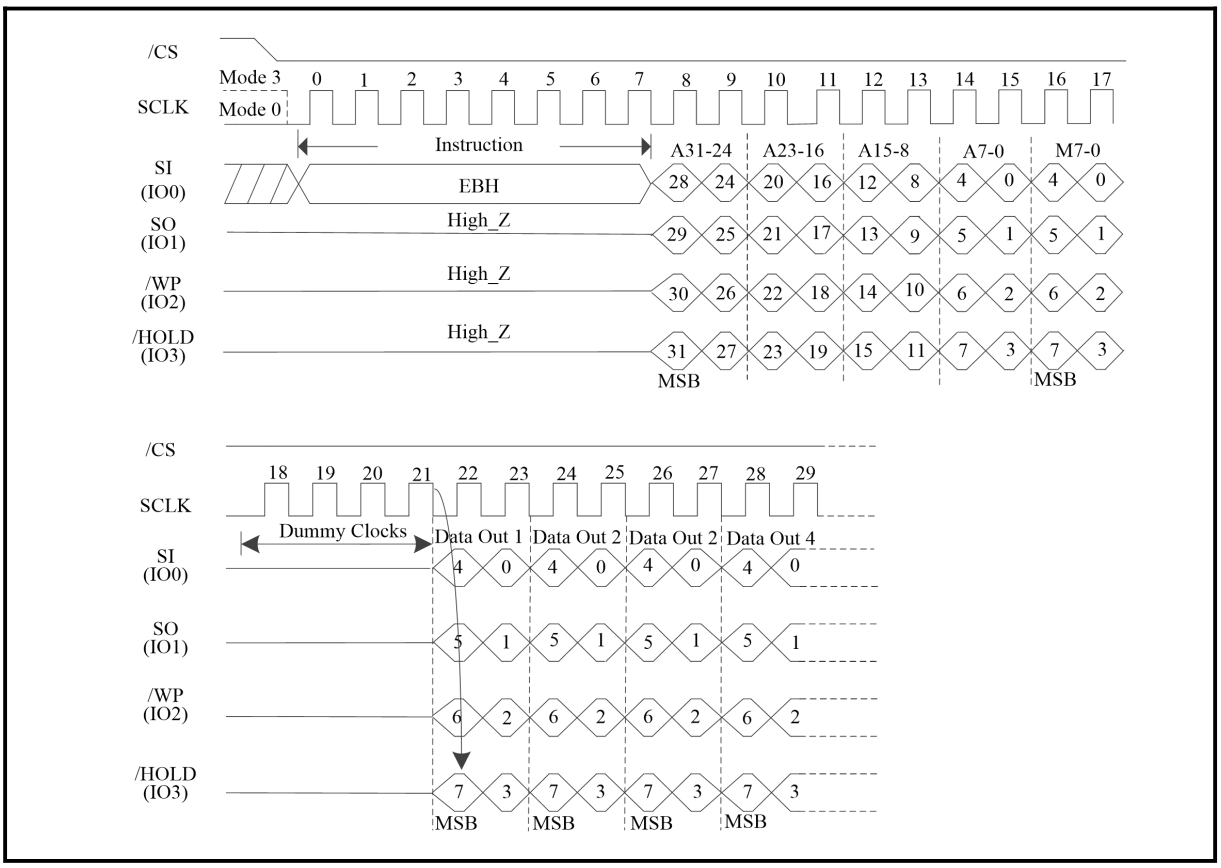


Figure 55. Quad I/O Fast Read Sequence Diagram (SPI Mode/3-Byte Address Mode; Initial instruction or previous (M5-4=(1,0)))

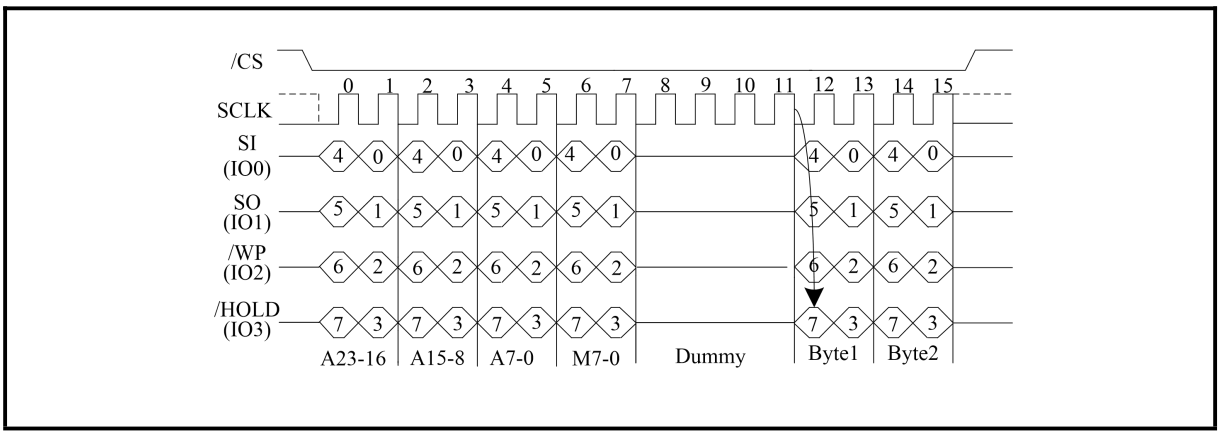
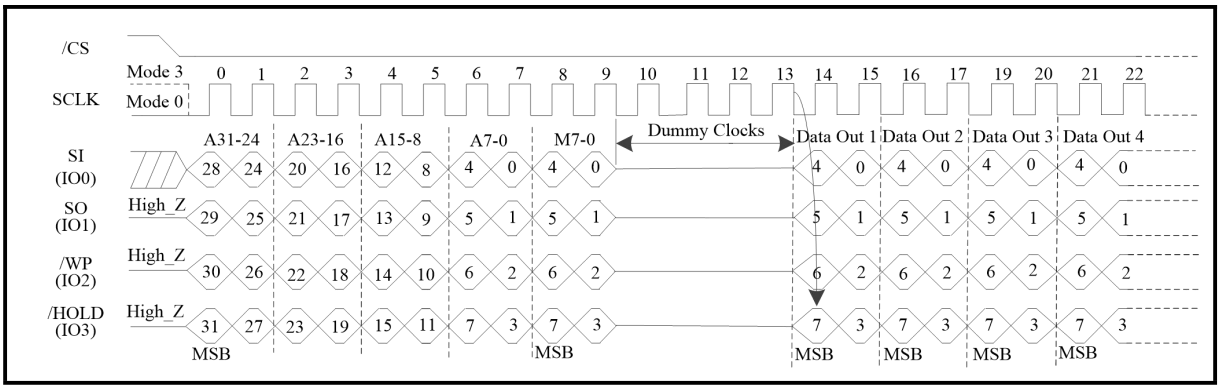


Figure 56. Quad I/O Fast Read Sequence Diagram (SPI Mode/4-Byte Address Mode; Initial instruction or previous (M5-4=(1,0)))



Quad I/O Fast Read with "8/16/32/64-Byte Wrap Around"

The Quad I/O Fast Read instruction can also be used to access a specific portion within a page by issuing a "Set Burst with Wrap" (77H) instruction prior to EBH. The "Set Burst with Wrap" (77H) instruction can either enable or disable the "Wrap Around" feature for the following EBH instructions. When "Wrap Around" is enabled, the data being accessed can be limited to either an 8, 16, 32 or 64-byte section of a 256-byte page. The output data starts at the initial address specified in the instruction, once it reaches the ending boundary of the 8/16/32/64-byte section, the output will wrap around to the beginning boundary automatically until /CS is pulled high to terminate the instruction.

The Burst with Wrap feature allows applications that use cache to quickly fetch a critical address and then fill the cache afterwards within a fixed length (8/16/32/64-byte) of data without issuing multiple read instructions.

The "Set Burst with Wrap" instruction allows three "Wrap Bits", W6-4 to be set. The W4 bit is used to enable or disable the "Wrap Around" operation while W6-5 are used to specify the length of the wrap around section within a page.

Fast Read Quad I/O (EBh) in QPI Mode

The Fast Read Quad I/O instruction is also supported in QPI mode, as shown in ***Figure 57-Figure 60.*** When QPI mode is enabled, the number of dummy clocks is configured by the "Set Read Parameters (C0h)" instruction to accommodate a wide range of applications with different needs for either maximum Fast Read frequency or minimum data access latency. Depending on the Read Parameter Bits P[6:4] setting, the number of dummy clocks can be configured as either 4-18. The default number of dummy clocks upon power up or after a Reset instruction is 4. In QPI mode, the "Continuous Read Mode" bits M7-0 are also considered as dummy clocks. In the default setting, the data output will follow the Continuous Read Mode bits immediately.

"Continuous Read Mode" feature is also available in QPI mode for Fast Read Quad I/O instruction. Please refer to the description on previous pages.

"Wrap Around" feature is not available in QPI mode for Fast Read Quad I/O instruction. To perform a read operation with fixed data length wrap around in QPI mode, a dedicated "Burst Read with Wrap" (0Ch) instruction must be used.

Figure 57. Quad I/O Fast Read Sequence Diagram (QPI Mode/3-Byte Address Mode; Initial instruction or previous (M5-4≠(1,0)))

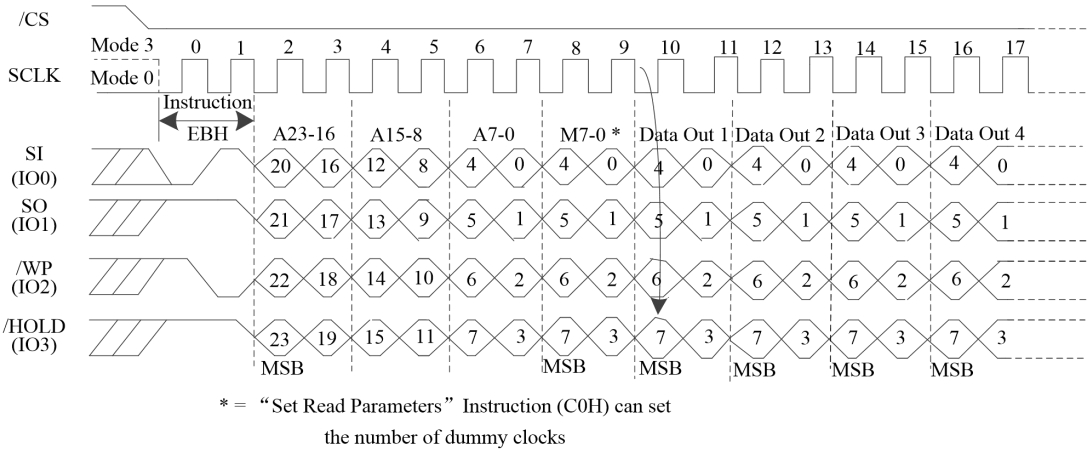


Figure 58. Quad I/O Fast Read Sequence Diagram (QPI Mode/4-Byte Address Mode; Initial instruction or previous (M5-4≠(1,0)))

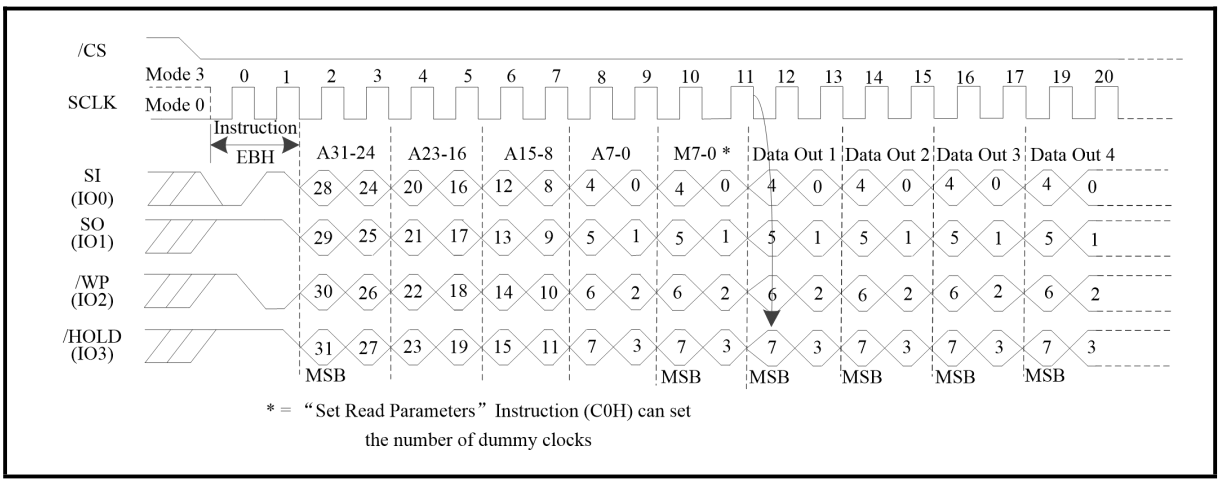


Figure 59. Quad I/O Fast Read Sequence Diagram (QPI Mode/3-Byte Address Mode; Initial instruction or previous (M5-4=(1,0)))

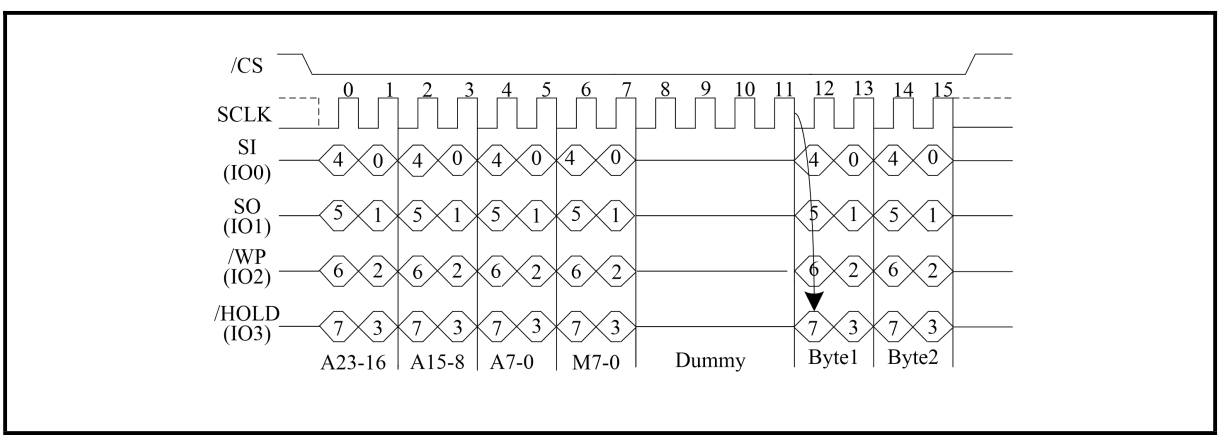
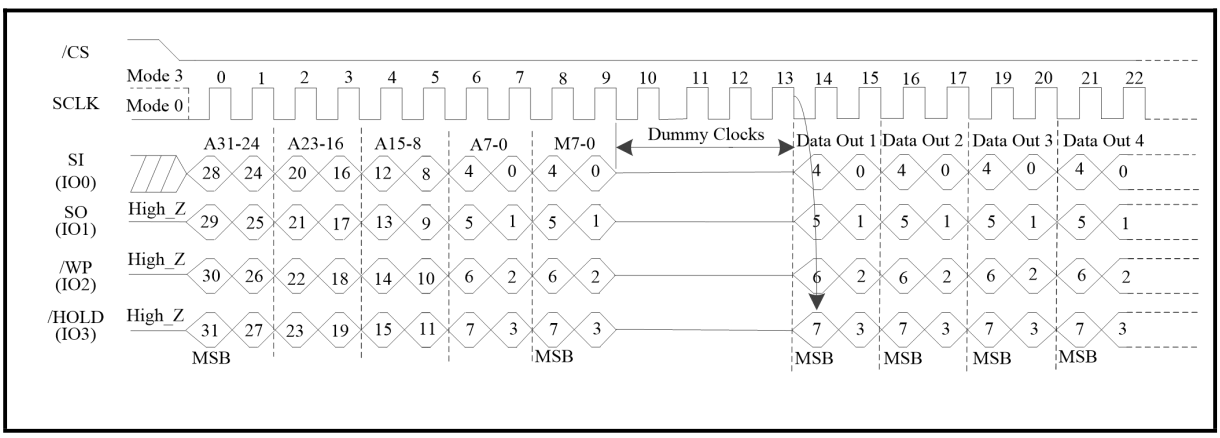


Figure 60. Quad I/O Fast Read Sequence Diagram (QPI Mode/4-Byte Address Mode; Initial instruction or previous (M5-4=(1,0)))



7.2.12 DTR Fast Read Quad I/O(EDH)

The DTR Fast Read Quad I/O (EDh) instruction is similar to the Fast Read Dual I/O (BBh) instruction except that address and data bits are input and output through four pins IO0, IO1, IO2 and IO3 and Dummy clocks (can be configured using DC bits or C0H instruction) are required in SPI mode prior to the data output, as shown in ***Figure 61-Figure 68.*** The Quad Enable bit (QE) of Status Register must be set to enable.

DTR Fast Read Quad I/O with "Continuous Read Mode"

The Fast Read Quad I/O instruction can further reduce instruction overhead through setting the "Continuous Read Mode" bits (M7-0) after the input Address bits (A23/A31-0). The upper nibble of the (M7-4) controls the length of the next Fast Read Quad I/O instruction through the inclusion or exclusion of the first byte instruction code. The lower nibble bits of the (M3-0) are don't care ("x"). However, the IO pins should be high-impedance prior to the falling edge of the first data out clock.

If the "Continuous Read Mode" bits M5-4 = (1,0), then the next Fast Read Quad I/O instruction (after /CS is raised and then lowered) does not require the EDh instruction code. This reduces the instruction sequence by eight clocks and allows the Read address to be immediately entered after /CS is asserted low. If the "Continuous Read Mode" bits M5-4 do not equal to (1,0), the next instruction (after /CS is raised and then lowered) requires the first byte instruction code, thus returning to normal operation.

Figure 61. DTR Fast Read Quad I/O (SPI Mode/3-Byte Address Mode; Initial instruction or previous (M5-4≠(1,0)))

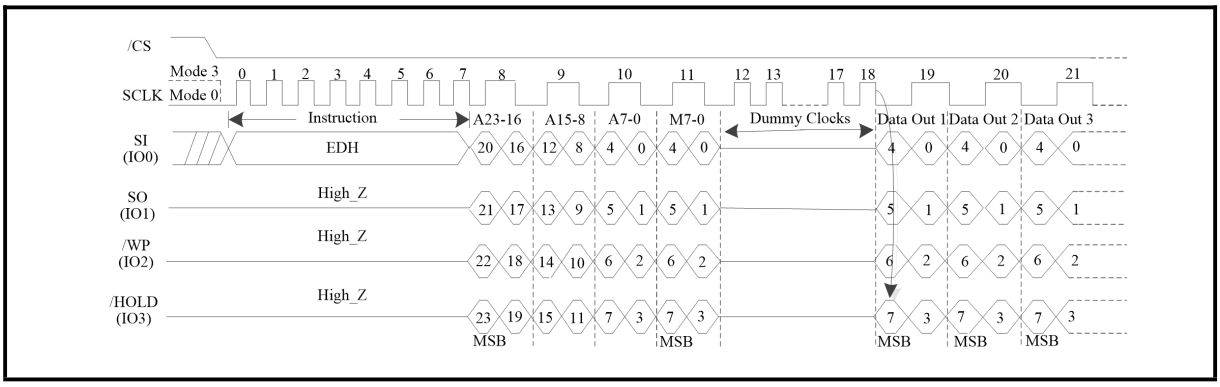


Figure 62. DTR Fast Read Quad I/O (SPI Mode/4-Byte Address Mode; Initial instruction or previous (M5-4≠(1,0)))

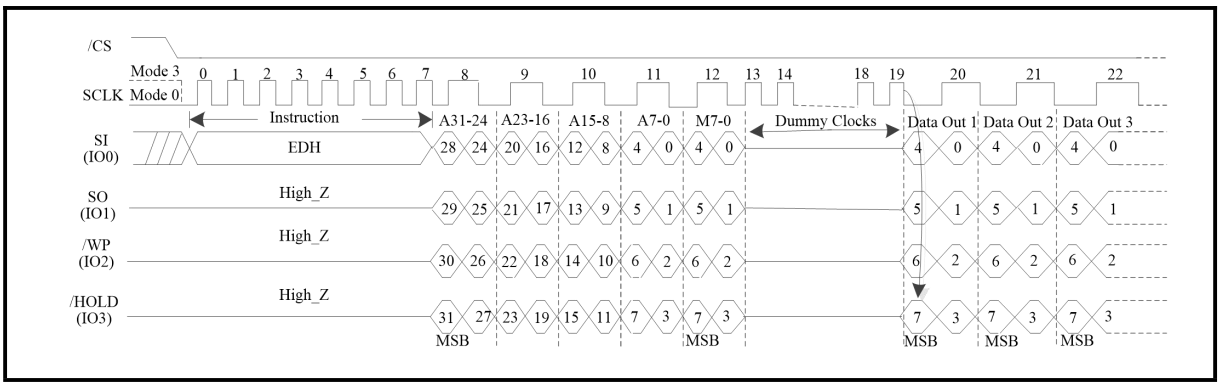


Figure 63. DTR Fast Read Quad I/O (SPI Mode/3-Byte Address Mode; Initial instruction or previous (M5-4=(1,0)))

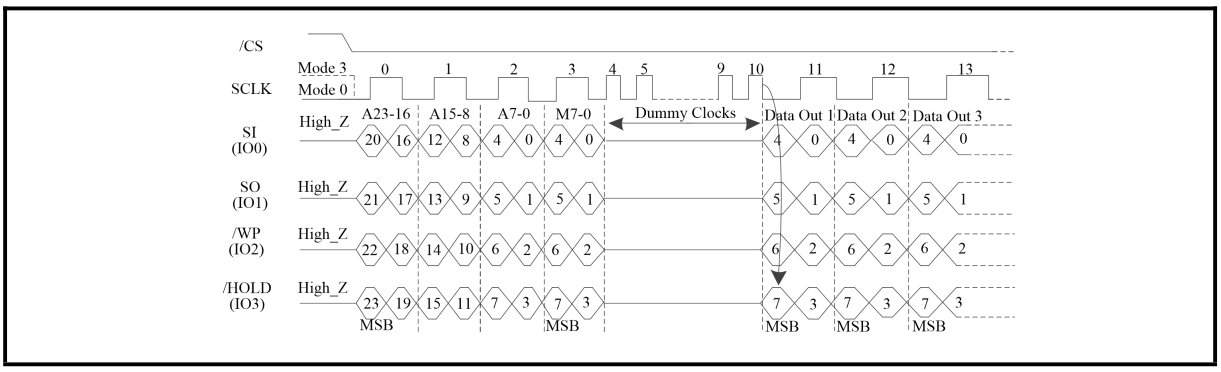
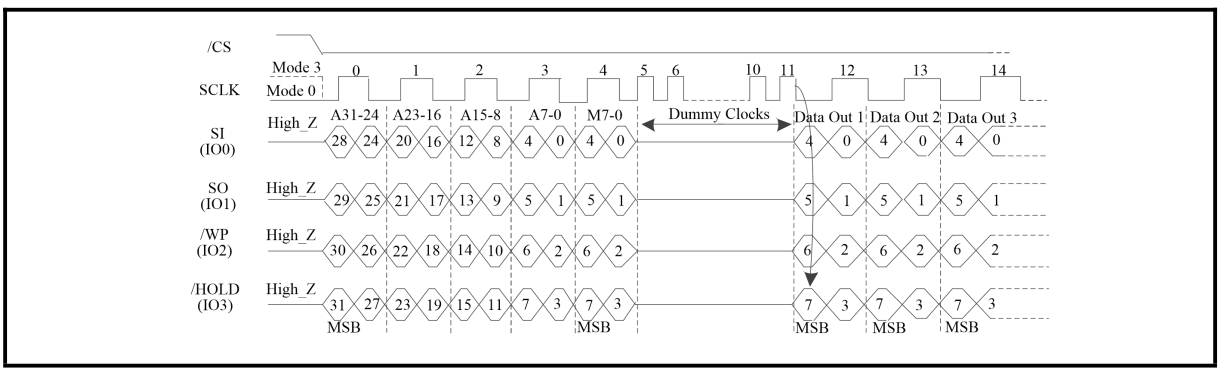


Figure 64. DTR Fast Read Quad I/O (SPI Mode/4-Byte Address Mode; Initial instruction or previous (M5-4=(1,0)))



DTR Fast Read Quad I/O with "8/16/32/64-Byte Wrap Around" in Standard SPI mode

The Fast Read Quad I/O instruction can also be used to access a specific portion within a page by issuing a "Set Burst with Wrap" (77h) instruction prior to EDh. The "Set Burst with Wrap" (77h) instruction can either enable or disable the "Wrap Around" feature for the following EDh instructions. When "Wrap Around" is enabled, the data being accessed can be limited to either an 8, 16, 32 or 64-byte section of a 256-byte page. The output data starts at the initial address specified in the instruction, once it reaches the ending boundary of the 8/16/32/64-byte section, the output will wrap around to the beginning boundary automatically until /CS is pulled high to terminate the instruction.

The Burst with Wrap feature allows applications that use cache to quickly fetch a critical address and then fill the cache afterwards within a fixed length (8/16/32/64-byte) of data without issuing multiple read instructions.

The "Set Burst with Wrap" instruction allows three "Wrap Bits", W6-4 to be set. The W4 bit is used to enable or disable the "Wrap Around" operation while W6-5 are used to specify the length of the wrap around section within a page.

DTR Fast Read Quad I/O (EDh) in QPI Mode

The DTR Fast Read Quad I/O instruction is also supported in QPI mode, as shown in ***Figure 65-Figure 68***. In QPI mode, the "Continuous Read Mode" can further reduce instruction overhead through setting the "Continuous Read Mode" bits (M7-0) after the input Address bits (A23/31-0). Please refer to the description on previous pages. If the "Continuous Read Mode" bits (M5-4)= (1,0), then the next Fast Read Quad I/O instruction(after /CS is raised and then lowered) does not require the EDH instruction code, The instruction sequence is shown in the followed Figure. If the "Continuous Read Mode" bits M5-4 do not equal to (1,0), the next instruction requires the first EDH instruction code, thus returning to normal operation. A "Continuous Read Mode" Reset instruction can also be used to reset (M5-4) before issuing normal instruction.

When QPI mode is enabled, the number of dummy clocks is configured by the "Set Read Parameters (C0h)" instruction to accommodate a wide range of applications with different needs

for either maximum Fast Read frequency or minimum data access latency. Depending on the Read Parameter Bits P[6:4] setting, the number of dummy clocks can be configured as either 4-18. The default number of dummy clocks upon power up or after a Reset instruction is 4. Please note that the number of dummy includes M7-0.

Figure 65. DTR Fast Read Quad I/O (QPI Mode/3-Byte Address Mode; Initial instruction or previous (M5-4≠(1,0)))

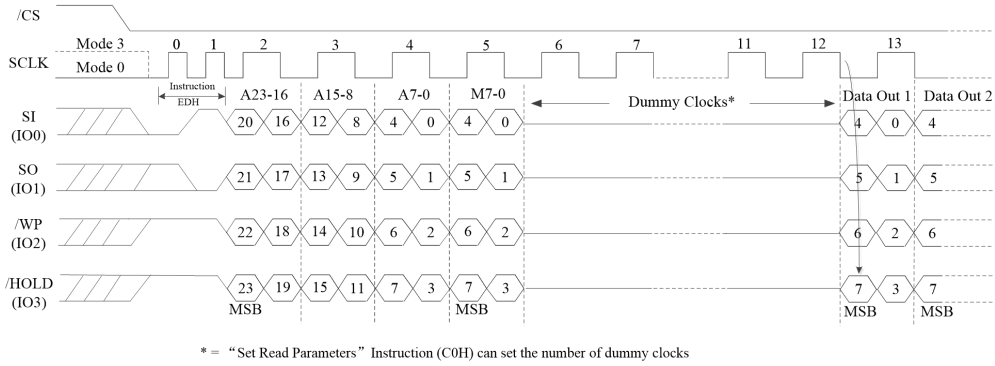


Figure 66. DTR Fast Read Quad I/O (QPI Mode/4-Byte Address Mode; Initial instruction or previous (M5-4≠(1,0)))

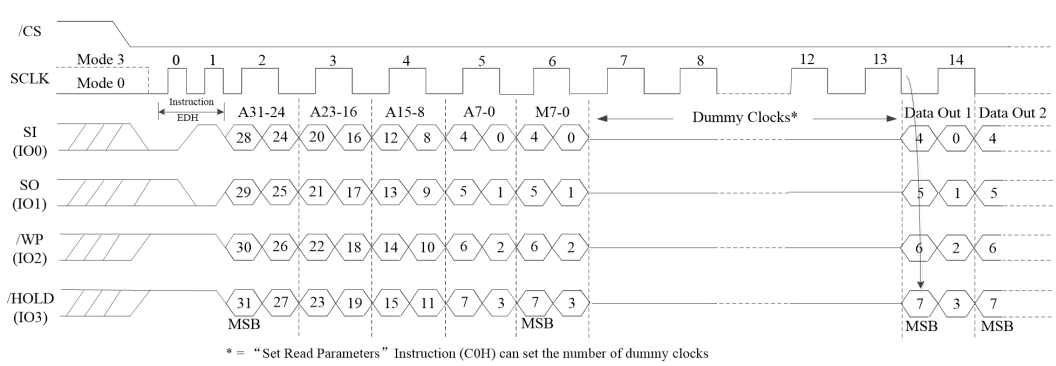


Figure 67. DTR Fast Read Quad I/O (QPI Mode/3-Byte Address Mode; Initial instruction or previous (M5-4=(1,0)))

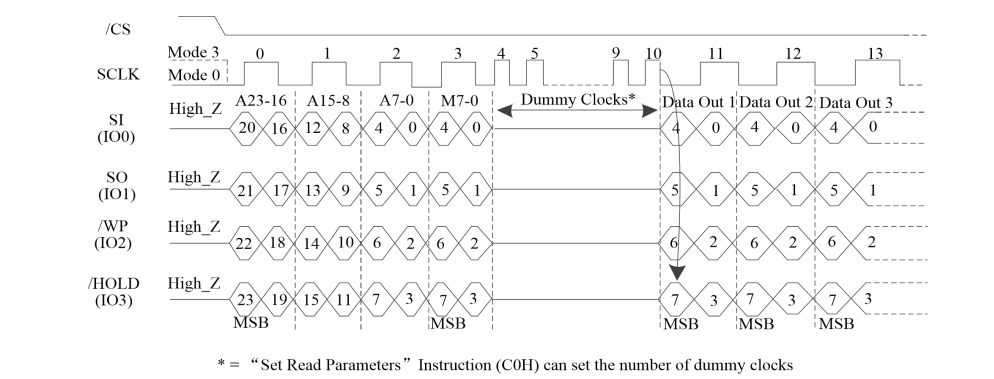
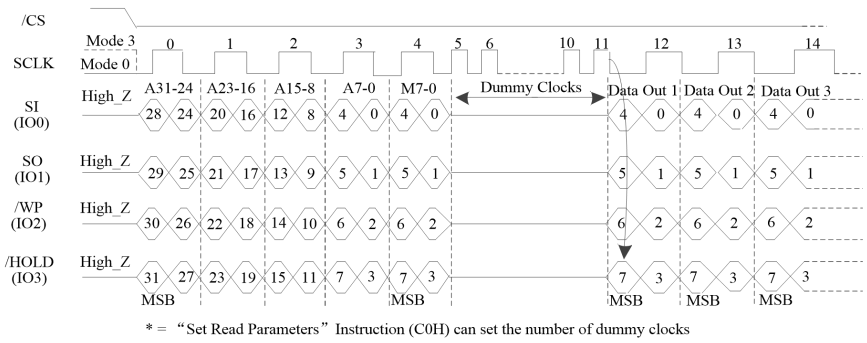


Figure 68. DTR Fast Read Quad I/O (QPI Mode/4-Byte Address Mode; Initial instruction or previous (M5-4=(1,0)))



7.2.13 Fast Read Quad I/O with 4-Byte Address (ECH)

The Fast Read Quad I/O with 4-Byte Address instruction is similar to the Quad I/O Fast Read instruction except that it requires 32-bit address instead of 24-bit address. No matter the device is operating in 3-Byte Address Mode or 4-byte Address Mode, the Fast Read Quad I/O with 4-Byte Address instruction will always require 32-bit address to access the entire 256Mb memory. The Quad Enable bit (QE) of Status Register must be set to enable.

Figure 69. Fast Read Quad I/O with 4-Byte Address (SPI Mode; Initial instruction or previous M5-4≠10)

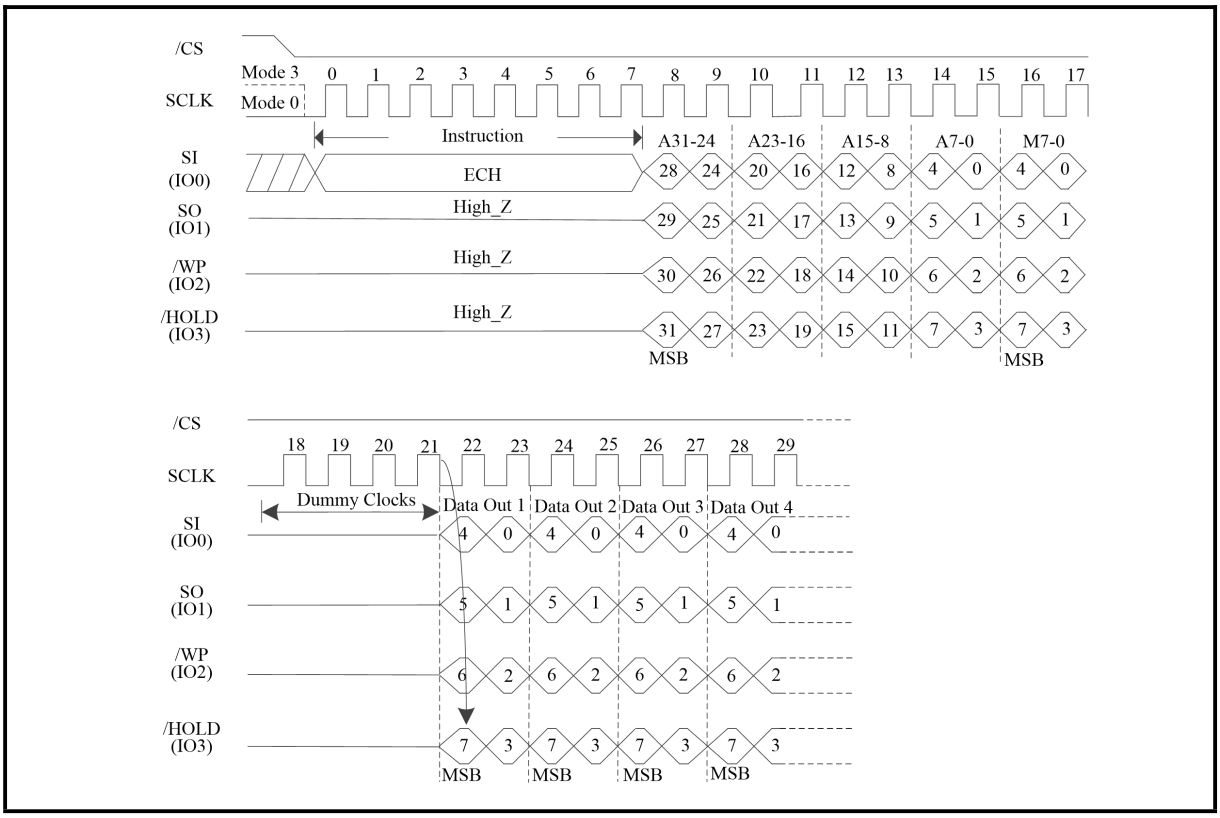
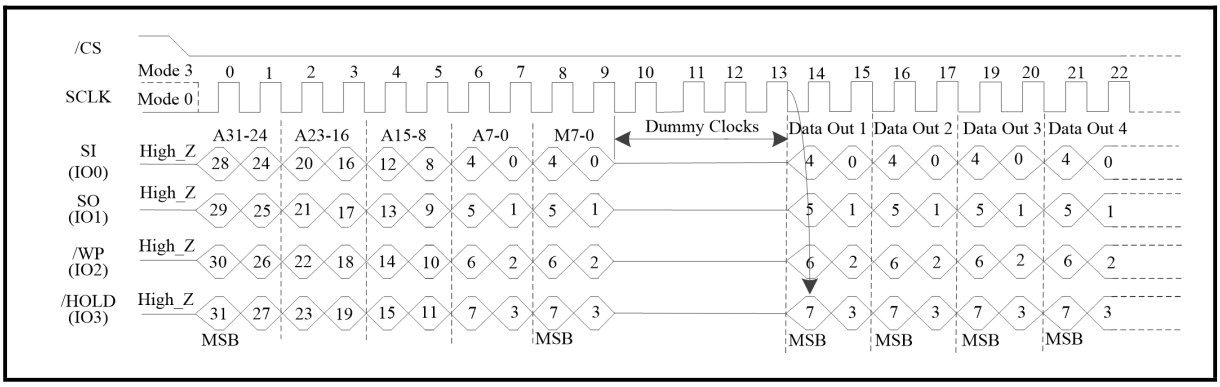


Figure 70. Fast Read Quad I/O with 4-Byte Address (SPI Mode; Initial instruction or previous M5-4=10)



Fast Read Quad I/O with 4-Byte Address with "8/16/32/64-Byte Wrap Around" in Standard SPI mode

The Fast Read Quad I/O with 4-Byte Address instruction can also be used to access a specific portion within a page by issuing a "Set Burst with Wrap" (77h) instruction prior to ECh. The "Set Burst with Wrap" (77h) instruction can either enable or disable the "Wrap Around" feature for the following ECh instructions. When "Wrap Around" is enabled, the data being accessed can be limited to either an 8, 16, 32 or 64-byte section of a 256-byte page. The output data starts at the initial address specified in the instruction, once it reaches the ending boundary of the 8/16/32/64-byte section, the output will wrap around to the beginning boundary automatically until /CS is pulled high to terminate the instruction.

The Burst with Wrap feature allows applications that use cache to quickly fetch a critical address and then fill the cache afterwards within a fixed length (8/16/32/64-byte) of data without issuing multiple read instructions.

The “Set Burst with Wrap” instruction allows three “Wrap Bits”, W6-4 to be set. The W4 bit is used to enable or disable the “Wrap Around” operation while W6-5 are used to specify the length of the wrap around section within a page.

Fast Read Quad I/O with 4-Byte Address (ECh) in QPI Mode

The Fast Read Quad I/O with 4-Byte Address instruction is also supported in QPI mode, as shown in ***Figure 71-Figure 72***. When QPI mode is enabled, the number of dummy clocks is configured by the “Set Read Parameters (C0h)” instruction to accommodate a wide range of applications with different needs for either maximum Fast Read frequency or minimum data access latency. Depending on the Read Parameter Bits P[6:4] setting, the number of dummy clocks can be configured as either 4-18. The default number of dummy clocks upon power up or after a Reset instruction is 4. In QPI mode, the “Continuous Read Mode” bits M7-0 are also considered as dummy clocks. In the default setting, the data output will follow the Continuous Read Mode bits immediately.

“Continuous Read Mode” feature is also available in QPI mode for Fast Read Quad I/O with 4-Byte Address instruction. Please refer to the description on previous pages.

“Wrap Around” feature is not available in QPI mode for Fast Read Quad I/O with 4-Byte Address instruction. To perform a read operation with fixed data length wrap around in QPI mode, a dedicated “Burst Read with Wrap” (0Ch) instruction must be used.

Figure 71. Fast Read Quad I/O with 4-Byte Address (QPI Mode; Initial instruction or previous M5-4≠10)

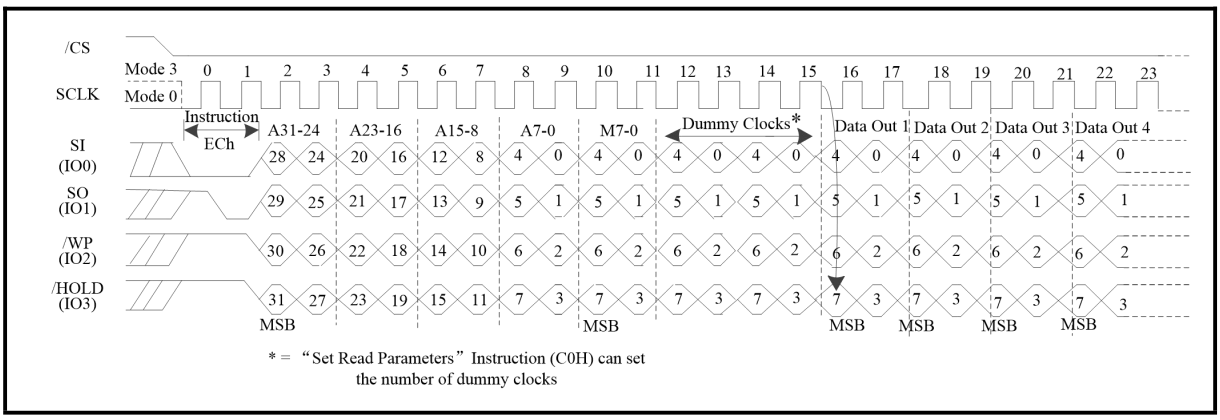
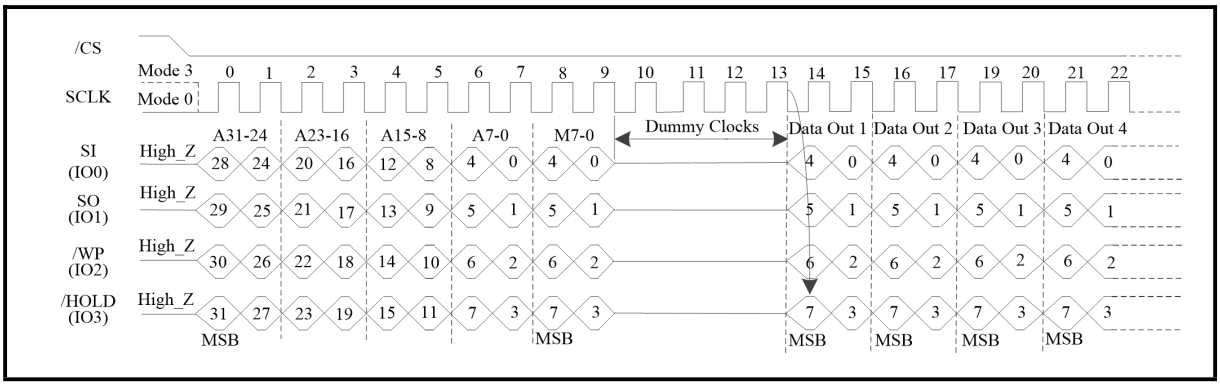


Figure 72. Fast Read Quad I/O with 4-Byte Address (QPI Mode; Initial instruction or previous M5-4=10)



7.2.14 DTR Quad I/O Fast Read with 4- Byte Address (EEH)

The DTR Quad I/O Fast Read with 4- Byte Address (EEh) instruction is similar to the Fast Read Dual I/O (BBh) instruction except that address and data bits are input and output through four pins IO0, IO1, IO2 and IO3 and Dummy clocks (can be configured using DC bits or C0H instruction) are required in SPI mode prior to the data output, as shown in ***Figure 73-Figure 76***. The Quad Enable bit (QE) of Status Register must be set to enable.

DTR Fast Read Quad I/O with "Continuous Read Mode"

The DTR Quad I/O Fast Read with 4-Byte Address instruction can further reduce instruction overhead through setting the "Continuous Read Mode" bits (M7-0) after the input Address bits (A31-0) The upper nibble of the (M7-4) controls the length of the next Fast Read Quad I/O instruction through the inclusion or exclusion of the first byte instruction code. The lower nibble bits of the (M3-0) are don't care ("x"). However, the IO pins should be high-impedance prior to the falling edge of the first data out clock.

If the "Continuous Read Mode" bits M5-4 = (1,0), then the next DTR Quad I/O Fast Read with 4- Byte Address instruction (after /CS is raised and then lowered) does not require the EEh instruction code, as shown in ***Figure 74***. This reduces the instruction sequence by eight clocks and allows the Read address to be immediately entered after /CS is asserted low. If the "Continuous Read Mode" bits M5-4 do not equal to (1,0), the next instruction (after /CS is raised and then lowered) requires the first byte instruction code, thus returning to normal operation.

When QPI mode is enabled, the number of dummy clocks is configured by the "Set Read Parameters (C0h)" instruction to accommodate a wide range of applications with different needs for either maximum Fast Read frequency or minimum data access latency. Depending on the Read Parameter Bits P[6:4] setting, the number of dummy clocks can be configured as either 4-18. The default number of dummy clocks upon power up or after a Reset instruction is 4. Please note that the number of dummy includes M7-0.

Figure 73. DTR Quad I/O Fast Read with 4- Byte Address (SPI Mode; Initial instruction or previous M5-4≠10)

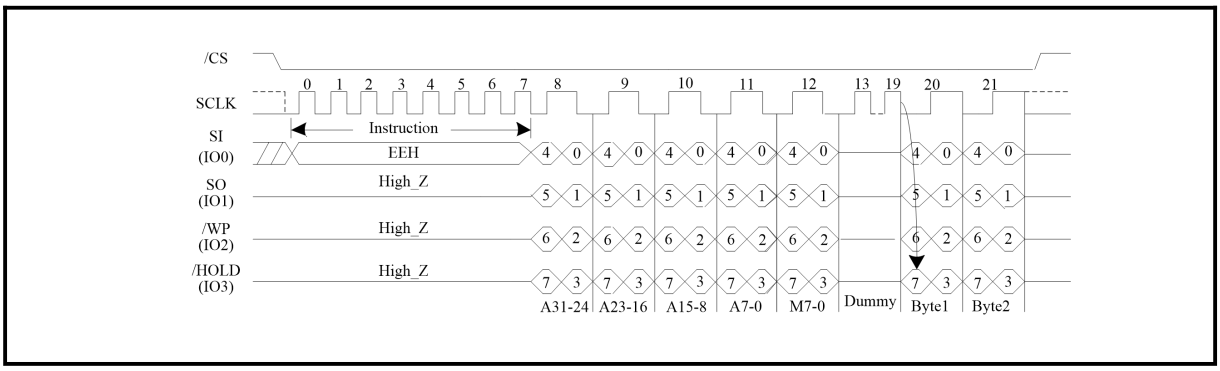
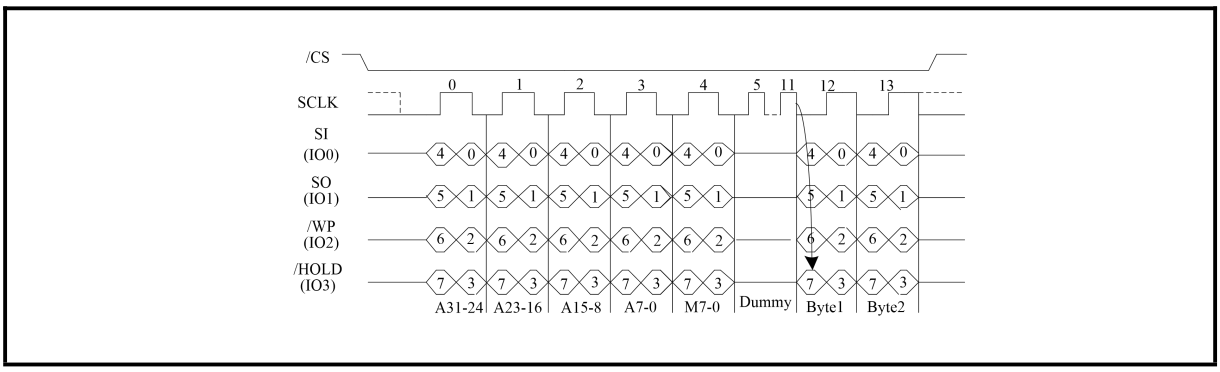


Figure 74. DTR Quad I/O Fast Read with 4- Byte Address (SPI Mode; Initial instruction or previous M5-4=10)



DTR Quad I/O Fast Read with 4- Byte Address with "8/16/32/64-Byte Wrap Around" in Standard SPI mode

The DTR Quad I/O Fast Read with 4- Byte Address instruction can also be used to access a specific portion within a page by issuing a "Set Burst with Wrap" (77h) instruction prior to EEh. The "Set Burst with Wrap" (77h) instruction can either enable or disable the "Wrap Around" feature for the following EEh instructions. When "Wrap Around" is enabled, the data being accessed can be limited to either an 8, 16, 32 or 64-byte section of a 256-byte page. The output data starts at the initial address specified in the instruction, once it reaches the ending boundary of the 8/16/32/64-byte section, the output will wrap around to the beginning boundary automatically until /CS is pulled high to terminate the instruction.

The Burst with Wrap feature allows applications that use cache to quickly fetch a critical address and then fill the cache afterwards within a fixed length (8/16/32/64-byte) of data without issuing multiple read instructions.

The "Set Burst with Wrap" instruction allows three "Wrap Bits", W6-4 to be set. The W4 bit is used to enable or disable the "Wrap Around" operation while W6-5 are used to specify the length of the wrap around section within a page.

DTR Quad I/O Fast Read with 4- Byte Address (EEh) in QPI Mode

"Continuous Read Mode" feature is also available in QPI mode for DTR Quad I/O Fast Read with 4- Byte Address instruction.

"Wrap Around" feature is not available in QPI mode for Fast Read Quad I/O instruction. To perform a read operation with fixed data length wrap around in QPI mode, a dedicated "Burst Read with Wrap" (0Ch) instruction must be used.

Figure 75. DTR Quad I/O Fast Read with 4- Byte Address (QPI Mode; Initial instruction or previous M5-4≠10)

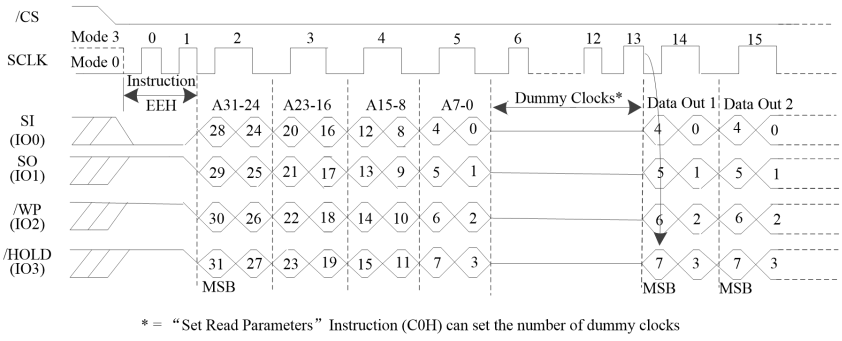
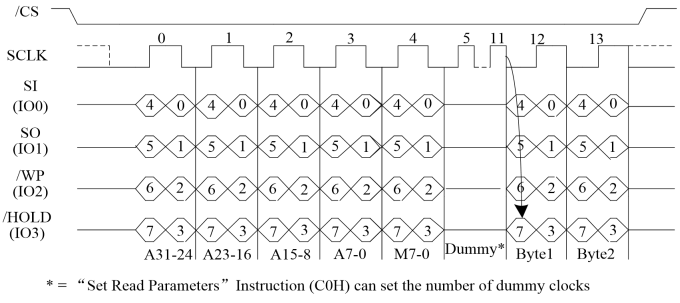


Figure 76. DTR Quad I/O Fast Read with 4- Byte Address (QPI Mode; Initial instruction or previous M5-4=10)



7.2.15 Set Burst with Wrap (77H)

See ***Figure 77-Figure 78,*** The Set Burst with Wrap instruction is used in conjunction with “EBH”, “EDH”, “ECH”, “EEH” and “E7H” instructions to access a fixed length of 8/16/32/64-byte section within a 256-byte page, in standard SPI mode.

The Set Burst with Wrap instruction sequence:/CS goes low ->Send Set Burst with Wrap instruction ->Send24 Dummy bits ->Send 8 bits” Wrap bits”->/CS goes high.

If W6-4 is set by a Set Burst with Wrap instruction, all the following “EBH”, “EDH”, “ECH”, “EEH” and “E7H” instructions will use the W6-4 setting to access the 8/16/32/64-byte section within any page. To exit the “Wrap Around” function and return to normal read operation, another Set Burst with Wrap instruction should be issued to set W4=1. The default value of W4 upon power on is 1.

W6 , W5	W4 = 0		W4 =1 (DEFAULT)	
	Wrap Around	Wrap Length	Wrap Around	Wrap Length
0 0	Yes	8-byte	No	N/A
0 1	Yes	16-byte	No	N/A
1 0	Yes	32-byte	No	N/A
1 1	Yes	64-byte	No	N/A

Figure 77. Set Burst with Wrap Sequence Diagram (SPI Mode only/3-Byte Address Mode)

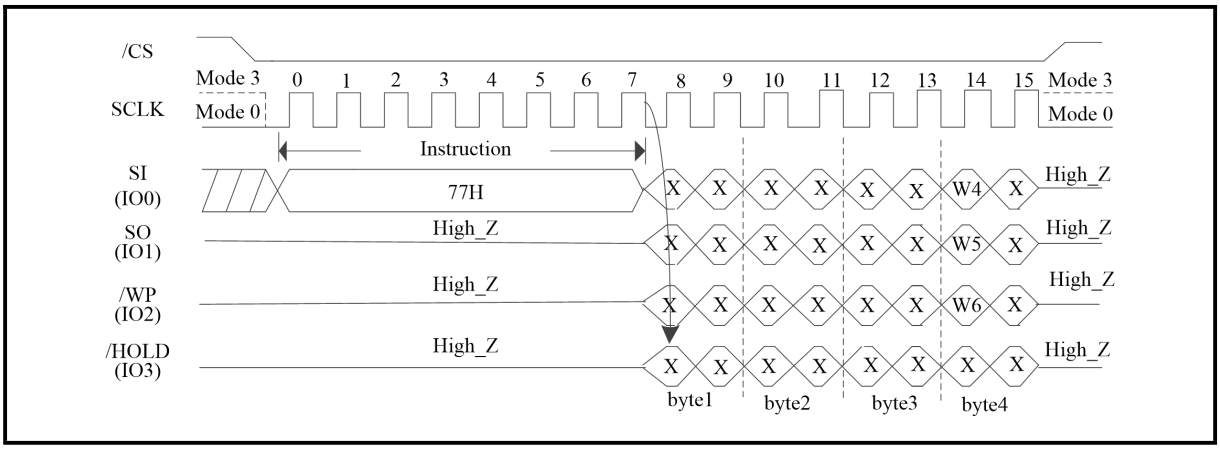
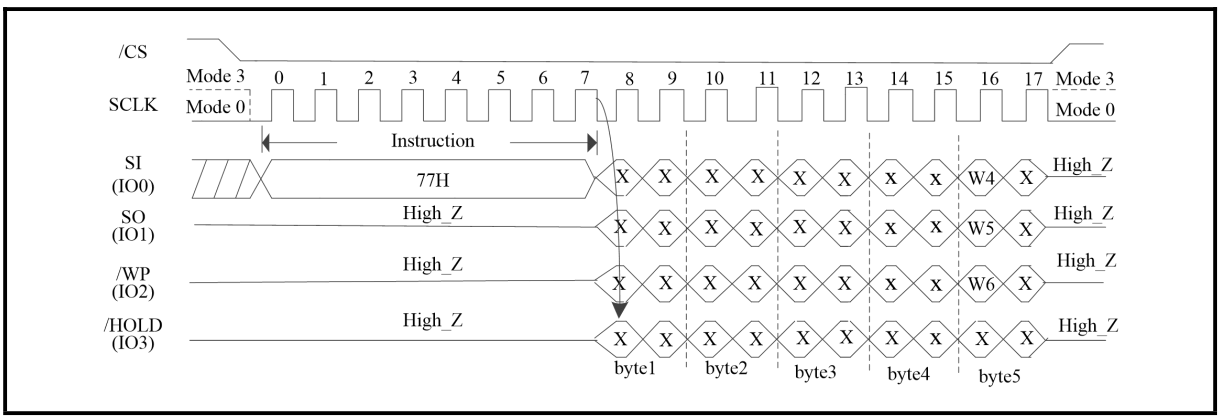


Figure 78. Set Burst with Wrap Sequence Diagram (SPI Mode only/4-Byte Address Mode)



7.2.16 Set Read Parameters (C0h)

In QPI mode, to accommodate a wide range of applications with different needs for either maximum read frequency or minimum data access latency, “Set Read Parameters (C0h)” instruction can be used to configure the number of dummy clocks for “0BH”, “EBH”, “ECH”, “0CH” “EDH”, “EEH”, “0EH”, “4BH”, “48H” and “5AH” instructions, as shown in ***Table 14***, and to configure the number of bytes of “Wrap Length” for the “0CH” and “0EH” instruction.

Table 14. Instructions that configurable dummy number

Mode	Instruction	
QPI	Fast Read	0Bh
	Fast Read Quad I/O	EBh
	Fast Read Quad I/O with 4-Byte Address	ECh
	Burst Read with Wrap	0Ch
	DTR Fast Read Quad I/O	EDh
	DTR Quad I/O Fast Read with 4- Byte Address	EEh
	DTR Burst Read with Wrap	0Eh
	Read Unique ID Number	4Bh
	Read Security Registers	48h
	Read Serial Flash Discoverable Parameter	5Ah

In Standard SPI mode, the “Set Read Parameters (C0h)” instruction is not accepted. The dummy clocks for various Fast Read instructions in Standard/Dual/Quad SPI mode are fixed, please refer to the Instruction ***Table 12*** for details. The “Wrap Length” is set by W5-4 bit in the “Set Burst with Wrap (77h)” instruction. This setting will remain unchanged when the device is switched from Standard SPI mode to QPI mode.

The default “Wrap Length” after a power up or a Reset instruction is 8 bytes, the default number of dummy clocks is 4 (non-DTR) or 6 (DTR). The number of dummy clocks is only programmable for “0BH”, “EBH”, “ECH”, “0CH”, “EDH”, “EEH”, “0EH”, “4BH”, “48H” and “5AH” instructions in the QPI mode. Whenever the device is switched from SPI mode to QPI mode, the number of dummy clocks should be set again, prior to any “0BH”, “EBH”, “ECH”, “0CH”, “EDH”, “EEH”, “0EH”, “48H” and “5AH” instructions.

Table 15 shows the configuration of dummy numbers for non-DTR instructions (“0BH”, “EBH”, “ECH”, “0CH””, “48H” and “5AH”), and ***Table 16*** shows the configuration of dummy numbers for DTR instructions (“EDH”, “EEH”, “0EH”).

Figure 79. Burst Read with Wrap (QPI Mode only)

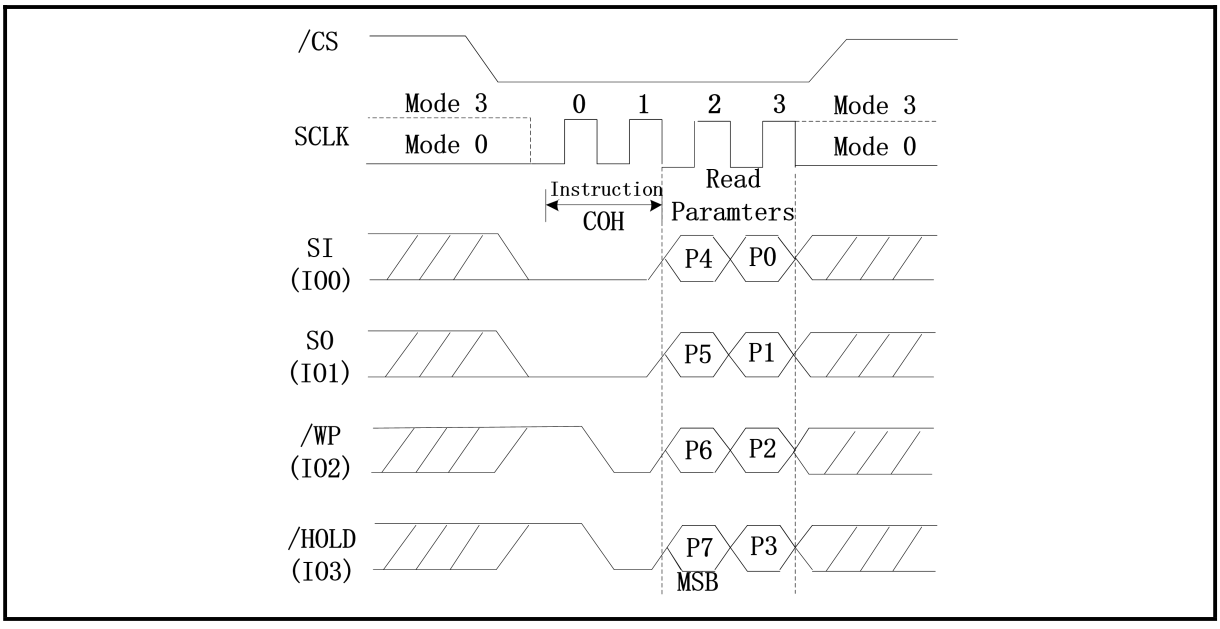


Table 15-1. Configuration of the number of dummies for non-DTR instructions (-40C ~ +85C)

P6 – P4	DUMMY CLOCKS	MAXIMUM READ FREQ. (VCC=2.7V~2.9V)	MAXIMUM READ FREQ. (VCC=3.0V~3.6V)
0 0 0	4	72 MHz	80 MHz
0 0 1	6	96 MHz	108 MHz
0 1 0	8	108 MHz	120 MHz
0 1 1	10	133 MHz	150 MHz
1 0 0	12	133 MHz	150 MHz
1 0 1	14	133 MHz	150 MHz
1 1 0	16	133 MHz	150 MHz
1 1 1	18	133 MHz	150 MHz

P1 – P0	WRAP LENGTH
0 0	8-byte
0 1	16-byte
1 0	32-byte
1 1	64-byte

Table 15-2. Configuration of the number of dummies for non-DTR instructions (-40C ~ +105C)

P6 – P4	DUMMY CLOCKS	MAXIMUM READ FREQ. (VCC=2.7V~2.9V)	MAXIMUM READ FREQ. (VCC=3.0V~3.6V)
0 0 0	4	72 MHz	80 MHz
0 0 1	6	96 MHz	96 MHz
0 1 0	8	108 MHz	120 MHz
0 1 1	10	120 MHz	133 MHz
1 0 0	12	133 MHz	150 MHz
1 0 1	14	133 MHz	150 MHz
1 1 0	16	133 MHz	150 MHz
1 1 1	18	133 MHz	150 MHz

P1 – P0	WRAP LENGTH
0 0	8-byte
0 1	16-byte
1 0	32-byte
1 1	64-byte

Table 15-3. Configuration of the number of dummies for non-DTR instructions (-40C ~ +125C)

P6 – P4	DUMMY CLOCKS	MAXIMUM READ FREQ. (VCC=2.7V~2.9V)	MAXIMUM READ FREQ. (VCC=3.0V~3.6V)
0 0 0	4	72 MHz	72 MHz
0 0 1	6	96 MHz	96 MHz
0 1 0	8	108 MHz	120 MHz
0 1 1	10	120 MHz	133 MHz
1 0 0	12	133 MHz	150 MHz
1 0 1	14	133 MHz	150 MHz
1 1 0	16	133 MHz	150 MHz
1 1 1	18	133 MHz	150 MHz

P1 – P0	WRAP LENGTH
0 0	8-byte
0 1	16-byte
1 0	32-byte
1 1	64-byte

Table 16-1. Configuration of the number of dummies for DTR instructions (-40C ~ +85C)

P6 – P4	DUMMY CLOCKS	MAXIMUM READ FREQ. (VCC=2.7V~2.9V)	MAXIMUM READ FREQ. (VCC=3.0V~3.6V)
0 0 0	6	72 MHz	84 MHz
0 0 1	8	100 MHz	100 MHz
0 1 0	10	100 MHz	100 MHz
0 1 1	12	100 MHz	100 MHz
1 0 0	14	100 MHz	100 MHz
1 0 1	16	100 MHz	100 MHz
1 1 0	18	100 MHz	100 MHz
1 1 1	20	100 MHz	100 MHz

P1 – P0	WRAP LENGTH
0 0	8-byte
0 1	16-byte
1 0	32-byte
1 1	64-byte

Table 16-2. Configuration of the number of dummies for DTR instructions (-40C ~ +105C)

P6 – P4	DUMMY CLOCKS	MAXIMUM READ FREQ. (VCC=2.7V~2.9V)	MAXIMUM READ FREQ. (VCC=3.0V~3.6V)
0 0 0	6	72 MHz	84 MHz
0 0 1	8	100 MHz	100 MHz
0 1 0	10	100 MHz	100 MHz
0 1 1	12	100 MHz	100 MHz
1 0 0	14	100 MHz	100 MHz
1 0 1	16	100 MHz	100 MHz
1 1 0	18	100 MHz	100 MHz
1 1 1	20	100 MHz	100 MHz

P1 – P0	WRAP LENGTH
0 0	8-byte
0 1	16-byte
1 0	32-byte
1 1	64-byte

Table 16-3. Configuration of the number of dummies for DTR instructions (-40C ~ +125C)

P6 – P4	DUMMY CLOCKS	MAXIMUM READ FREQ. (VCC=2.7V~2.9V)	MAXIMUM READ FREQ. (VCC=3.0V~3.6V)
0 0 0	6	72 MHz	84 MHz
0 0 1	8	100 MHz	100 MHz
0 1 0	10	100 MHz	100 MHz
0 1 1	12	100 MHz	100 MHz
1 0 0	14	100 MHz	100 MHz
1 0 1	16	100 MHz	100 MHz
1 1 0	18	100 MHz	100 MHz
1 1 1	20	100 MHz	100 MHz

P1 – P0	WRAP LENGTH
0 0	8-byte
0 1	16-byte
1 0	32-byte
1 1	64-byte

7.2.17 Burst Read with Wrap (0CH)

The “Burst Read with Wrap (0Ch)” instruction provides an alternative way to perform the read operation with “Wrap Around” in QPI mode. The instruction is similar to the “Fast Read (0Bh)” instruction in QPI mode, except the addressing of the read operation will “Wrap Around” to the beginning boundary of the “Wrap Length” once the ending boundary is reached.

The “Wrap Length” and the number of dummy clocks can be configured by the “Set Read Parameters (C0h)” instruction

Figure 80. Burst Read with Wrap (QPI Mode only/3-Byte Address Mode)

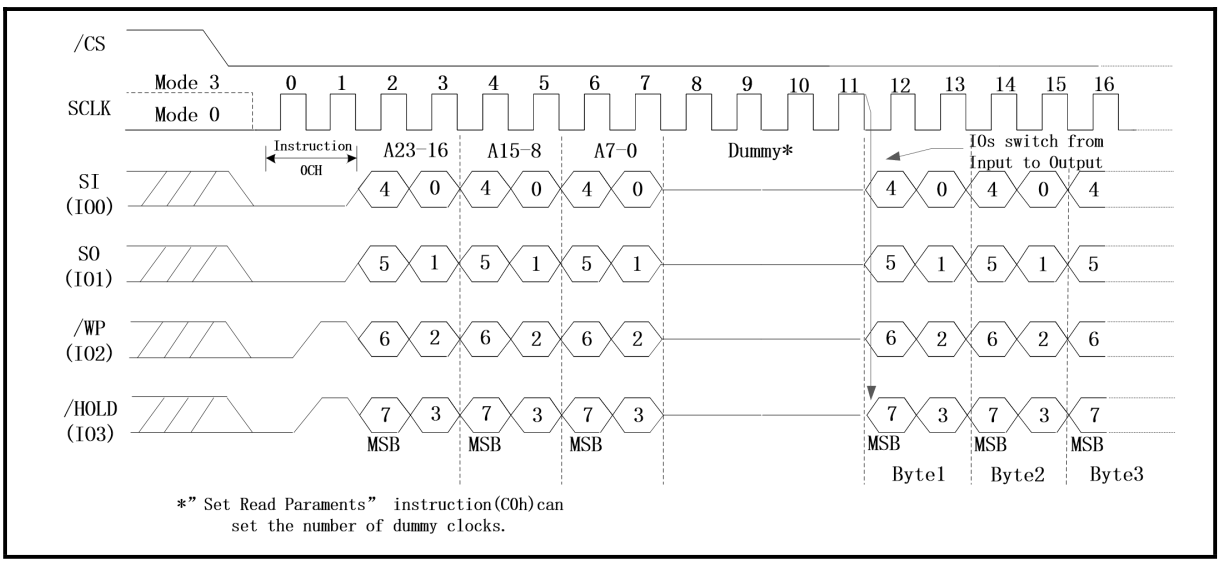
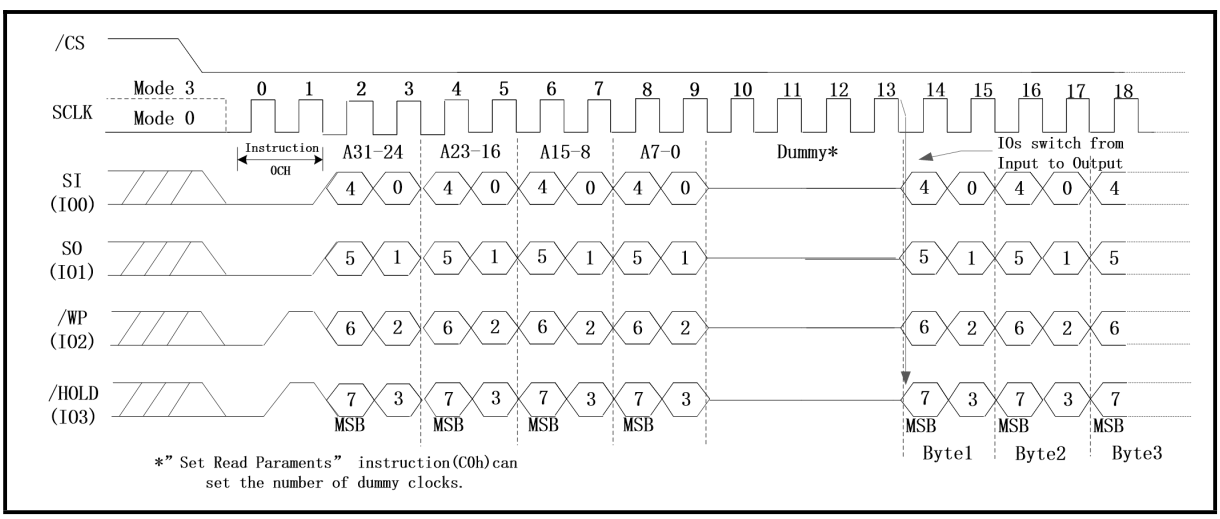


Figure 81. Burst Read with Wrap (QPI Mode only/4-Byte Address Mode)



7.2.18 DTR Burst Read with Wrap (0EH)

The “DTR Burst Read with Wrap (0Eh)” instruction provides an alternative way to perform the read operation with “Wrap Around” in QPI mode. The instruction is similar to the “Fast Read (0Bh)” instruction in QPI mode, except the addressing of the read operation will “Wrap Around” to the beginning boundary of the “Wrap Length” once the ending boundary is reached.

The “Wrap Length” can be configured by the “Set Read Parameters (C0h)” instruction.

The number of dummy clocks is configured by the “Set Read Parameters (C0h)” instruction to accommodate a wide range of applications with different needs for either maximum Fast Read frequency or minimum data access latency. Depending on the Read Parameter Bits P[6:4] setting, the number of dummy clocks can be configured as either 6-20.

Figure 82. DTR Burst Read with Wrap (QPI Mode only/3-Byte Address Mode)

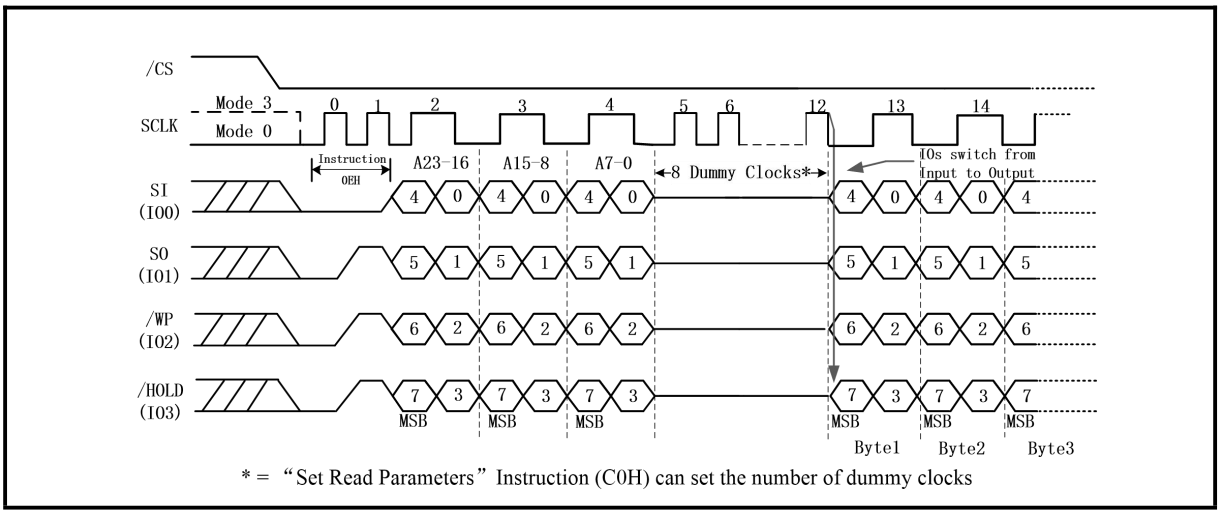
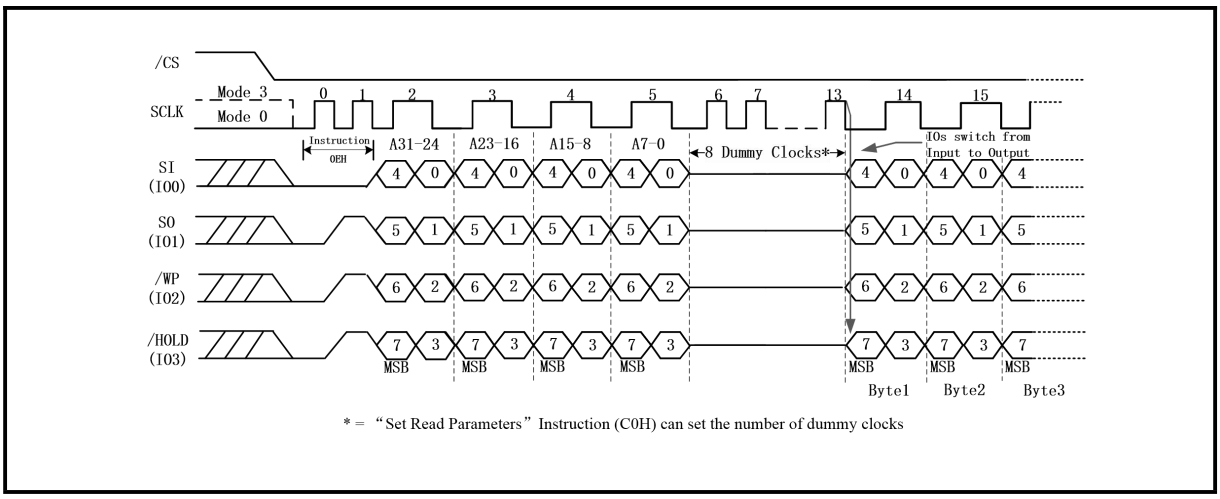


Figure 83. DTR Burst Read with Wrap (QPI Mode only/4-Byte Address Mode)



7.3 ID and Security Instructions

7.3.1 Read Manufacture ID/ Device ID (90H)

See ***Figure 84-Figure 85***, The Read Manufacturer/Device ID instruction is an alternative to the Release from Power-Down/Device ID instruction that provides both the JEDEC assigned Manufacturer ID and the specific Device ID.

The instruction is initiated by driving the /CS pin low and shifting the instruction code “90H” followed by a 24-bit address (A23-A0) of 000000H, regardless of the 3-byte or 4-byte Address Mode.

Figure 84. Read Manufacture ID/ Device ID Sequence Diagram (SPI Mode)

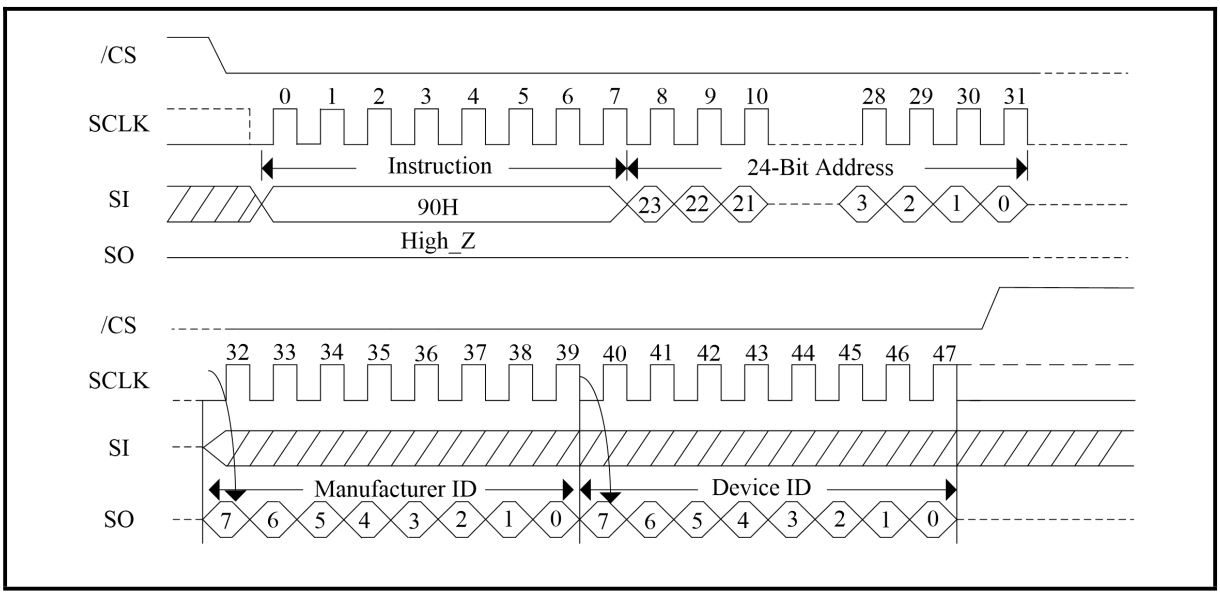
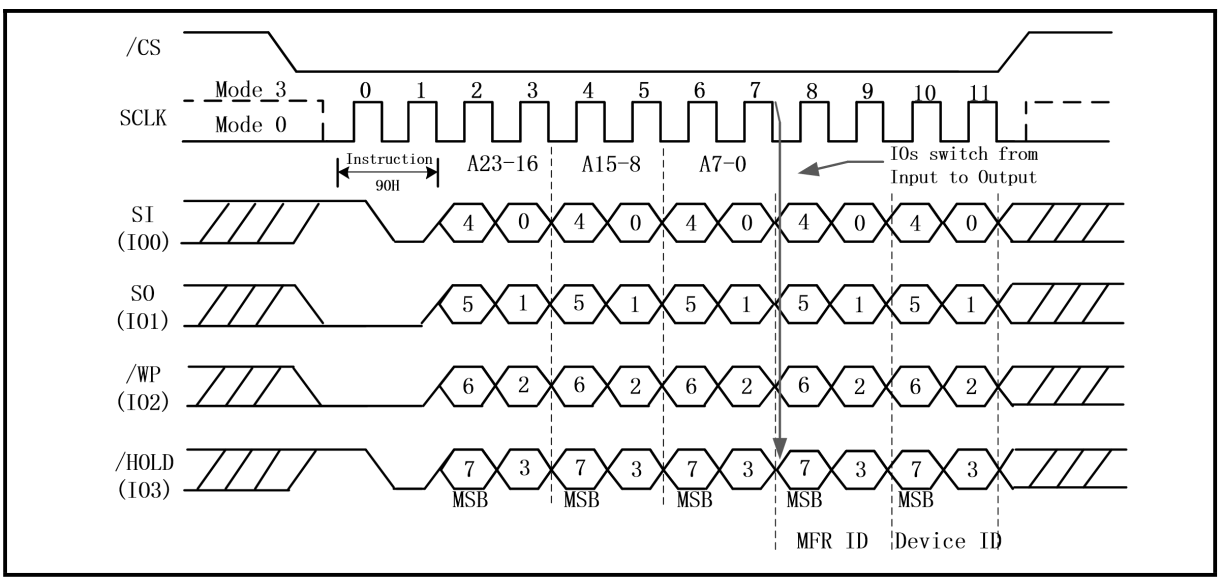


Figure 85. Read Manufacture ID/ Device ID Sequence Diagram (QPI Mode)



7.3.2 Dual I/O Read Manufacture ID/ Device ID (92H)

See ***Figure 86-Figure 87***, the Dual I/O Read Manufacturer/Device ID instruction is an alternative to the Release from Power-Down/Device ID instruction that provides both the JEDEC assigned Manufacturer ID and the specific Device ID by Dual I/O.

The instruction is initiated by driving the /CS pin low and shifting the instruction code “92H” followed by a 24/32-bit address (A23/31-A0) of 000000/00000000H.

Figure 86. Dual I/O Read Manufacture ID/ Device ID Sequence Diagram (SPI Mode/3-Byte Address Mode)

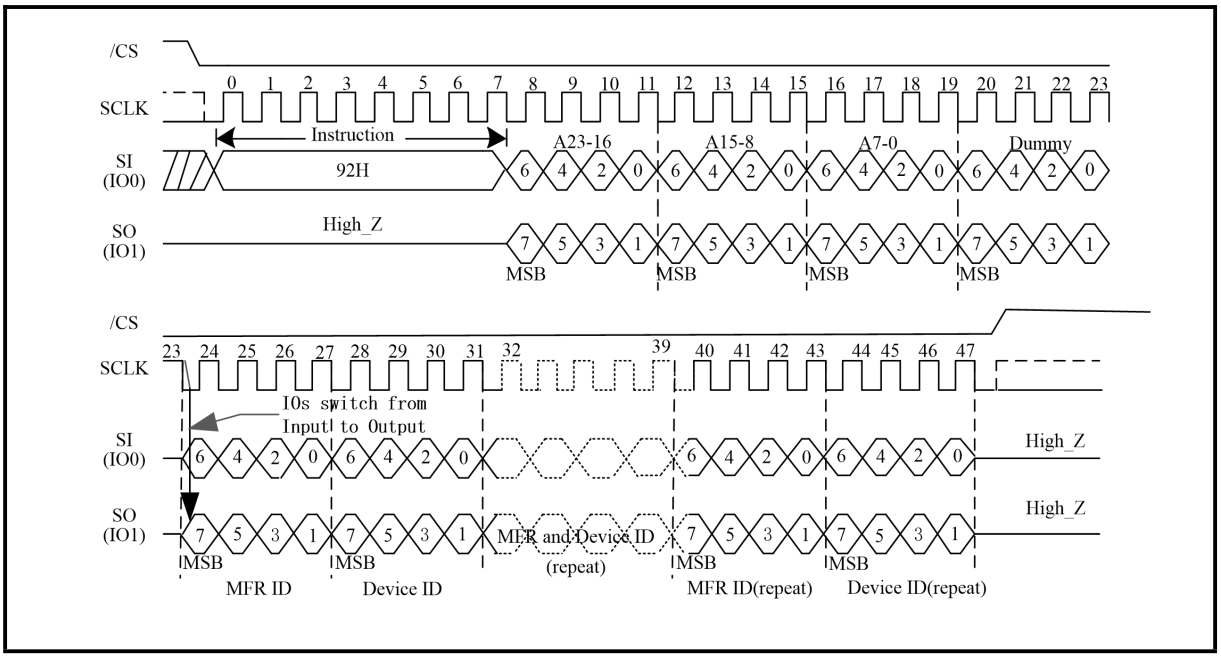
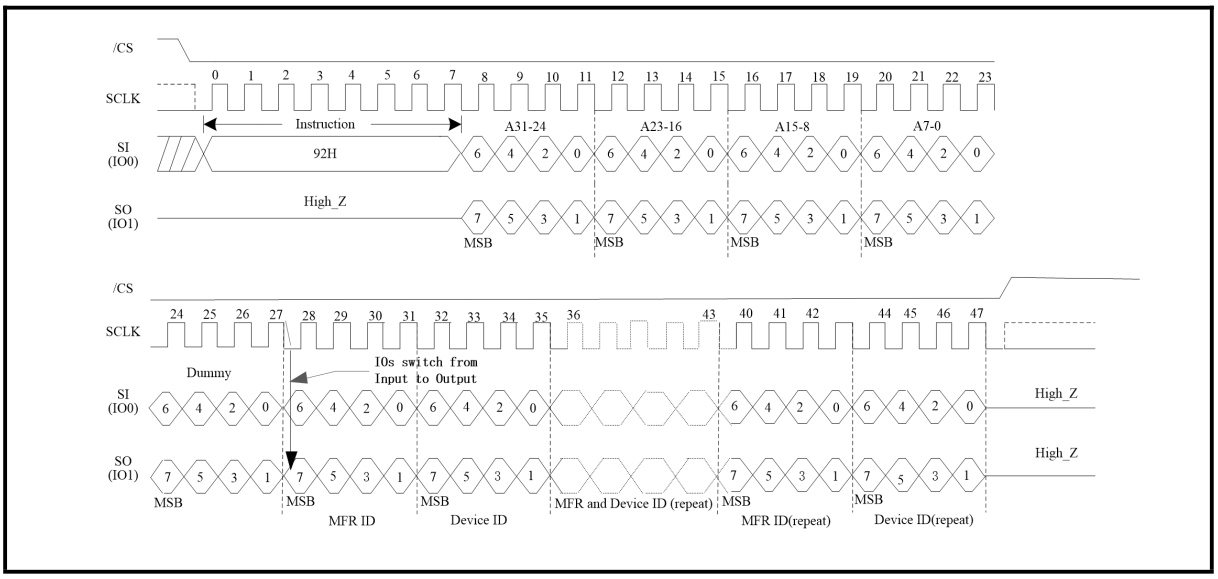


Figure 87. Dual I/O Read Manufacture ID/ Device ID Sequence Diagram (SPI Mode/4-Byte Address Mode)



7.3.3 Quad I/O Read Manufacture ID/ Device ID (94H)

See ***Figure 88-Figure 89***, the Quad I/O Read Manufacturer/Device ID instruction is an alternative to the Release from Power-Down/Device ID instruction that provides both the JEDEC assigned Manufacturer ID and the specific Device ID by quad I/O. The Quad Enable bit (QE) of Status Register must be set to enable.

The instruction is initiated by driving the /CS pin low and shifting the instruction code “94H” followed by a 24/32-bit address (A23/31-A0) of 000000H and 6 dummy clocks.

Figure 88. Quad I/O Read Manufacture ID/ Device ID Sequence Diagram (SPI Mode/3-Byte Address Mode)

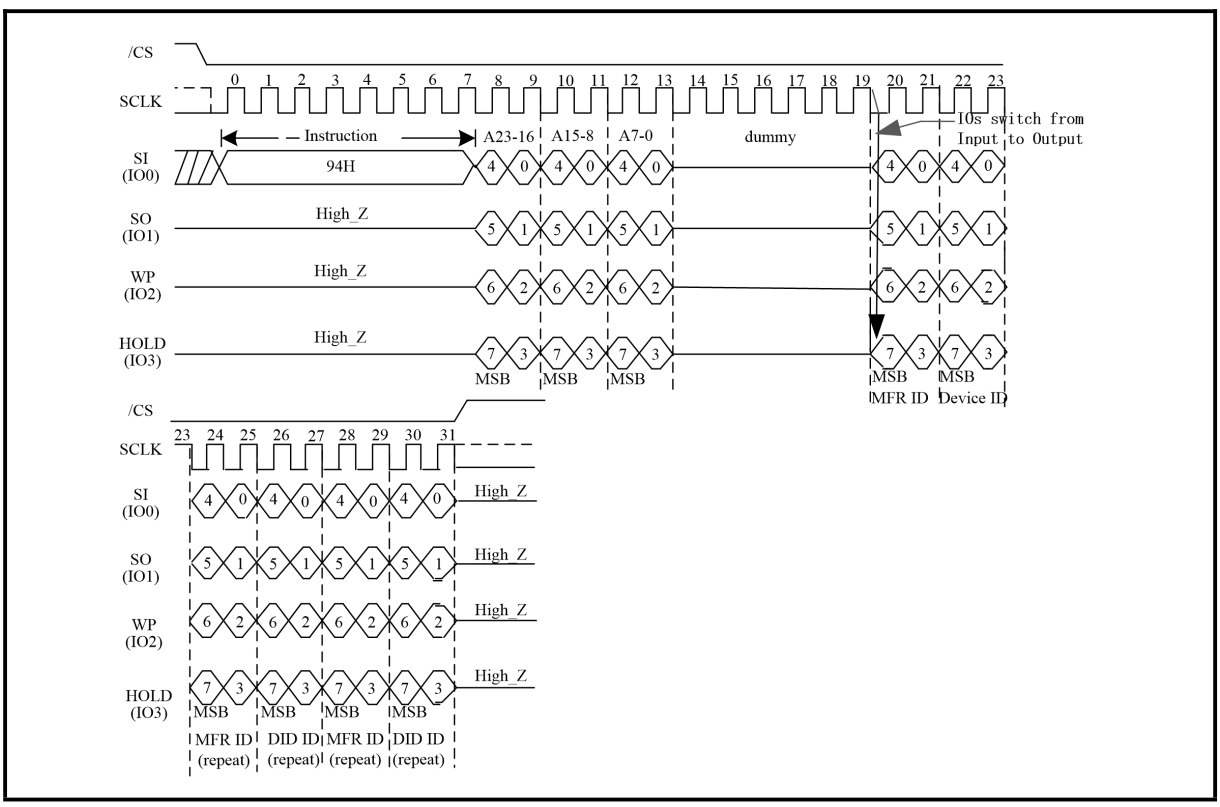
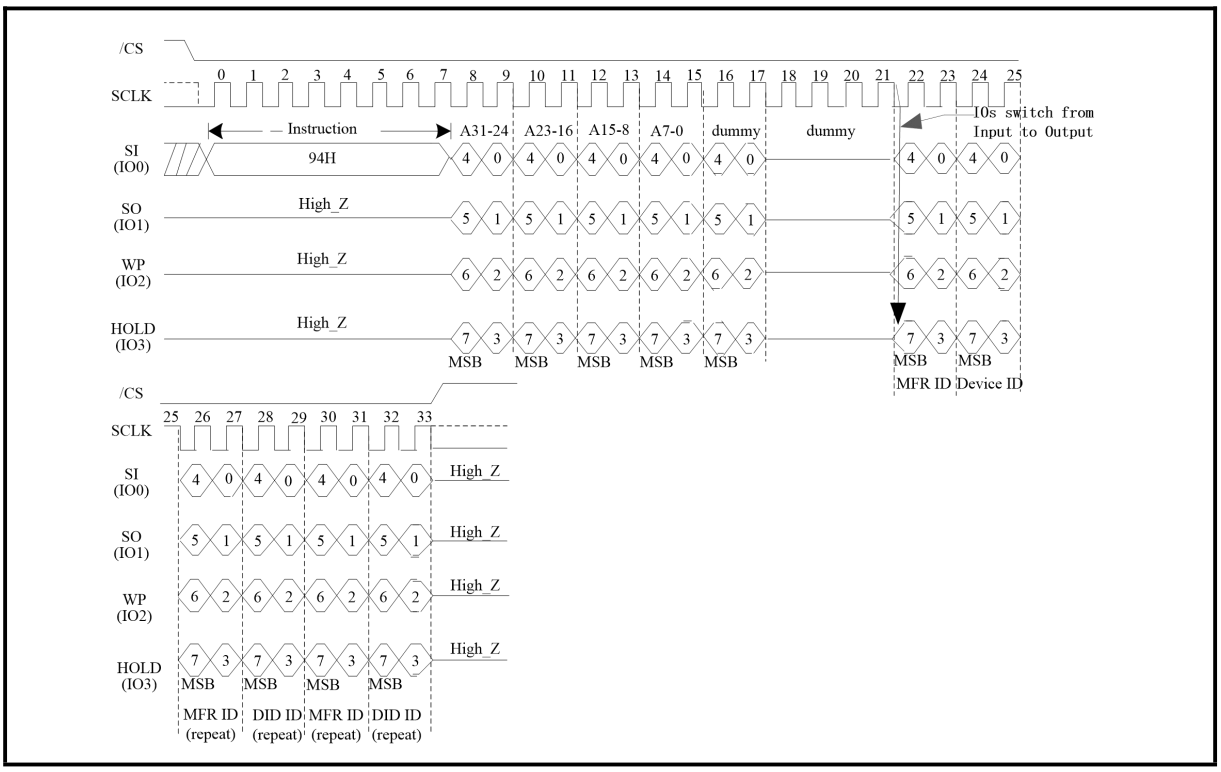


Figure 89. Quad I/O Read Manufacture ID/ Device ID Sequence Diagram (SPI Mode/3-Byte Address Mode)



7.3.4 Read JEDEC ID (9FH)

The JEDEC ID instruction allows the 8-bit manufacturer identification to be read, followed by two bytes of device identification. The device identification indicates the memory type in the first byte, and the memory capacity of the device in the second byte. JEDEC ID instruction while an Erase or Program cycle is in progress, is not decoded, and has no effect on the cycle that is in progress. The JEDEC ID instruction should not be issued while the device is in Deep Power-Down Mode.

See ***Figure 90-Figure 91***, the device is first selected by driving /CS to low. Then, the 8-bit instruction code for the instruction is shifted in. This is followed by the 24-bit device identification, stored in the memory, being shifted out on Serial Data Output, each bit being shifted out during the falling edge of Serial Clock. The JEDEC ID instruction is terminated by driving /CS to high at any time during data output. When /CS is driven high, the device is put in the Standby Mode. Once in the Standby Mode, the device waits to be selected, so that it can receive, decode and execute instructions.

Figure 90. JEDEC ID Sequence Diagram (SPI Mode)

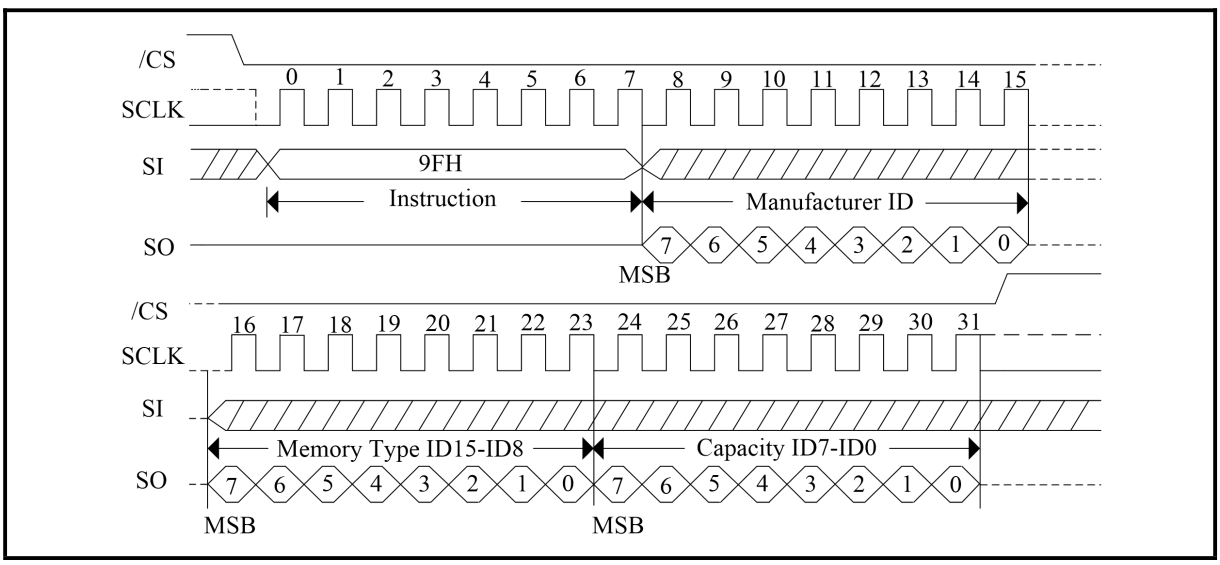
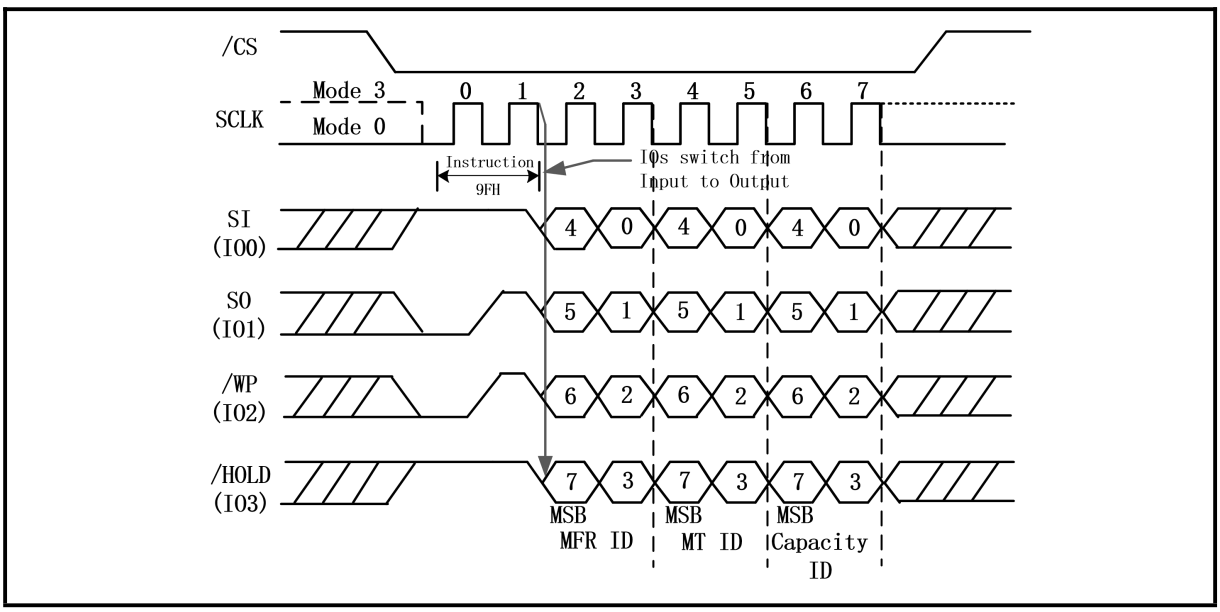


Figure 91. JEDEC ID Sequence Diagram (QPI Mode)



7.3.5 Read Unique ID Number (4Bh)

The Read Unique ID Number instruction accesses a factory-set read-only 128-bit number that is unique to each BY25FQ256 device. The ID number can be used in conjunction with user software methods to help prevent copying or cloning of a system. The Read Unique ID instruction is initiated by driving the /CS pin low and shifting the instruction code “4Bh” followed by four or five bytes of dummy clocks in SPI mode. In QPI mode, it contains 3/4 bytes dummy and some dummy that can be configured by the “Set Read Parameters (C0h)” instruction. After which, the 128-bit ID is shifted out on the falling edge of SCLK as shown from ***Figure 106*** to ***Figure 109***.

Figure 92. Read Unique ID Sequence Diagram (SPI Mode/3-Byte Address Mode)

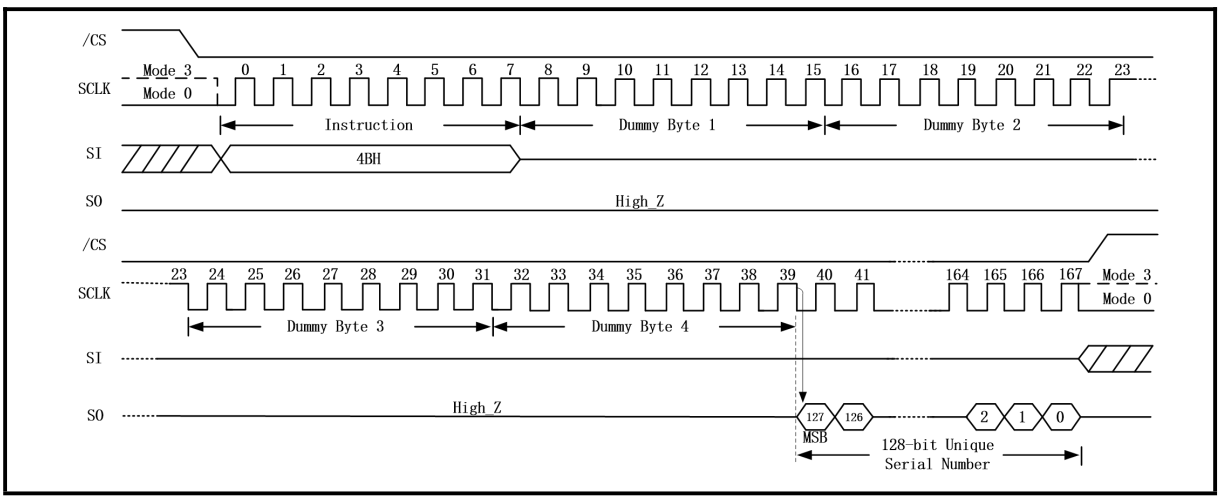


Figure 93. Read Unique ID Sequence Diagram (SPI Mode/4-Byte Address Mode)

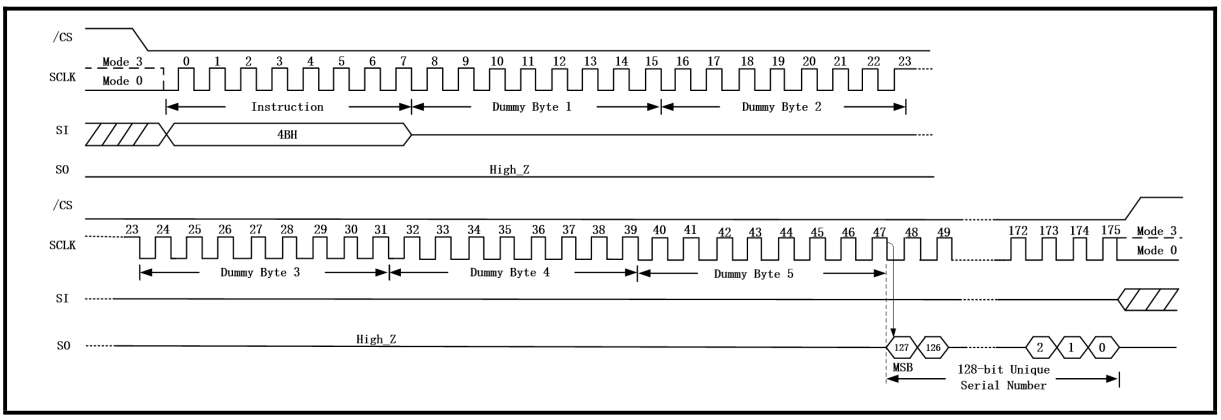


Figure 94. Read Unique ID Sequence Diagram (QPI Mode/3-Byte Address Mode)

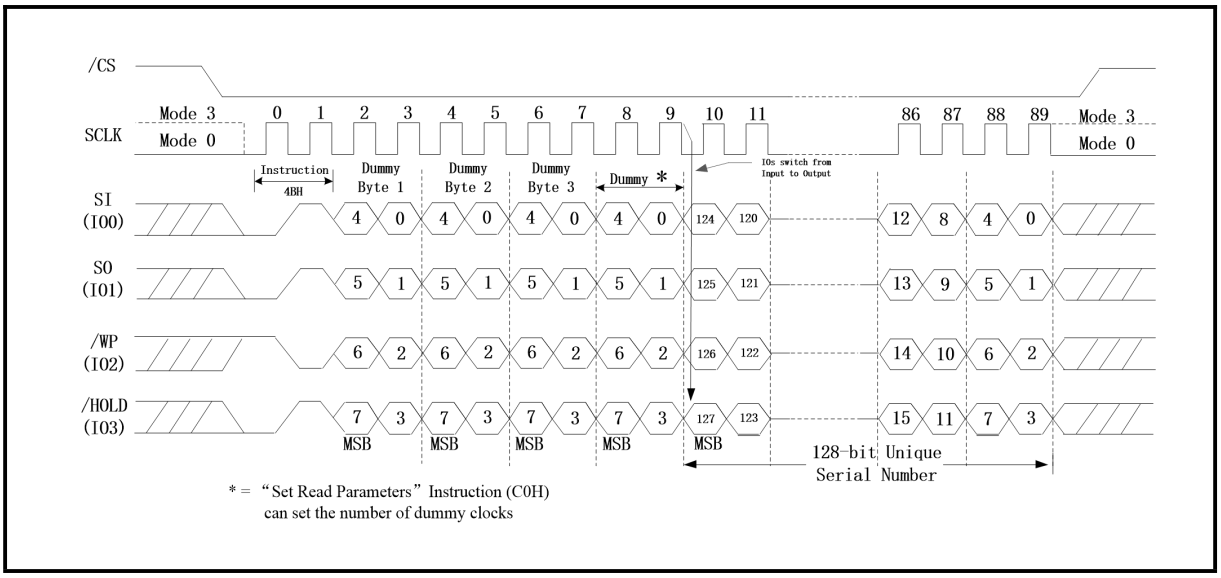
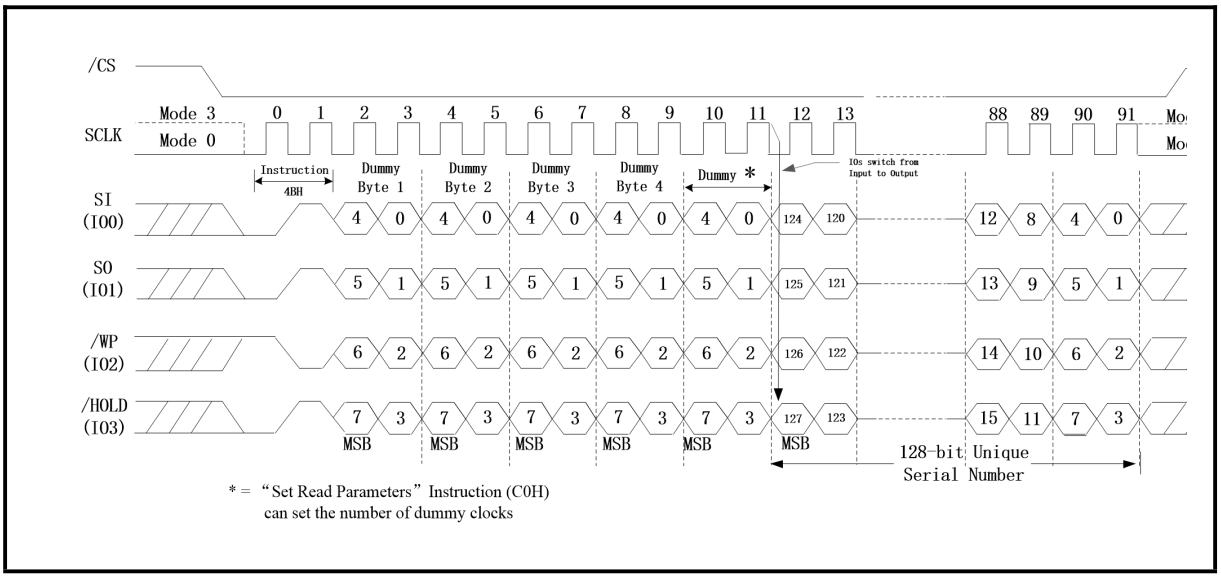


Figure 95. Read Unique ID Sequence Diagram (QPI Mode/4-Byte Address Mode)



7.3.6 Deep Power-Down (B9H)

Although the standby current during normal operation is relatively low, standby current can be further reduced with the Deep Power-down instruction. The lower power consumption makes the Deep Power-down (DPD) instruction especially useful for battery powered applications (*see ICC1 and ICC2*). The instruction is initiated by driving the /CS pin low and shifting the instruction code "B9h" as shown in ***Figure 96-Figure 97***

The /CS pin must be driven high after the eighth bit has been latched. If this is not done the Deep Power down instruction will not be executed. After /CS is driven high, the power-down state will entered within the time duration of tDP. While in the power-down state only the Release from Deep Power-down/Device ID instruction, software reset sequence or hardware reset sequence, which restores the device to normal operation, will be recognized. All other Instructions are ignored. This includes the Read Status Register instruction, which is always available during normal operation. Ignoring all but one instruction also makes the Power Down state a useful condition for securing maximum write protection. The device always powers-up in the normal operation with the standby current of ICC1.

Figure 96. Deep Power-Down Sequence Diagram (SPI Mode)

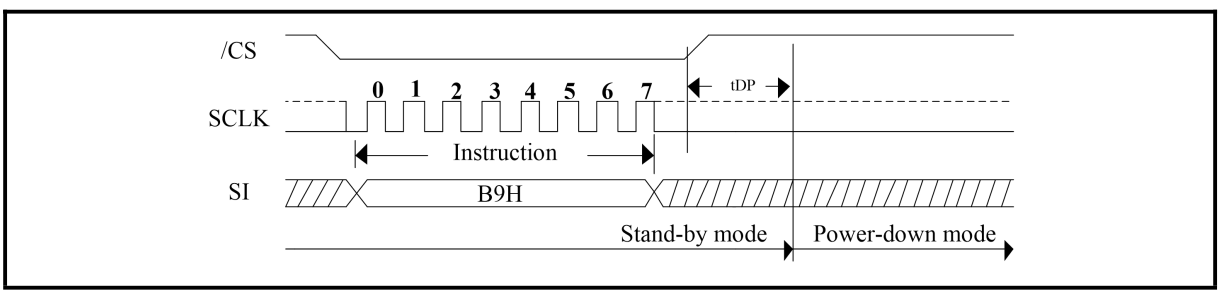
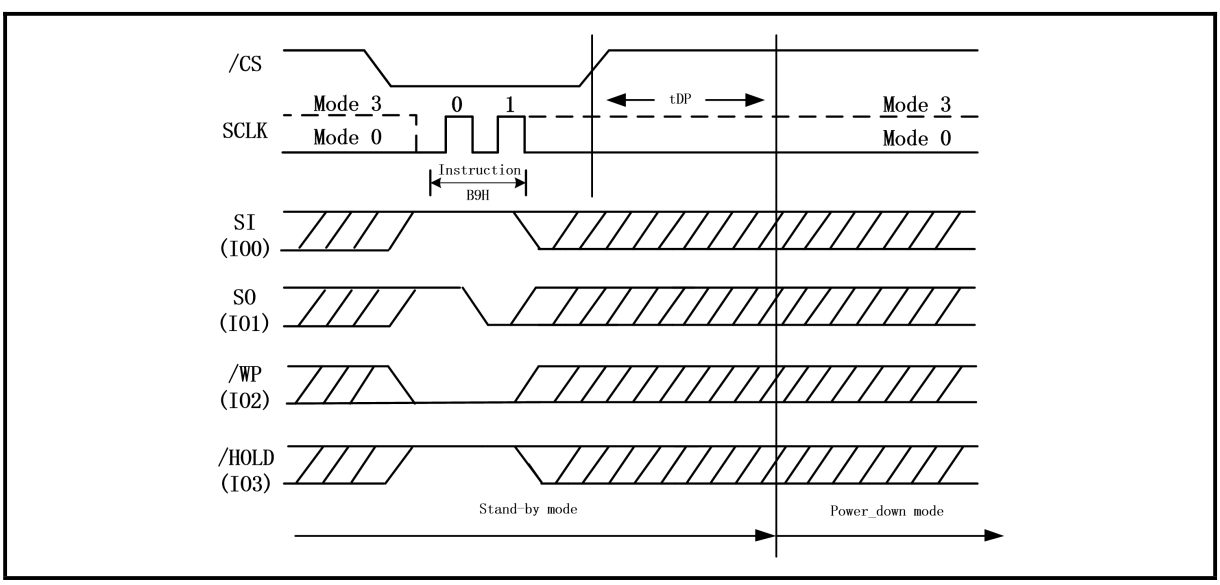


Figure 97. Deep Power-Down Sequence Diagram (QPI Mode)



7.3.7 Release from Deep Power-Down/Read Device ID (ABH)

The Release from Power-Down or Device ID instruction is a multi-purpose instruction. It can be used to release the device from the Power-Down state or obtain the devices electronic identification (ID) number.

See ***Figure 98-Figure 99***, to release the device from the Power-Down state, the instruction is issued by driving the /CS pin low, shifting the instruction code "ABH" and driving /CS high Release from Power-Down will take the time duration of tRES1 (See *AC Characteristics*) before the device will resume normal operation and other instruction are accepted. The /CS pin must remain high during the tRES1 time duration.

When used only to obtain the Device ID while not in the Power-Down state, the instruction is initiated by driving the /CS pin low and shifting the instruction code "ABH" followed by 3-dummy byte. The Device ID bits are then shifted out on the falling edge of SCLK with most significant bit (MSB) first as shown in ***Figure 100-Figure 101***. The Device ID value for the BY25FQ256 is listed in Manufacturer and Device Identification table. The Device ID can be read continuously. The instruction is completed by driving /CS high.

When used to release the device from the Power-Down state and obtain the Device ID, the instruction is the same as previously described, and shown in ***Figure 100-Figure 101***, except that after /CS is driven high it must remain high for a time duration of tRES2 (See *AC Characteristics*). After this time duration the device will resume normal operation and other instruction will be accepted. If the Release from Power-Down/Device ID instruction is issued while an Erase, Program or Write cycle is in process (when WIP equal 1) the instruction is ignored and will not have any effects on the current cycle.

Figure 98. Release Power-Down Sequence Diagram (SPI Mode)

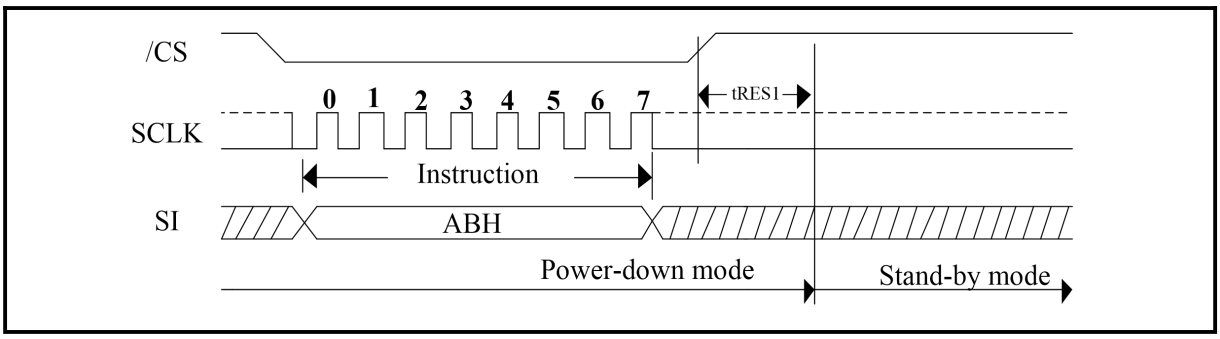


Figure 99. Release Power-Down Sequence Diagram (QPI Mode)

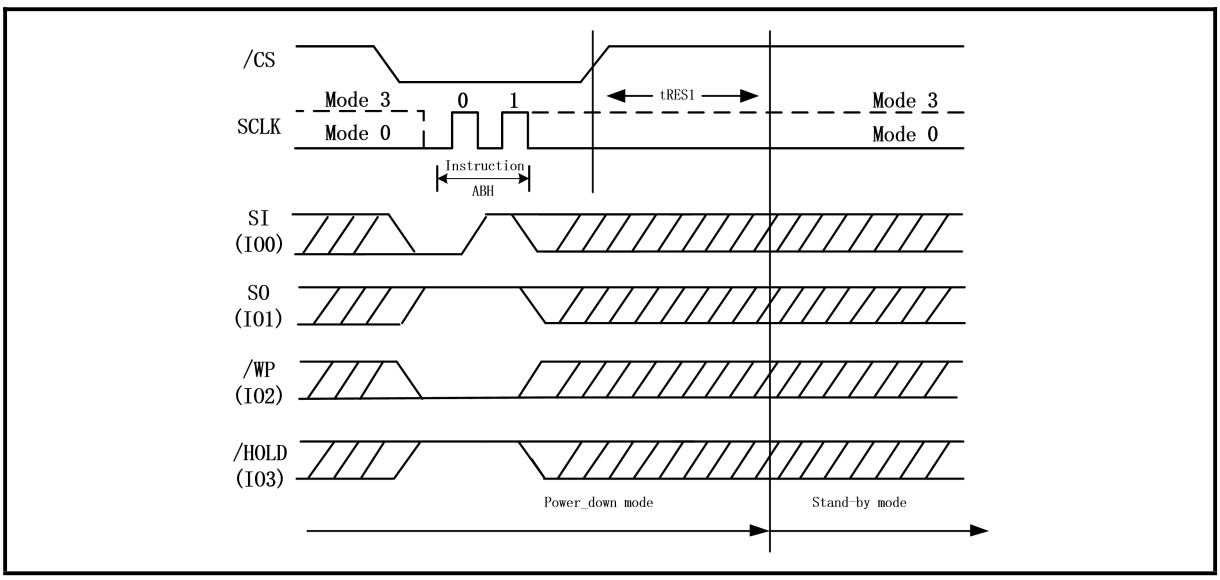


Figure 100. Release Power-Down/Read Device ID Sequence Diagram (SPI Mode)

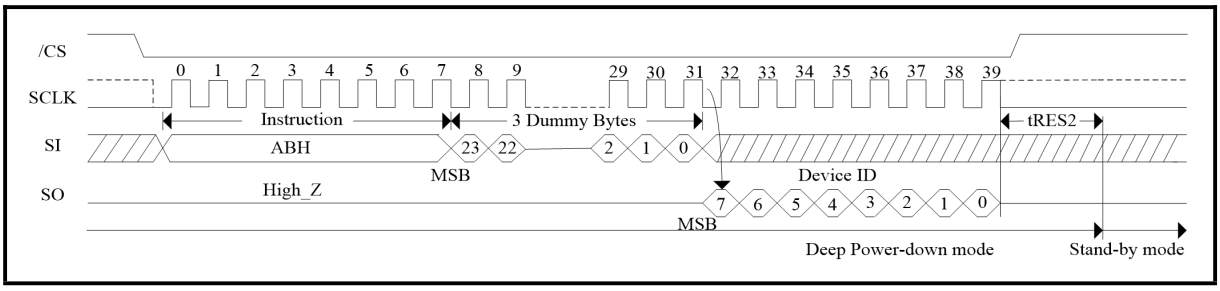
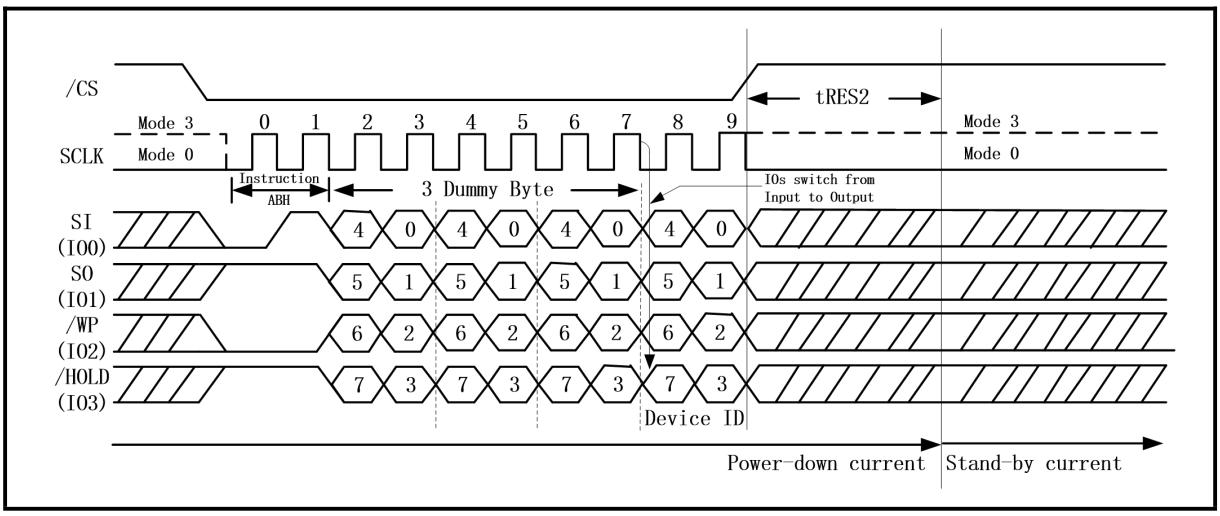


Figure 101. Release Power-Down/Read Device ID Sequence Diagram (QPI Mode)



7.3.8 Read Security Registers (48H)

See ***Figure 102-Figure 105***, the instruction is followed by a 3/4-byte address (A23/31-A0) and the dummy byte. In QPI mode, the number of dummy can be configured by the "C0h" instruction. Each bit being latched-in during the rising edge of SCLK. Then the memory content, at that address, is shifted out on SO, each bit being shifted out, at a Max frequency fC, during the falling edge of SCLK. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. Once the A8-A0 address reaches the last byte of the register (Byte FFH), it will reset to 000H, the instruction is completed by driving /CS high.

ADDRESS	A23/31-A16	A15-12	A11-9	A8-0
Security Register #1	00H/0000H	0 0 0 1	0 0 0	Byte Address
Security Register #2	00H/0000H	0 0 1 0	0 0 0	Byte Address
Security Register #3	00H/0000H	0 0 1 1	0 0 0	Byte Address

Figure 102. Read Security Registers instruction Sequence Diagram (SPI Mode/3-Byte Address Mode)

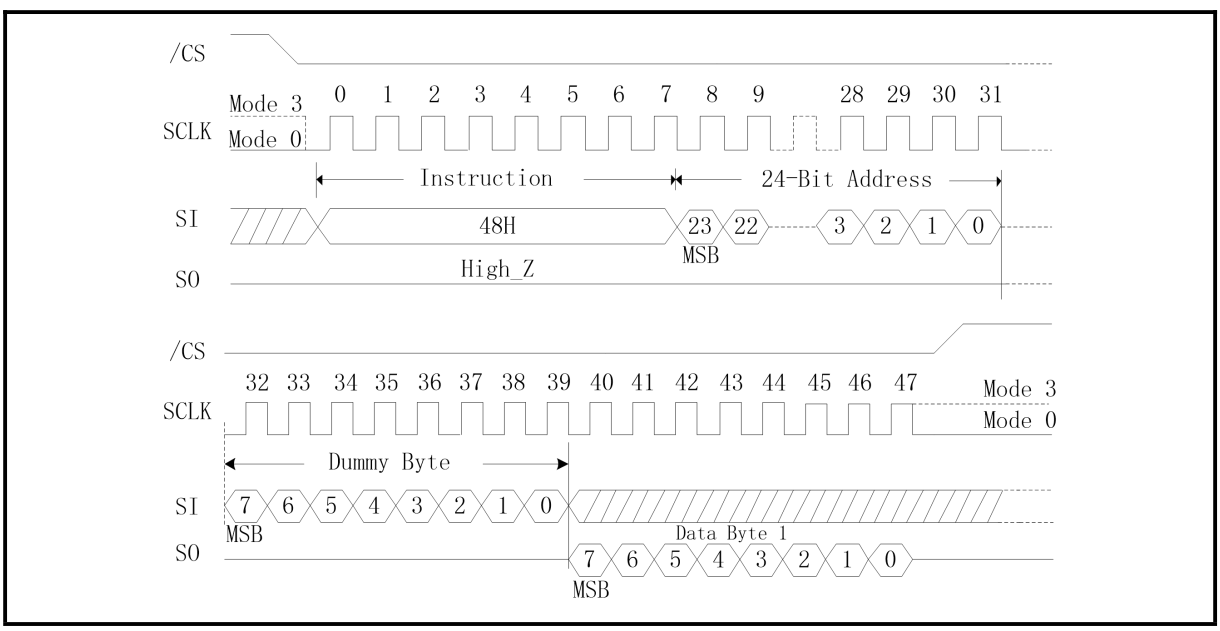


Figure 103. Read Security Registers instruction Sequence Diagram (SPI Mode/4-Byte Address Mode)

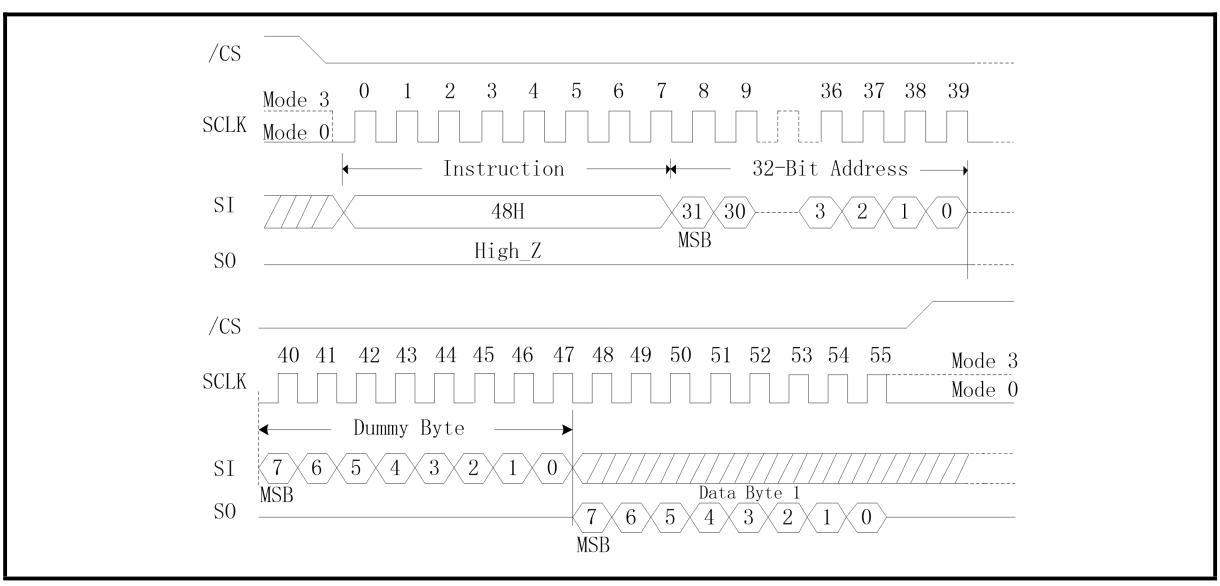


Figure 104. Read Security Registers instruction Sequence Diagram (QPI Mode/3-Byte Address Mode)

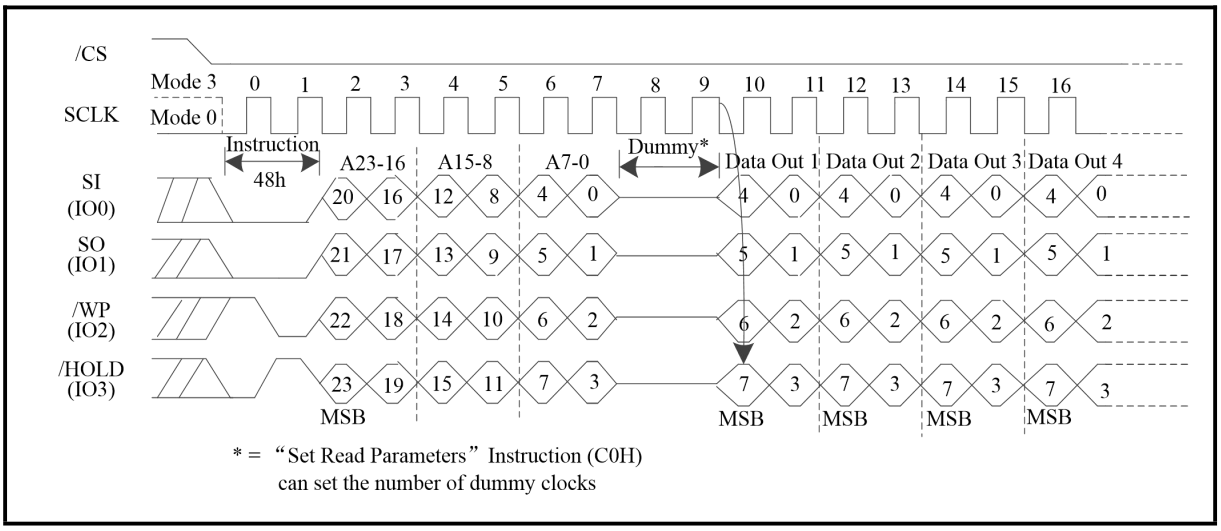
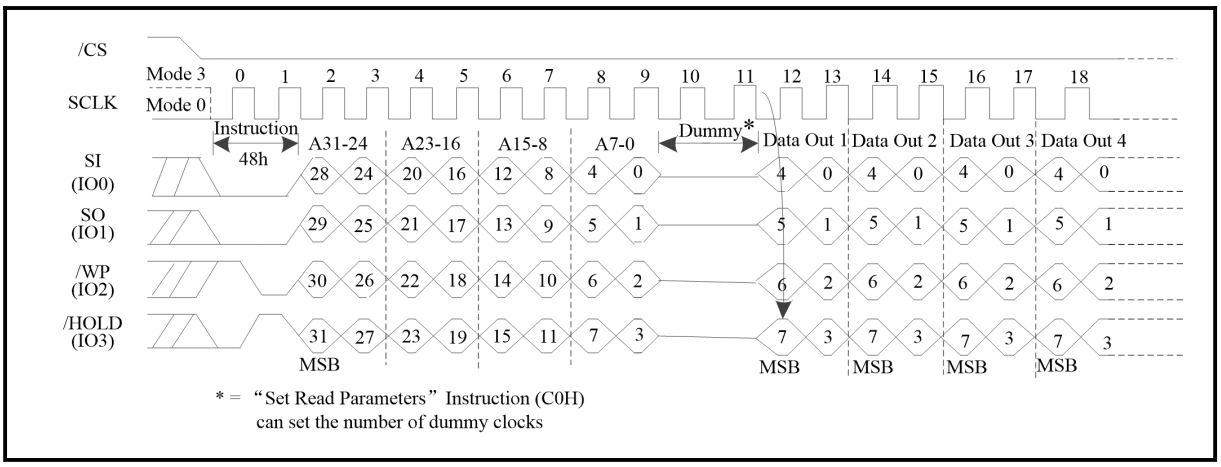


Figure 105. Read Security Registers instruction Sequence Diagram (QPI Mode/4-Byte Address Mode)



7.3.9 Erase Security Registers (44H)

The BY25FQ256 provides three 1024-byte Security Registers which can be erased and programmed individually. These registers may be used by the system manufacturers to store security and other important information separately from the main memory array.

See ***Figure 106-Figure 109***, the Erase Security Registers instruction is similar to Block/Sector Erase instruction. A Write Enable instruction must previously have been executed to set the Write Enable Latch bit.

The Erase Security Registers instruction sequence: /CS goes low sending Erase Security Registers instruction /CS goes high. /CS must be driven high after the eighth bit of the instruction code has been latched in otherwise the Erase Security Registers instruction is not executed. As soon as /CS is driven high, the self-timed Erase Security Registers cycle (whose duration is tSE) is initiated. While the Erase Security Registers cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Erase Security Registers cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch bit is reset. The Security Registers Lock Bit (LB) in the Status Register can be used to OTP protect the security registers. Once the LB bit is set to 1, the Security Registers will be permanently locked; the Erase Security Registers instruction will be ignored.

ADDRESS	A23/31-A16	A15-12	A11-9	A8-0
Security Register #1	00H/0000H	0 0 0 1	0 0 0	Byte Address
Security Register #2	00H/0000H	0 0 1 0	0 0 0	Byte Address
Security Register #3	00H/0000H	0 0 1 1	0 0 0	Byte Address

Figure 106. Erase Security Registers instruction Sequence Diagram (SPI Mode/3-Byte Address Mode)

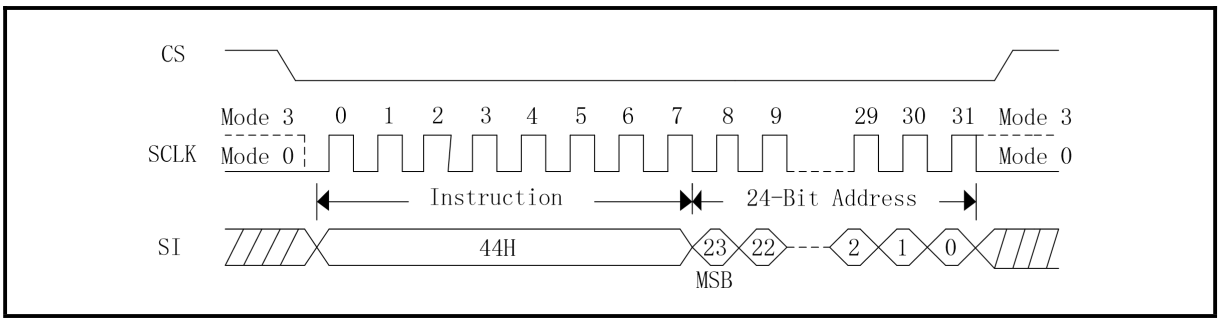


Figure 107. Erase Security Registers instruction Sequence Diagram (SPI Mode/4-Byte Address Mode)

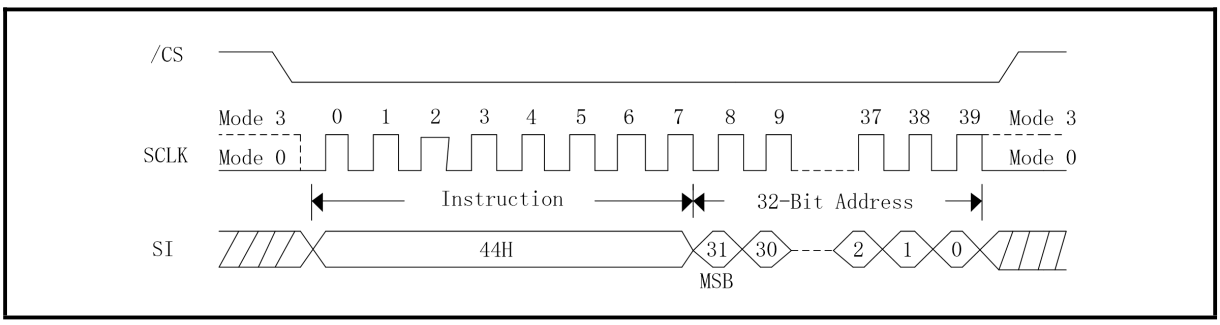


Figure 108. Erase Security Registers instruction Sequence Diagram (QPI Mode/3-Byte Address Mode)

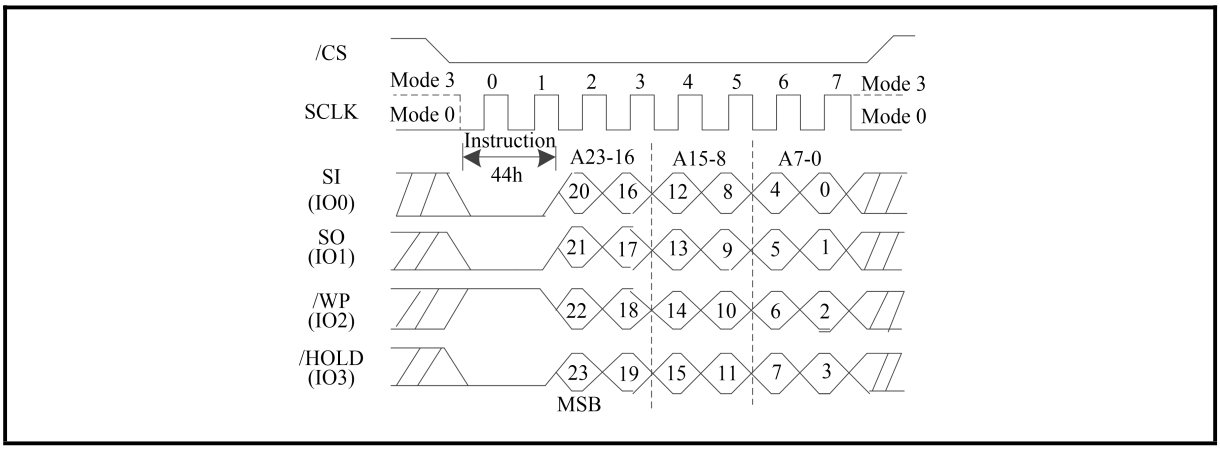
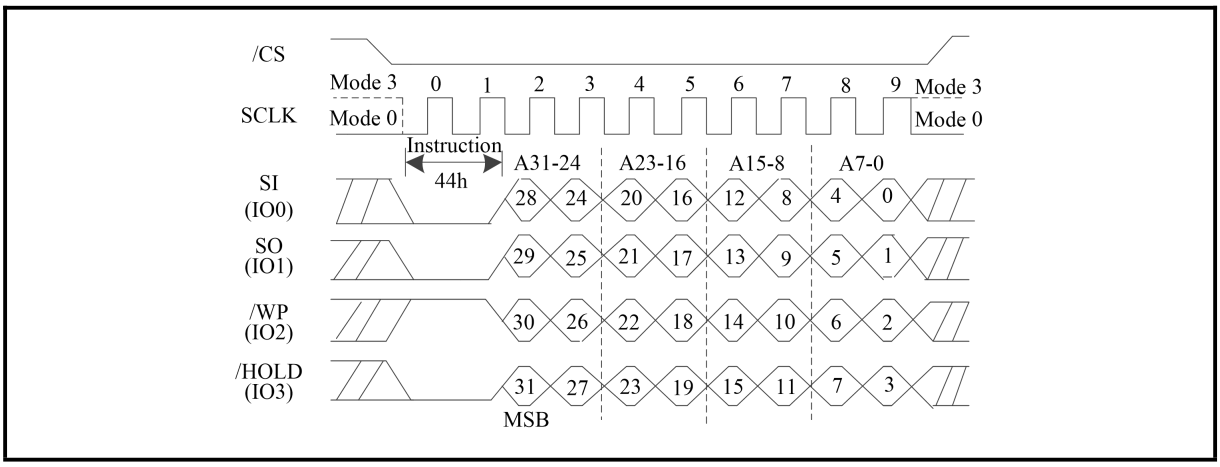


Figure 109. Erase Security Registers instruction Sequence Diagram (QPI Mode/4-Byte Address Mode)



7.3.10 Program Security Registers (42H)

See ***Figure 110-Figure 113***, the Program Security Registers instruction is similar to the Page Program instruction. It allows from one byte to 1024 bytes of security register data to be programmed by two times (one time program 256 bytes). A Write Enable instruction must previously have been executed to set the Write Enable Latch bit before sending the Program Security Registers instruction. The Program Security Registers instruction is entered by driving /CS Low, followed by the instruction code (42H), 3/4-byte address and at least one data byte on SI. As soon as /CS is driven high, the self-timed Program Security Registers cycle (whose duration is tPP) is initiated. While the Program Security Registers cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Program Security Registers cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch bit is reset.

If the Security Registers Lock Bit (LB3/LB2/LB1) is set to 1, the Security Registers will be permanently locked. Program Security Registers instruction will be ignored.

ADDRESS	A23/31-A16	A15-12	A11-10	A9-0
Security Register #1	00H/0000H	0 0 0 1	0 0	Byte Address
Security Register #2	00H/0000H	0 0 1 0	0 0	Byte Address
Security Register #3	00H/0000H	0 0 1 1	0 0	Byte Address

Figure 110. Program Security Registers instruction Sequence Diagram (SPI Mode/3-Byte Address Mode)

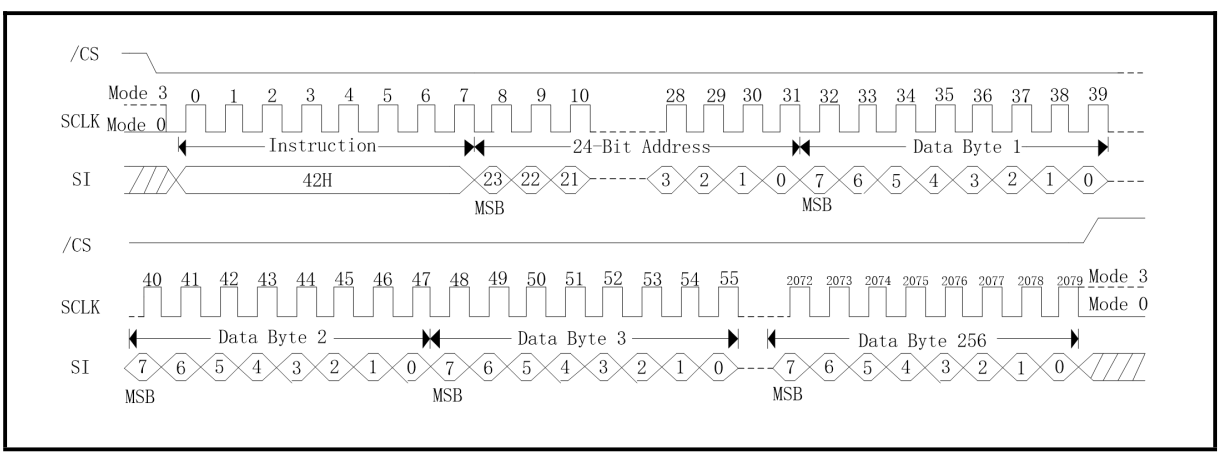


Figure 111. Program Security Registers instruction Sequence Diagram (SPI Mode/4-Byte Address Mode)

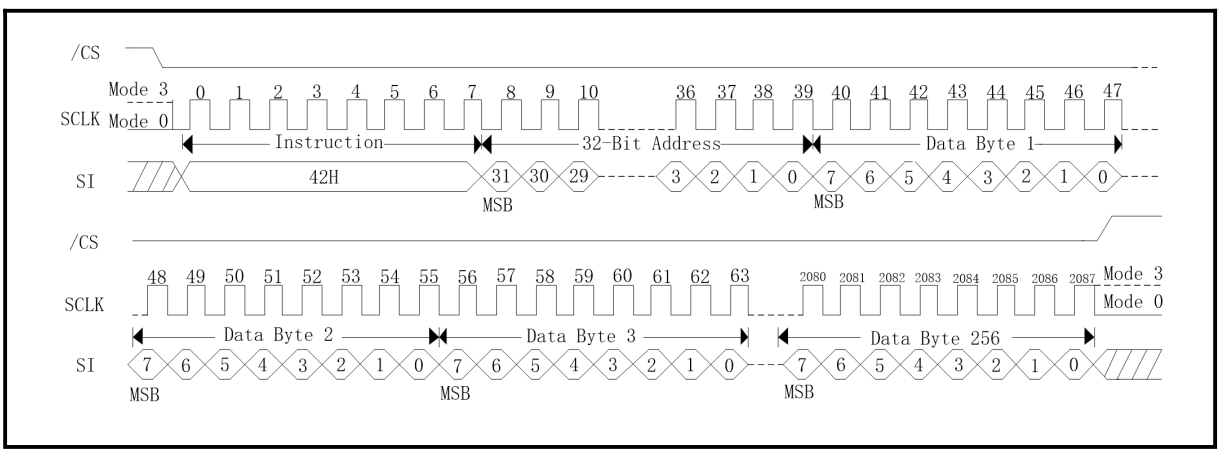


Figure 112. Program Security Registers instruction Sequence Diagram (QPI Mode/3-Byte Address Mode)

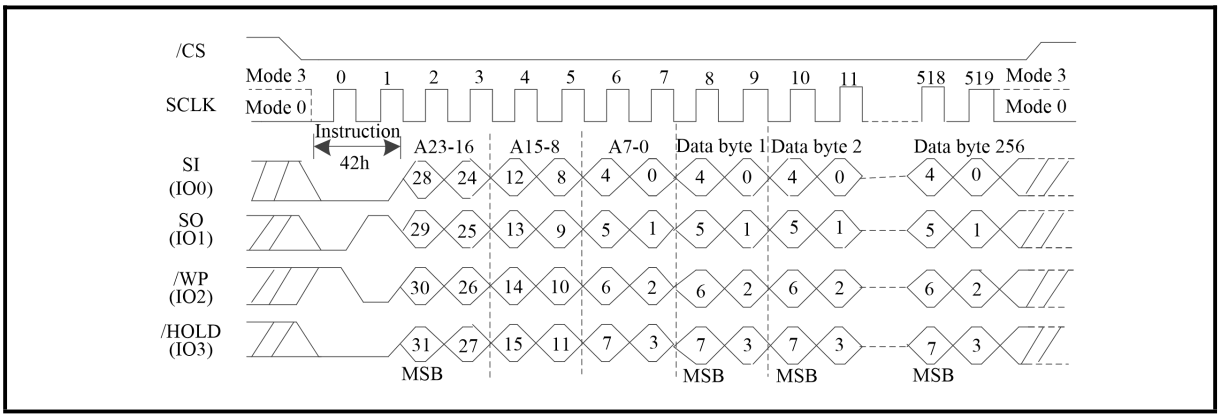
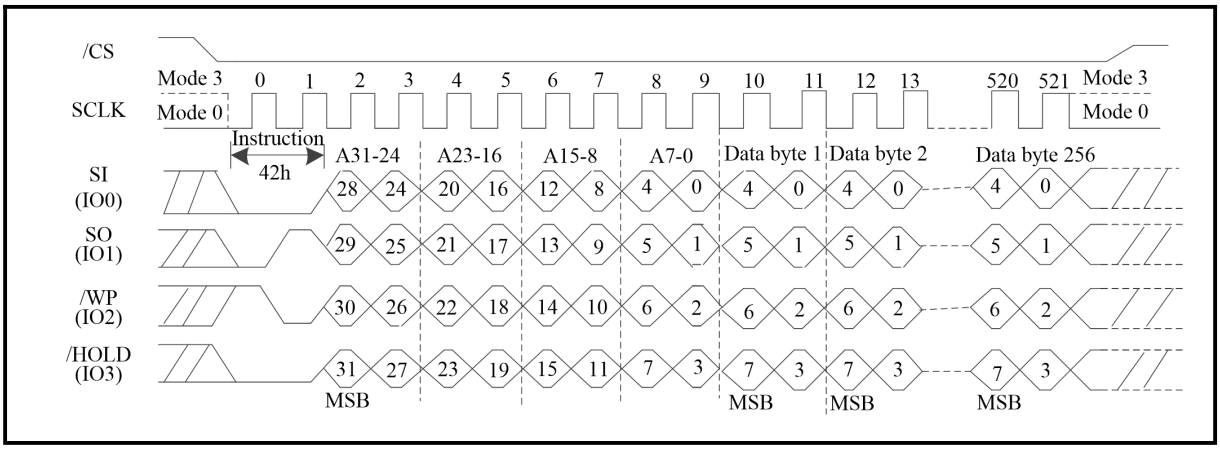


Figure 113. Program Security Registers instruction Sequence Diagram (QPI Mode/4-Byte Address Mode)



7.3.11 Read Serial Flash Discoverable Parameter (5AH)

See ***Figure 114-Figure 115,***The Serial Flash Discoverable Parameter (SFDP) standard provides a consistent method of describing the functional and feature capabilities of serial flash devices in a standard set of internal parameter tables. These parameter tables can be interrogated by host system software to enable adjustments needed to accommodate divergent features from multiple vendors. The concept is similar to the one found in the Introduction of JEDEC Standard, JESD68 on CFI. SFDP is a standard of JEDEC Standard No.216.

The Read SFDP instruction is initiated by driving the /CS pin low and shifting the instruction code “5Ah” followed by a 24-bit address (A23-A0) into the SI pin, regardless of the 3-byte or 4-byte Address Mode. Eight “dummy” clocks are also required in SPI mode. In QPI mode，the number of dummy clocks can be configured by the “Set Read Parameters (C0h)” instruction.

Figure 114. Read Serial Flash Discoverable Parameter instruction Sequence Diagram (SPI Mode)

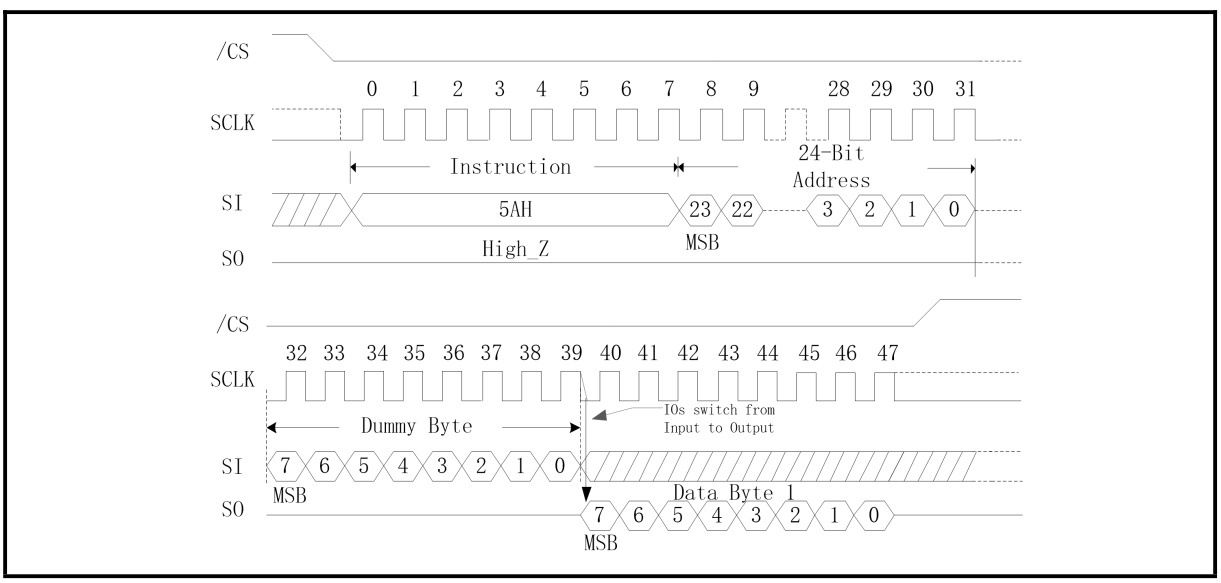


Figure 115. Read Serial Flash Discoverable Parameter instruction Sequence Diagram (QPI Mode)

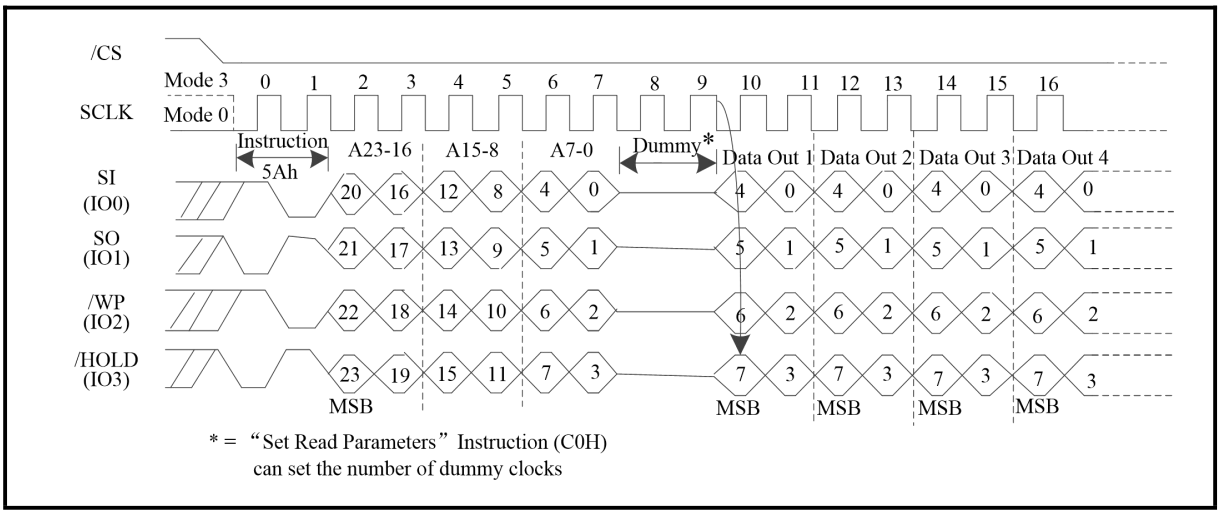


Table 7.3.11.a. Signature and Parameter Identification Data Values

Description	Comment	Add(H) (Byte)	DW Add (Bit)	Data	Data
SFDP Signature	Fixed:50444653H	00H	07:00	53H	53H
		01H	15:08	46H	46H
		02H	23:16	44H	44H
		03H	31:24:	50H	50H
SFDP Minor Revision Number	Start from 00H	04H	07:00	08H	08H
SFDP Major Revision Number	Start from 01H	05H	15:08	01H	01H
Number of Parameters Headers	Start from 00H	06H	23:16	02H	02 H
Unused	Contains 0xFFH and can never be changed	07H	31:24	FFH	FFH
ID number (JEDEC)	00H: It indicates a JEDEC specified header	08H	07:00	00H	00H
1st Parameter Table Minor Revision Number	Start from 0x00H	09H	15:08	07H	07H
1st Parameter Table Major Revision Number	Start from 0x01H	0AH	23:16	01H	01H
1st Parameter Table Length (in double word)	How many DWORDs in the Parameter table	0BH	31:24	10H	10H
1st Parameter Table Pointer (PTP)	First address of JEDEC Flash Parameter table	0CH	07:00	30H	30H
		0DH	15:08	00H	00H
		0EH	23:16	00H	00H
Unused	Contains 0xFFH and can never be changed	0FH	31:24	FFH	FFH
ID Number LSB (Manufacturer ID)	It is indicates BoyaDevice manufacturer ID	10H	07:00	68H	68H
2nd Parameter Table Minor Revision Number	Start from 0x00H	11 H	15:08	00H	00H
2nd Parameter Table Major Revision Number	Start from 0x01H	12H	23:16	01H	01H
2nd Parameter Table Length (in double word)	How many DWORDs in the Parameter table	13H	31:24	03H	03H
2nd Parameter Table Pointer (PTP)	First address of Boya Device Flash Parameter table	14H	07:00	90H	90H
		15H	15:08	00H	00H
		16H	23:16	00H	00H
Unused	Contains 0xFFH and can never be changed	17H	31:24	FFH	FFH
3rd Parameter ID LSB	4-byte Address Instruction Table is assigned the ID LSB of FF 84h	18H	07:00	84H	84H
3rd Parameter Minor Revision	Start from 0x00H	19H	15:08	01H	01H
3rd Parameter Major Revision	Start from 0x00H	1AH	23:16	01H	01H
3rd Parameter Length (in double words)	How many DWORDs in the Parameter table	1BH	31:24	02H	02H

3rd Parameter Table Pointer (byte address)	First address of Boya Device Flash Parameter table	1CH	07:00	C0H	C0H
		1DH	15:08	00H	00H
		1EH	23:16	00H	00H
3rd Parameter ID MSB	4-byte Address Instruction Table is assigned the ID of FF84h	1FH	31:24	FFH	FFH

Table 7.3.11.b. Parameter Table (0): JEDEC Flash Parameter Tables

Description	Comment	Add(H) (Byte)	DW Add (Bit)	Data	Data
Block/Sector Erase Size	00: Reserved; 01: 4KB erase; 10: Reserved; 11: not support 4KB erase	30H	01:00	01b	E5H
Write Granularity	0: 1Byte, 1: 64Byte or larger		02	1b	
Write Enable Instruction Requested for Writing to Volatile Status Registers	0: Nonvolatile status bit 1: Volatile status bit (BP status register bit)		03	0b	
Write Enable Opcode Select for Writing to Volatile Status Registers	0: Use 50H Opcode, 1: Use 06H Opcode, Note: If target flash status register is Nonvolatile, then bits 3 and 4 must be set to 00b.		04	0b	
Unused	Contains 111b and can never be changed		07:05	111b	
4KB Erase Opcode		31H	15:08	20H	20H
(1 -1 -2) Fast Read	0=Not support, 1=Support	32H	16	1b	FBH
Address Bytes Number used in addressing flash array	00: 3Byte only, 01: 3 or 4Byte, 10: 4Byte only, 11: Reserved		18:17	01b	
Double Transfer Rate (DTR) clocking	0=Not support, 1=Support		19	1b	
(1 -2-2) Fast Read	0=Not support, 1=Support		20	1b	
(1 -4-4) Fast Read	0=Not support, 1=Support		21	1b	
(1 -1 -4) Fast Read	0=Not support, 1=Support		22	1b	
Unused			23	1b	
Unused		33H	31:24	FFH	FFH
Flash Memory Density		37H:34H	31:00	0FFFFFFFH	
(1 -4-4) Fast Read Number of Wait states	00000b: Wait states (Dummy Clocks) not support	38H	04:00	00100b	44H
(1 -4-4) Fast Read Number of Mode Bits	000b:Mode Bits not support		07:05	010b	
(1 -4-4) Fast Read Opcode		39H	15:08	EBH	EBH
(1 -1 -4) Fast Read Number of Wait states	00000b: Wait states (Dummy Clocks) not support	3AH	20:16	01000b	08H
(1 -1 -4) Fast Read Number of Mode Bits	000b:Mode Bits not support		23:21	000b	
(1 -1 -4) Fast Read Opcode		3BH	31:24	6BH	6BH
(1 -1 -2) Fast Read Number of Wait states	00000b: Wait states (Dummy Clocks) not support	3CH	04:00	01000b	08H
(1 -1 -2) Fast Read Number of Mode Bits	000b: Mode Bits not support		07:05	000b	
(1 -1 -2) Fast Read Opcode		3DH	15:08	3BH	3BH
(1 -2-2) Fast Read Number of Wait states	0000b: Wait states (Dummy Clocks) not support	3EH	20:16	00010b	42H
(1 -2-2) Fast Read Number of Mode Bits	000b: Mode Bits not support		23:21	010b	
(1 -2-2) Fast Read Opcode		3FH	31:24	BBH	BBH
(2-2-2) Fast Read	0=not support 1=support	40H	00	0b	FEH
Unused			03:01	111b	
(4-4-4) Fast Read	0=not support 1=support		04	1b	
Unused			07:05	111b	
Unused		43H:41H	31:08	FFFFFFH	FFFFFFH
Unused		45H:44H	15:00	FFFFH	FFFFH
(2-2-2) Fast Read Number of Wait states	0 0000b: Wait states (Dummy Clocks) not support	46H	20:16	00000b	00H
(2-2-2) Fast Read Number of Mode Bits	000b: Mode Bits not support		23:21	000b	
(2-2-2) Fast Read Opcode		47H	31:24	FFH	FFH
Unused		49H:48H	15:00	FFFFH	FFFFH
(4-4-4) Fast Read Number of Wait states	0 0100b: Wait states (Dummy Clocks) 16 bits are needed	4AH	20:16	001 00b	44H

(4-4-4) Fast Read Number of Mode Bits	010b: Mode Bits 8 mode bits are needed			23:21	010b	
(4-4-4) Fast Read Opcode		4BH	31:24	EBH		EBH
Sector Type 1 Size	Sector/block size=2^N bytes 0x00b: this sector type don’t exist	4CH	07:00	0CH		0CH
Sector Type 1 erase Opcode		4DH	15:08	20H		20H
Sector Type 2 Size	Sector/block size=2^N bytes 0x00b: this sector type don’t exist	4EH	23:16	0FH		0FH
Sector Type 2 erase Opcode		4FH	31:24	52H		52H
Sector Type 3 Size	Sector/block size=2^N bytes 0x00b: this sector type don’t exist	50H	07:00	10H		10H
Sector Type 3 erase Opcode		51H	15:08	D8H		D8H
Sector Type 4 Size	Sector/block size=2^N bytes 0x00b: this sector type don’t exist	52H	23:16	00H		00H
Sector Type 4 erase Opcode		53H	31:24	FFH		FFH
Erase Type (1:4) Typical Erase Times and Multiplier Used To Derive Max Erase Times	Multiplier from typical erase time to maximum erase time, 3:0 count Formula: Erase Type n (or Chip) erase maximum time = 2 * (count + 1) * Erase Type n (or Chip) erase typical time	54H	03:00	0010b		22H
	Erase Type 1 Erase, Typical time 8:4 count Formula: typical time = (count + 1)*units		07:04	0010b		
		55H	08	0b		4AH
			10:09	01b		
	Erase Type 2 Erase, Typical time 17:16 units (00b: 1 ms, 01b: 16 ms, 10b: 128 ms, 11b: 1 s), 15:11 count Formula: typical time = (count + 1)*units		15:11	01001b		
		56H	17:16	01b		05H
	Erase Type 3 Erase, Typical time 24:23 units (00b: 1 ms, 01b: 16 ms, 10b: 128 ms, 11b: 1 s), 22:18 count Formula: typical time = (count + 1)*units		22:18	00001b		
			23	0b		
		57H	24	1b		FFH
	Erase Type 4 Erase(DCh 256 kbyte erase), Typical time 31:30 units (00b: 1 ms, 01b: 16 ms, 10b: 128 ms, 11b: 1 s), 29:25 count Formula: typical time = (count + 1)*units		29:25	11111b		
			31:30	11b		
Chip Erase Typical Time, Byte Program and Page Program Typical Times, Page Size	Multiplier from typical time to max time for Page or byte program, 3:0 count Formula: maximum time = 2 * (count + 1)*typical time	58H	3:0	0010b		82H
	Page Size This field specifies 'N' and is used to calculate page size = 2^N bytes.		7:4	1000b		
	Page Program Typical time 13 units (0: 8 µs, 1: 64 µs), 12:8 count Formula: typical page program time = (count + 1)*units	59H	12:08	01001b		E9H
			13	1b		
	Byte Program Typical time, first byte 18 units (0: 1 µs, 1: 8 µs), 17:14 count Formula: first byte typical time = (count + 1)*units		15:14	11b		
		5AH	17:16	00b		14H
			18	1b		
	Byte Program Typical time, additional byte 23 units (0: 1 µs, 1: 8 µs), 22:19 count Formula: additional byte time = (count + 1)*units/byte		22:19	0010b		
			23	0b		
	Chip Erase, Typical time 30:29 units (00b: 16 ms, 01b: 256 ms, 10b: 4 s, 11b: 64 s), 28:24 count Formula: typical time = (count + 1)*units	5BH	28:24	01110b		CEH
			30:29	10b		
	Reserved		31	1b		
Erase/Program Suspend/Resume Support, Intervals, Latency, Keep Out Area Size	Prohibited Operations During Program Suspend xxx1b: May not initiate a new erase in the program suspended page size xx0xb: May not initiate a new page program anywhere (program nesting not permitted) x1xxb: May not initiate a read in the	5CH	3:0	1101b		EDH

	program suspended page size 1xxxb: The erase and program restrictions in bits 1:0 are sufficient				
	Prohibited Operations During Erase Suspend xxx0b: May not initiate a new erase anywhere (erase nesting not permitted) xx1xb: May not initiate a page program in the erase suspended erase type size x1xxb: May not initiate a read in the erase suspended erase type size 1xxxb: The erase and program restrictions in bits 5:4 are sufficient		7:4	1110b	
	Reserved	5DH	8	1b	61H
	Program Resume to Suspend Interval 12:9 count of fixed units of 64 µs Formula: program resume to suspend interval = (count + 1)*64 µs		12:9	0000b	
	Suspend in-progress program max latency 19:18 units (00b: 128ns, 01b: 1µs, 10b: 8µs, 11b: 64µs), 17:13 count Formula: suspend in-progress program max latency = (count+1)*units		15:13	011b	
	Erase Resume to Suspend Interval 23:20 count of fixed units of 64µs Formula: erase resume to suspend interval = (count + 1)*64 µs	5EH	17:16	10b	06H
			19:18	01b	
			23:20	0000b	
	Suspend in-progress erase max latency 30:29 units (00b: 128ns, 01b: 1µs, 10b: 8µs, 11b: 64µs), 28:24 count Formula: erase max latency = (count + 1)*units	5FH	28:24	10011b	33H
			30:29	01b	
	Suspend / Resume supported 0: supported 1: not supported		31	0b	
Program/Erase Suspend/Resume Instructions	Program Resume Instruction	60H	7:0	7AH	7AH
	Program Suspend Instruction	61H	15:8	75H	75H
	Resume Instruction Instruction used to resume a write or erase type operation.	62H	23:16	7AH	7AH
	Suspend Instruction Instruction used to suspend a write or erase type operation.	63H	31:24	75H	75H
Deep Powerdown and Status Register Polling Device Busy	Reserved	64H	1:0	11b	07H
	Status Register Polling Device Busy xx_xxx1b: Use of legacy polling is supported by reading the Status Register with 05h instruction and checking WIP bit[0] (0=ready; 1=busy).		7:2	000001b	
	Exit Deep Powerdown to next operation delay 14:13 units (00b: 128ns, 01b: 1µs, 10b: 8µs, 11b: 64µs), 12:8 count Formula: exit Deep Powerdown to next operation delay = (count+1)*units	65H	12:8	10011b	B3H
			14:13	01b	
	Exit Deep Powerdown Instruction		15	1010 1011b	
		66H	22:16		D5H
	Enter Deep Powerdown Instruction		23	1011 1001b	
		67H	30:24		5CH
	Deep Powerdown Supported 0: supported 1: not supported		31	0b	
Hold and WP Disable Function, Quad Enable Requirements, 4-4-4 Mode Enable/Disable Sequences, 0-4-4 Entry/Exit Methods and Support	4-4-4 mode disable sequences xxx1b: issue FFh instruction	68H	3:0	0001b	11H
	4-4-4 mode enable sequences x_xxx1b: set QE per QER description above, then issue instruction 38h		7:4	0001b	
		69H	8	0b	42H
	0-4-4 mode supported		9	1b	

	0: not supported, 1: supported				
	0-4-4 Mode Exit Method x1_xxxxb: Mode Bit[7:0] ≠ AXh		15:10	010000b	
	0-4-4 Mode Entry Method x1xxb: Mode Bit[7:0]=AXh	6AH	19:16	0100b	44H
	Quad Enable Requirements (QER) 100b: QE is bit 1 of status register 2. It is set via Write Status with two data bytes where bit 1 of the second byte is one. It is cleared via Write Status with two data bytes where bit 1 of the second byte is zero. In contrast to the 001b code, writing one byte to the status register does not modify status register 2.		22:20	100b	
	HOLD or RESET Disable 1: set bit 4 of the Non-Volatile Extended Configuration Register = 0 to disable HOLD or RESET 0: above feature is not supported		23	0b	
	Reserved	6BH	31:24	FFH	FFH
32-bit Address Entry/Exit Methods and Support, Soft Reset and Rescue Sequences, Volatile and Nonvolatile Status Register Support	Volatile or Non-Volatile Register and Write Enable Instruction for Status Register 1 xxx_1xxxb: Non-Volatile/Volatile status register 1 powers-up to last written value in the non-volatile status register, use instruction 06h to enable write to non-volatile status register. Volatile status register may be activated after power-up to override the non-volatile status register, use instruction 50h to enable write and activate the volatile status register.	6CH	6:0	0001000b	88H
	Reserved		7	1b	
	Soft Reset and Rescue Sequence Support x1_xxxxb: issue reset enable instruction 66h, then issue reset instruction 99h. The reset enable, reset sequence may be issued on 1, 2, or 4 wires depending on the device operating mode.	6DH	13:8	010000b	50H
	Exit 4-Byte Addressing xx_xxxx_xxx1b: issue instruction E9h to exit 4-Byte address mode (write enable instruction 06h is not required)		15:14	00 0000 0001b	
		6EH	23:16		00H
	Enter 4-Byte Addressing xxxx_xxx1b: issue instruction B7h (preceding write enable not required)	6FH	31:24	0000 0001b	01H

Table 7.3.11.c. Parameter Table (1): Boya Device Flash Parameter Tables

Description	Comment	Add(H) (Byte)	DW Add (Bit)	Data	Data
Vcc Supply Maximum Voltage	2000H=2.000V 2700H=2.700V 3600H=3.600V	91H:90H	15:00	3600H	3600H
Vcc Supply Minimum Voltage	1650H=1.650V 2250H=2.250V 2350H=2.350V 2700H=2.700V	93H:92H	31:16	2700H	2700H
HW Reset# pin	0=not support 1=support	95H:94H	00	1b	F99FH
HW Hold# pin	0=not support 1=support		01	1b	
Deep Power Down Mode	0=not support 1=support		02	1b	
SW Reset	0=not support 1=support		03	1b	
SW Reset Opcode	Should be issue Reset Enable(66H)before Reset cmd.		11:04	99H	
Program Suspend/Resume	0=not support 1=support		12	1b	
Erase Suspend/Resume	0=not support 1=support		13	1b	
Unused			14	1b	
Wrap-Around Read mode	0=not support 1=support		15	1b	
Wrap-Around Read mode Opcode		96H	23:16	77H	77H
Wrap-Around Read data length	08H:support 8B wrap-around read 16H:8B&16B 32H:8B&16B&32B 64H:8B&16B&32B&64B	97H	31:24	64H	64H
Individual block lock	0=not support 1=support	9BH:98H	00	0b	CBFCH
Individual block lock bit(Volatile/Nonvolatile)	0=Volatile 1=Nonvolatile		01	0b	
Individual block lock Opcode			09:02	FFH	
Individual block lock Volatile protect bit default protect status	0=protect 1=unprotect		10	0b	
Secured OTP	0=not support 1=support		11	1b	
Read Lock	0=not support 1=support		12	0b	
Permanent Lock	0=not support 1=support		13	0b	
Unused			15:14	11b	
Unused			31:16	FFFFH	FFFFH

Table 7.3.11.d. Parameter Table (2): JEDEC 4-byte Address Instruction Parameter Header and Table

Description	Comment	Add(H) (Byte)	DW Add (Bit)	Data	Data
Support for (1-1-1) READ Command, Instruction=13h	0: Not supported 1: Supported	C0H	0	1b	FFH
Support for (1-1-1) FAST_READ Command, Instruction=0Ch	0: Not supported 1: Supported		1	1b	
Support for (1-1-2) FAST_READ Command, Instruction=3Ch	0: Not supported 1: Supported		2	1b	
Support for (1-2-2) FAST_READ Command, Instruction=BCh	0: Not supported 1: Supported		3	1b	
Support for (1-1-4) FAST_READ Command, Instruction=6Ch	0: Not supported 1: Supported		4	1b	
Support for (1-4-4) FAST_READ Command, Instruction=ECh	0: Not supported 1: Supported		5	1b	
Support for (1-1-1) Page Program Command, Instruction=12h	0: Not supported 1: Supported		6	1b	
Support for (1-1-4) Page Program Command, Instruction=34h	0: Not supported 1: Supported		7	1b	
Support for (1-4-4) Page Program Command, Instruction=3Eh	0: Not supported 1: Supported	C1H	8	0b	8EH
Support for Erase Command – Type 1 size, Instruction lookup in next Dword	0: Not supported 1: Supported		9	1b	
Support for Erase Command – Type 2 size, Instruction lookup in next Dword	0: Not supported 1: Supported		10	1b	
Support for Erase Command – Type 3 size, Instruction lookup in next Dword	0: Not supported 1: Supported		11	1b	
Support for Erase Command – Type 4 size, Instruction(DCh 256 kbyte erase) lookup in next Dword	0: Not supported 1: Supported		12	0b	
Support for (1-1-1) DTR_Read Command, Instruction=0Eh(Boya 0Eh is for DTR wrap read, quadio)	0: Not supported 1: Supported		13	0b	
Support for (1-2-2) DTR_Read Command, Instruction=BEh	0: Not supported 1: Supported		14	0b	
Support for (1-4-4) DTR_Read Command, Instruction=EEh	0: Not supported 1: Supported		15	1b	
Support for volatile individual sector lock Read command, Instruction=E0h	0: Not supported 1: Supported	C2H	16	0b	00H
Support for volatile individual sector lock Write command, Instruction=E1h	0: Not supported 1: Supported		17	0b	
Support for non-volatile individual sector lock read command, Instruction=E2h	0: Not supported 1: Supported		18	0b	
Support for non-volatile individual sector lock write command, Instruction=E3h(Boya E3h is for oct read)	0: Not supported 1: Supported		19	0b	
Support for (1-1-8) FAST_READ Command, Instruction=7Ch	0: Not supported 1: Supported		20	0b	
Support for (1-8-8) FAST_READ Command, Instruction=CCh	0: Not supported 1: Supported		21	0b	
Support for (1-8-8) DTR_READ Command, Instruction=FDh	0: Not supported 1: Supported		22	0b	
Support for (1-1-8) Page Program Command, Instruction=84h	0: Not supported 1: Supported		23	0b	
Support for (1-8-8) Page Program Command, Instruction=8Eh	0: Not supported 1: Supported	C3H	24	0b	FEH
Reserved			31:25	all 1's	
nstruction for Erase Type 1		C4H	7:0	21H	21H
Instruction for Erase Type 2		C5H	15:8	5CH	5CH
Instruction for Erase Type 3		C6H	23:16	DCH	DCH
Instruction for Erase Type 4(DCh 256 kbyte erase)		C7H	31:24	FFH	FFH

7.4 Program and Erase Instructions

7.4.1 Page Program (02H)

The Page Program instruction is for programming the memory. A Write Enable instruction must previously have been executed to set the Write Enable Latch bit before sending the Page Program instruction.

See ***Figure 116-Figure 119***, the Page Program instruction is entered by driving /CS Low, followed by the instruction code, 3-byte address and at least one data byte on SI. If the 8 least significant address bits (A7-A0) are not all zero, all transmitted data that goes beyond the end of the current page are programmed from the start address of the same page (from the address whose 8 least significant bits (A7-A0) are all zero). /CS must be driven low for the entire duration of the sequence. The Page Program instruction sequence: /CS goes low-> sending Page Program instruction ->3-byte/4-byte address on SI ->at least 1 byte data on SI-> /CS goes high.

If more than 256 bytes are sent to the device, previously latched data are discarded and the last 256 data bytes are guaranteed to be programmed correctly within the same page. If less than 256 data bytes are sent to device, they are correctly programmed at the requested addresses without having any effects on the other bytes of the same page. /CS must be driven high after the eighth bit of the last data byte has been latched in; otherwise the Page Program instruction is not executed.

As soon as /CS is driven high, the self-timed Page Program cycle (whose duration is tPP) is initiated. While the Page Program cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Page Program cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch bit is reset.

A Page Program instruction applied to a page which is protected by the Block Protect (BP4, BP3, BP2, BP1, BP0) bits (see ***Table 7-Table 8***)、Individual Block/Sector Lock bit are not executed.

Figure 116. Page Program Sequence Diagram (SPI Mode/3-Byte Address Mode)

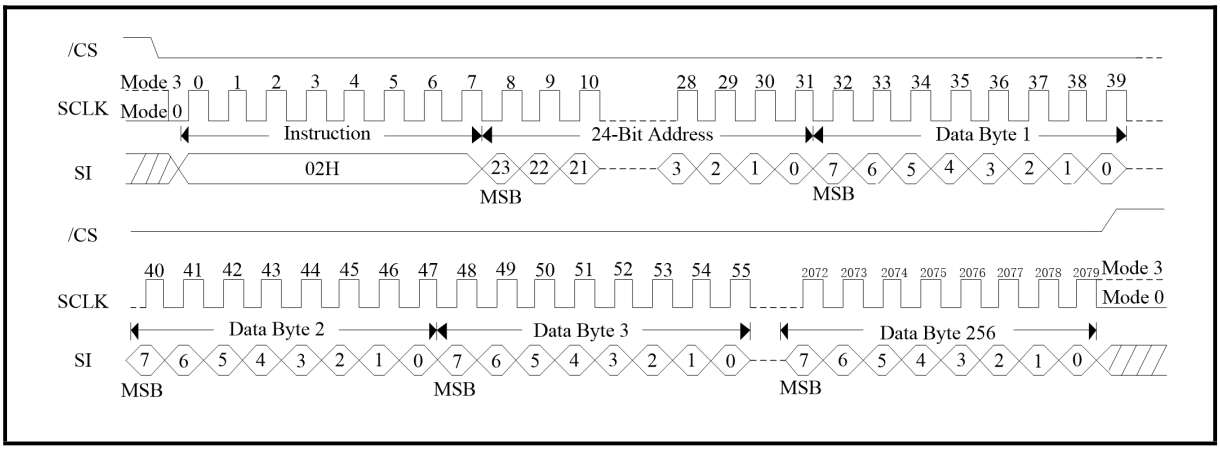


Figure 117. Page Program Sequence Diagram (SPI Mode/4-Byte Address Mode)

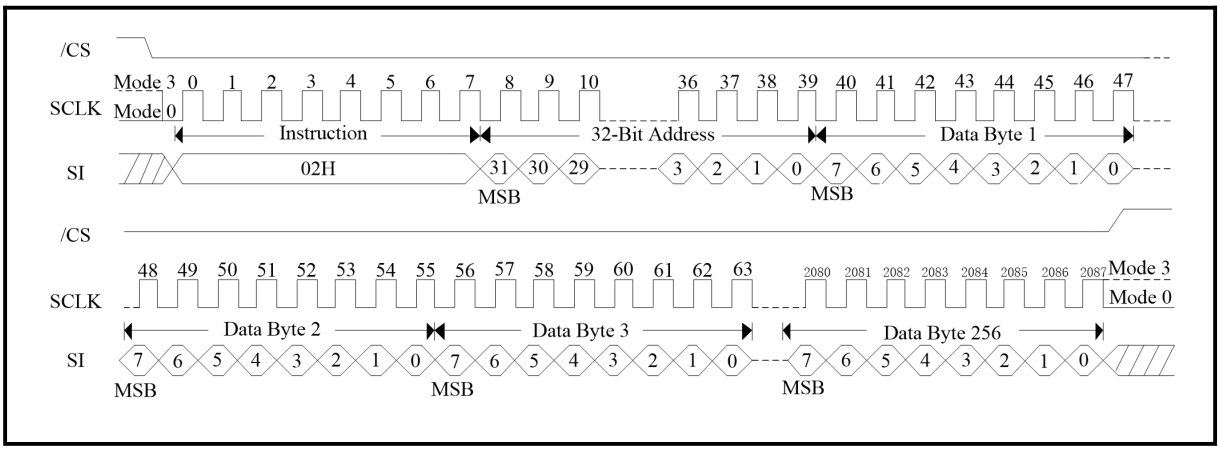


Figure 118. Page Program Sequence Diagram (QPI Mode/3-Byte Address Mode)

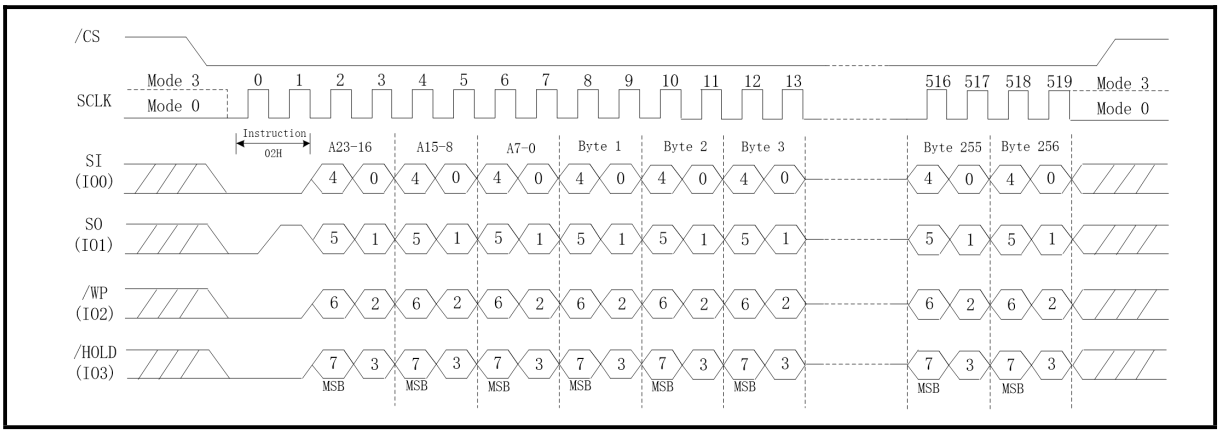
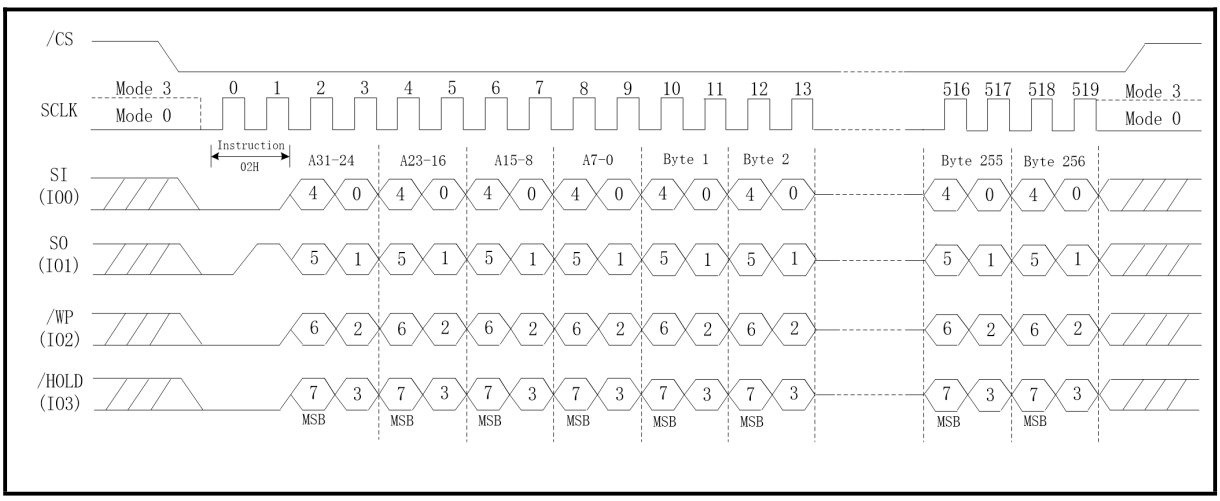


Figure 119. Page Program Sequence Diagram (QPI Mode/4-Byte Address Mode)



7.4.2 Page Program with 4-Byte Address (12H)

The Page Program with 4-Byte Address instruction is similar to the Page Program instruction except that it requires 32-bit address instead of 24-bit address. No matter the device is operating in 3-Byte Address Mode or 4-byte Address Mode, the Page Program with 4-Byte Address instruction will always require 32- bit address to access the entire 256Mb memory.

Figure 120. Page Program with 4-Byte Address (SPI Mode)

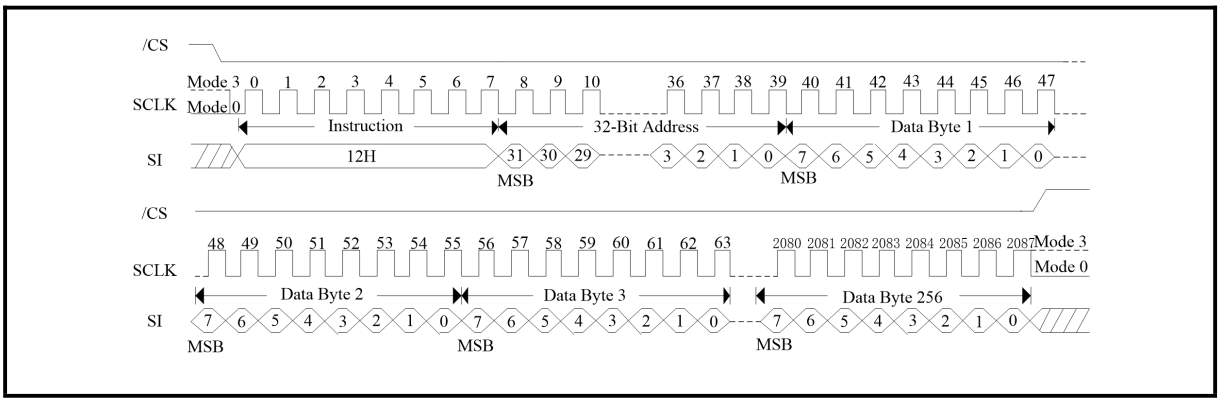
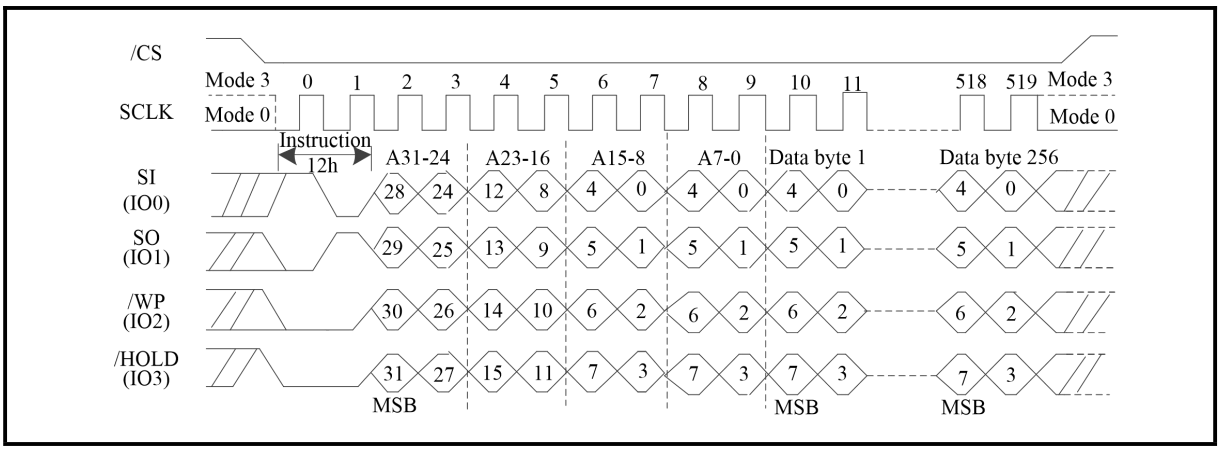


Figure 121. Page Program with 4-Byte Address (QPI Mode)



7.4.3 Quad Page Program (32H)

The Quad Page Program instruction is for programming the memory using for pins: IO0, IO1, IO2 and IO3. To use Quad Page Program the Quad enable in status register Bit9 must be set (QE=1). A Write Enable instruction must previously have been executed to set the Write Enable Latch bit before sending the Page Program instruction. The Quad Page Program instruction is entered by driving /CS Low, followed by the instruction code (32H), three address bytes and at least one data byte on IO pins. The Quad Enable bit (QE) of Status Register must be set to enable.

The instruction sequence is shown in ***Figure 122-Figure 123***. If more than 256 bytes are sent to the device, previously latched data are discarded and the last 256 data bytes are guaranteed to be programmed correctly within the same page. If less than 256 data bytes are sent to device, they are correctly programmed at the requested addresses without having any effects on the other bytes of the same page. /CS must be driven high after the eighth bit of the last data byte has been latched in; otherwise the Quad Page Program instruction is not executed.

As soon as /CS is driven high, the self-timed Quad Page Program cycle (whose duration is tPP) is initiated. While the Quad Page Program cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Quad Page Program cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch bit is reset. A Quad Page Program instruction applied to a page which is protected by the Block Protect (BP4, BP3, BP2, BP1, BP0) bits (see ***Table 7-Table 8***) is not executed

Figure 122. Quad Page Program Sequence Diagram (SPI Mode only/3-Byte Address Mode)

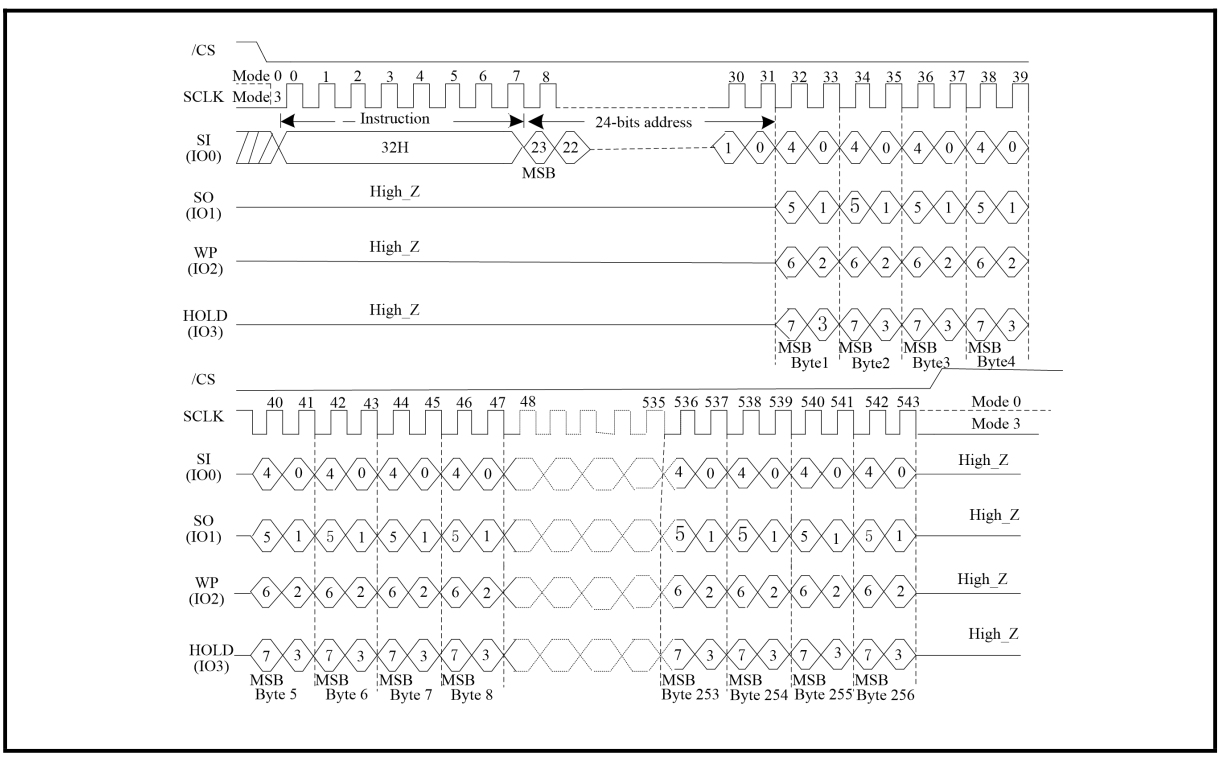
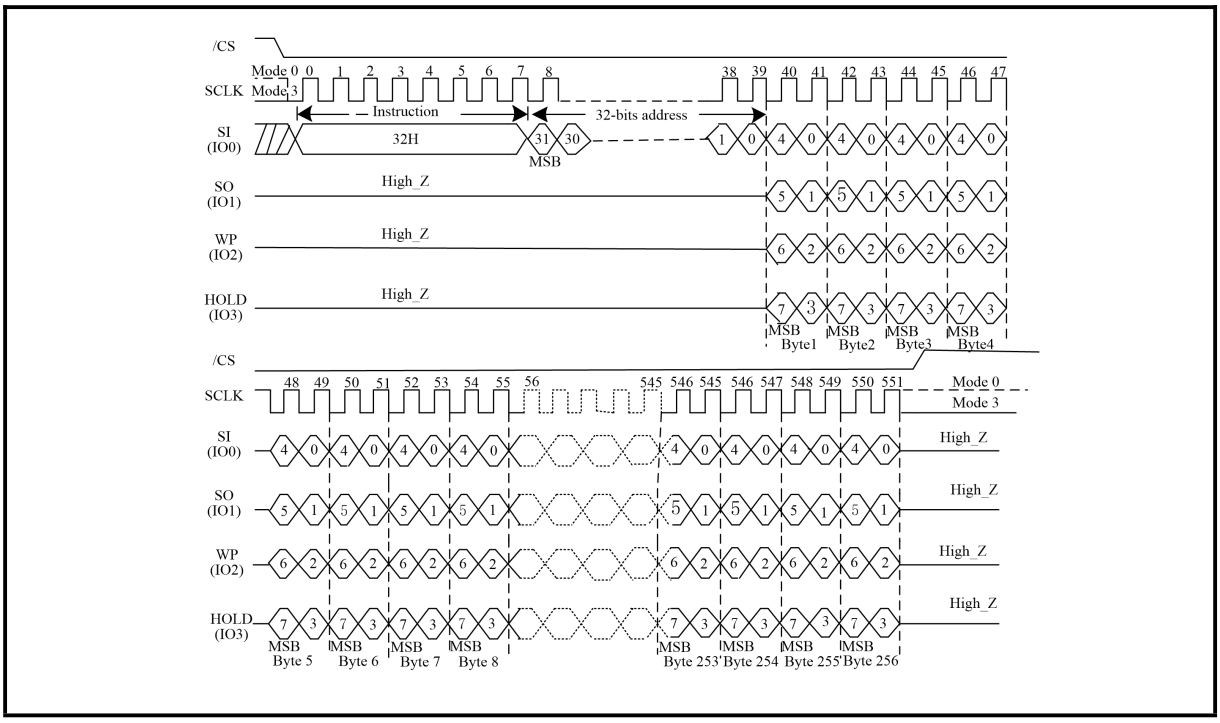


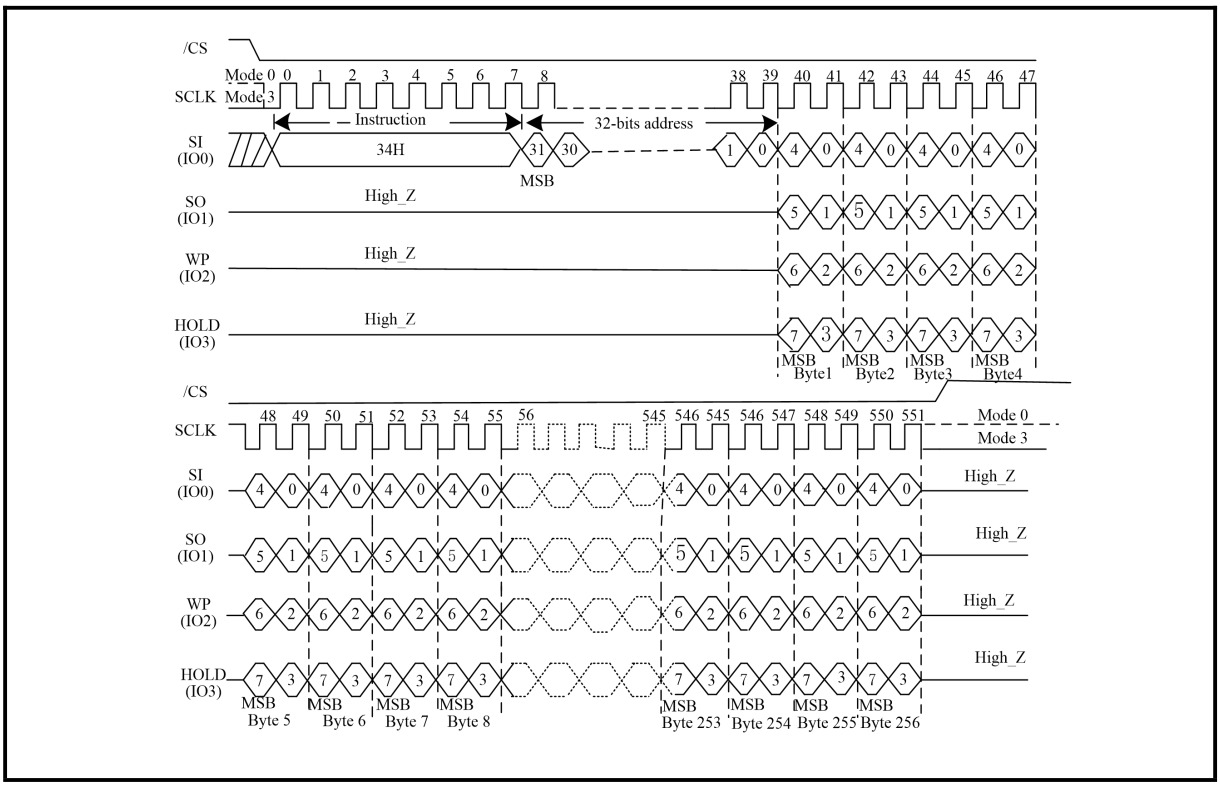
Figure 123. Quad Page Program Sequence Diagram (SPI Mode only/4-Byte Address Mode)



7.4.4 Quad Input Page Program with 4-Byte Address (34H)

The Quad Input Page Program with 4-Byte Address instruction is similar to the Quad Input Page Program instruction except that it requires 32-bit address instead of 24-bit address. No matter the device is operating in 3-Byte Address Mode or 4-byte Address Mode, the Quad Input Page Program with 4-Byte Address instruction will always require 32-bit address to access the entire 256Mb memory. The Quad Enable bit (QE) of Status Register must be set to enable.

Figure 124. Quad Page Program with 4-Byte Address Sequence Diagram (SPI Mode only)



7.4.5 Sector Erase (20H)

The Sector Erase instruction is for erasing the all data of the chosen sector. A Write Enable instruction must previously have been executed to set the Write Enable Latch bit. The Sector Erase instruction is entered by driving /CS low, followed by the instruction code, and 3-address byte on SI. Any address inside the sector is a valid address for the Sector Erase instruction. /CS must be driven low for the entire duration of the sequence.

See ***Figure 125-Figure 128***, The Sector Erase instruction sequence: /CS goes low-> sending Sector Erase instruction-> 3-byte/4-byte address on SI ->/CS goes high. /CS must be driven high after the eighth bit of the last address byte has been latched in; otherwise the Sector Erase instruction is not executed. As soon as /CS is driven high, the self-timed Sector Erase cycle (whose duration is tSE) is initiated. While the Sector Erase cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Sector Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch bit is reset. A Sector Erase instruction applied to a sector which is protected by the Block Protect (BP4, BP3, BP2, BP1, BP0) bits (see ***Table 7-Table 8***) is not executed.

Figure 125. Sector Erase Sequence Diagram (SPI Mode/3-Byte Address Mode)

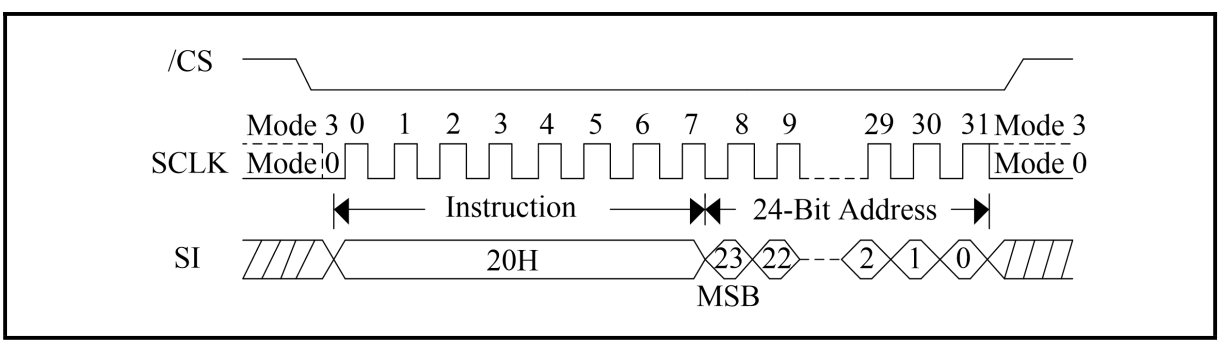


Figure 126. Sector Erase Sequence Diagram (SPI Mode/4-Byte Address Mode)

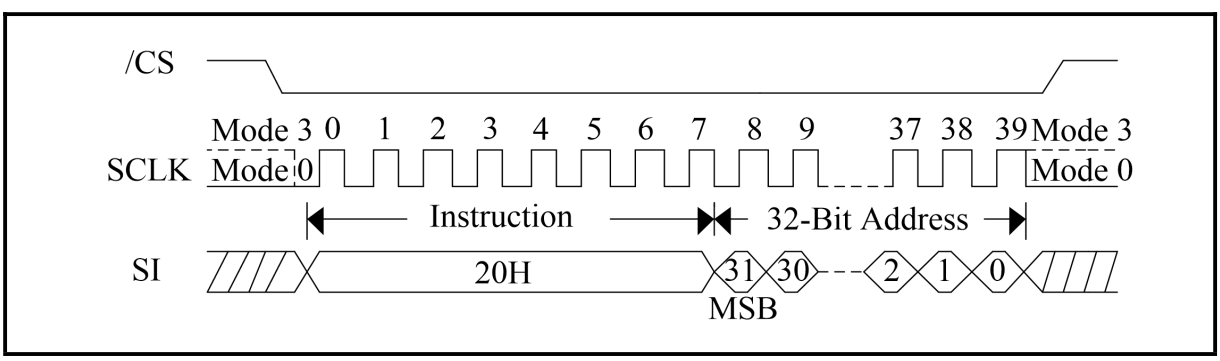


Figure 127. Sector Erase Sequence Diagram (QPI Mode/3-Byte Address Mode)

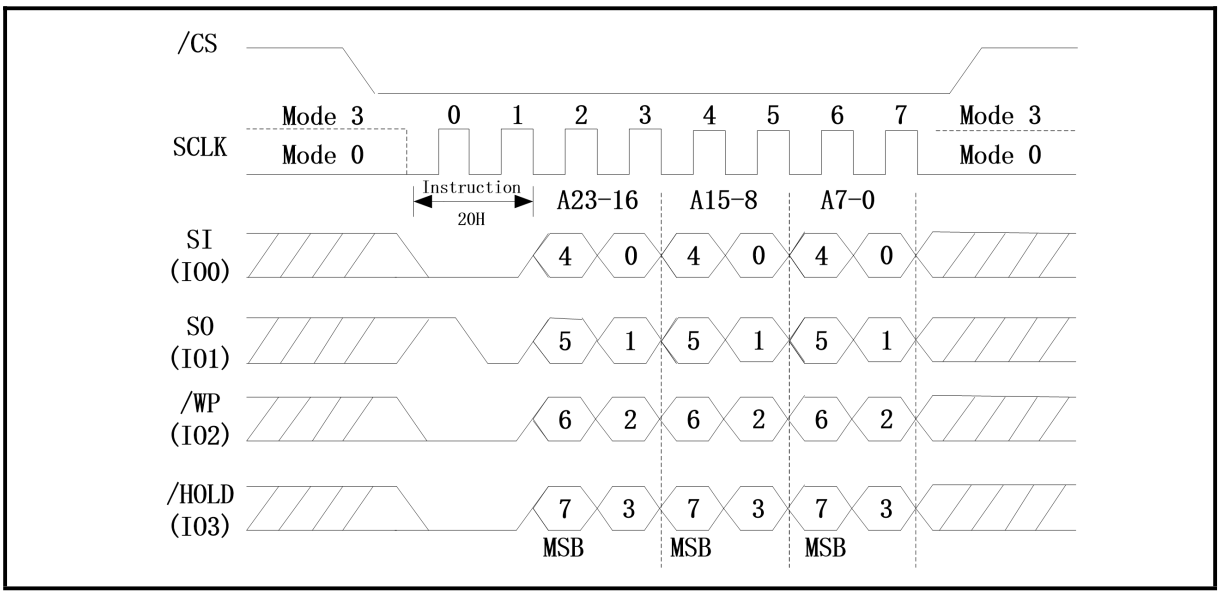
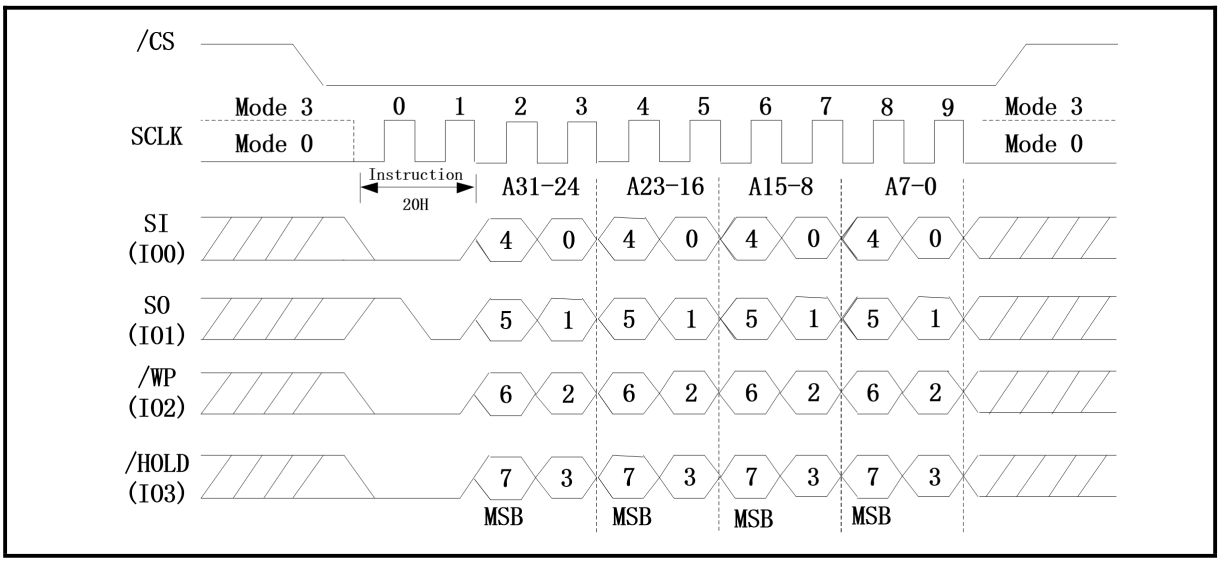


Figure 128. Sector Erase Sequence Diagram (QPI Mode/4-Byte Address Mode)



7.4.6 Sector Erase with 4-Byte Address (21H)

The Sector Erase with 4-Byte Address instruction is similar to the Sector Erase instruction except that it requires 32-bit address instead of 24-bit address. No matter the device is operating in 3-Byte Address Mode or 4-byte Address Mode, the Sector Erase with 4-Byte Address instruction will always require 32-bit address to access the entire 256Mb memory.

Figure 129. Sector Erase with 4-Byte Address (SPI Mode)

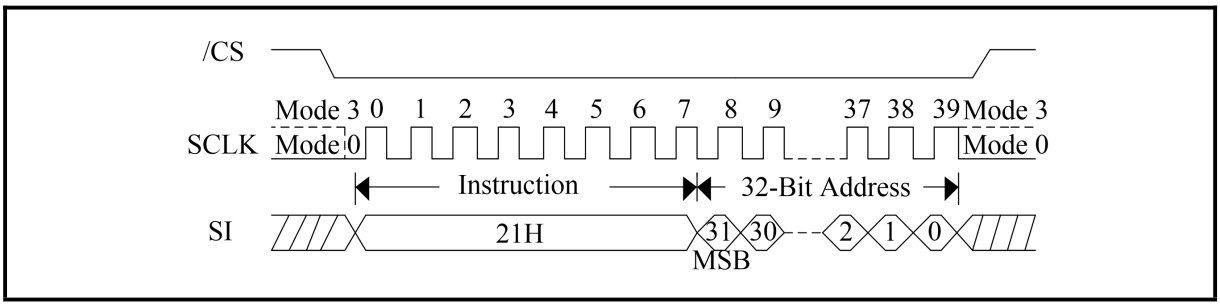
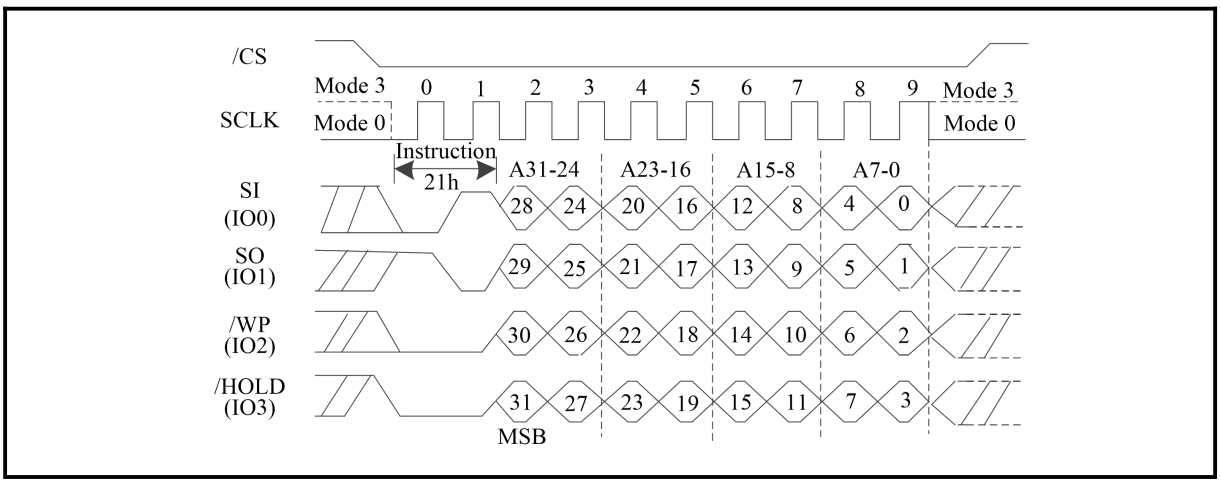


Figure 130. Sector Erase with 4-Byte Address (QPI Mode)



7.4.7 32KB Block Erase (52H)

The 32KB Block Erase instruction is for erasing the all data of the chosen block. A Write Enable instruction must previously have been executed to set the Write Enable Latch bit. The 32KB Block Erase instruction is entered by driving /CS low, followed by the instruction code, and 3-byte/4-byte address on SI. Any address inside the block is a valid address for the 32KB Block Erase instruction. /CS must be driven low for the entire duration of the sequence.

See ***Figure 131-Figure 134***, the 32KB Block Erase instruction sequence: /CS goes low ->sending 32KB Block Erase instruction ->3-byte/4-byte address on SI ->/CS goes high. /CS must be driven high after the eighth bit of the last address byte has been latched in; otherwise the 32KB Block Erase instruction is not executed. As soon as /CS is driven high, the self-timed Block Erase cycle (whose duration is tBE) is initiated. While the Block Erase cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Block Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch bit is reset. A 32KB Block Erase instruction applied to a block which is protected by the Block Protect (BP4, BP3, BP2, BP1, BP0) bits (see ***Table 7-Table 8***) is not executed.

Figure 131. 32KB Block Erase Sequence Diagram (SPI Mode/3-Byte Address Mode)

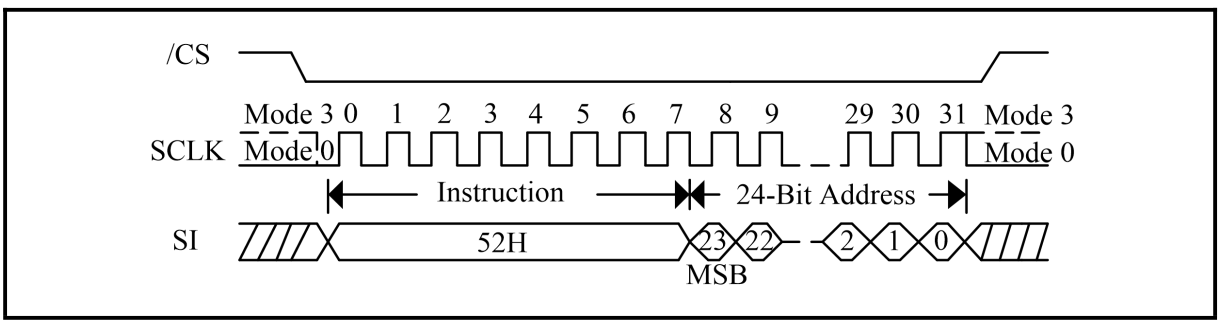


Figure 132. 32KB Block Erase Sequence Diagram (SPI Mode/4-Byte Address Mode)

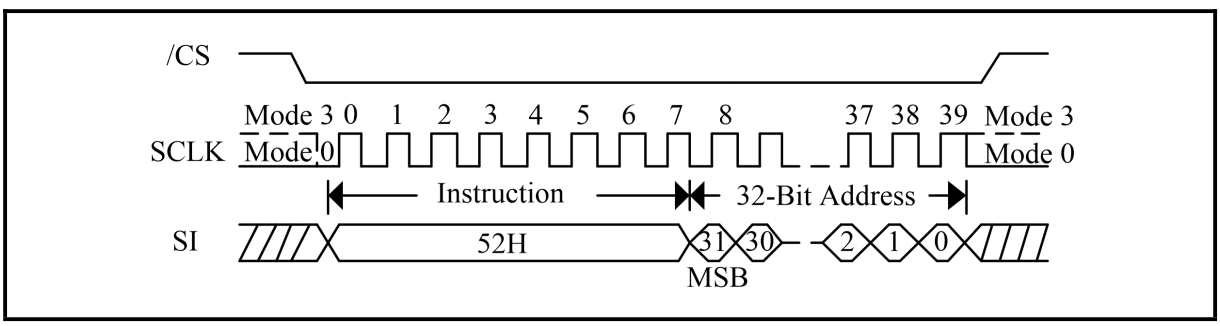


Figure 133. 32KB Block Erase Sequence Diagram (QPI Mode/3-Byte Address Mode)

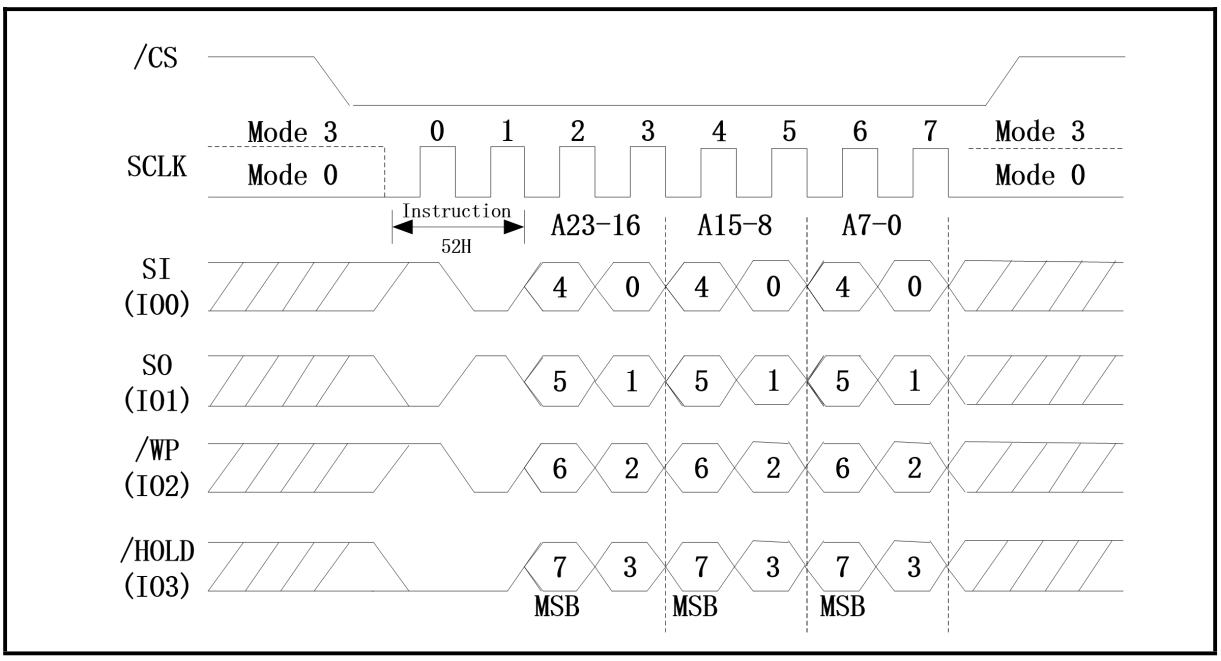
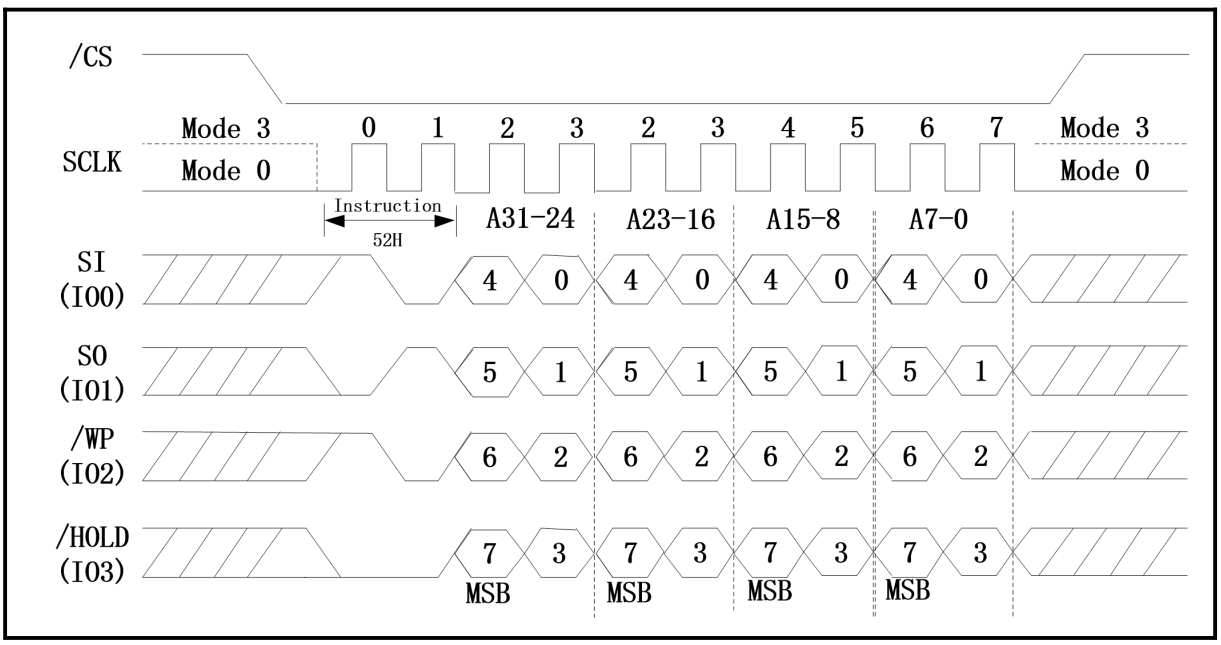


Figure 134. 32KB Block Erase Sequence Diagram (QPI Mode/4-Byte Address Mode)



7.4.8 32KB Block Erase with 4-Byte Address (5CH)

The 32KB Block Erase with 4-Byte Address instruction is similar to the 32KB Block Erase instruction except that it requires 32-bit address instead of 24-bit address. No matter the device is operating in 3-Byte Address Mode or 4-byte Address Mode, the 32KB Block Erase with 4-Byte Address instruction will always require 32-bit address to access the entire 256Mb memory.

Figure 135. 32KB Block Erase with 4-Byte Address (SPI Mode)

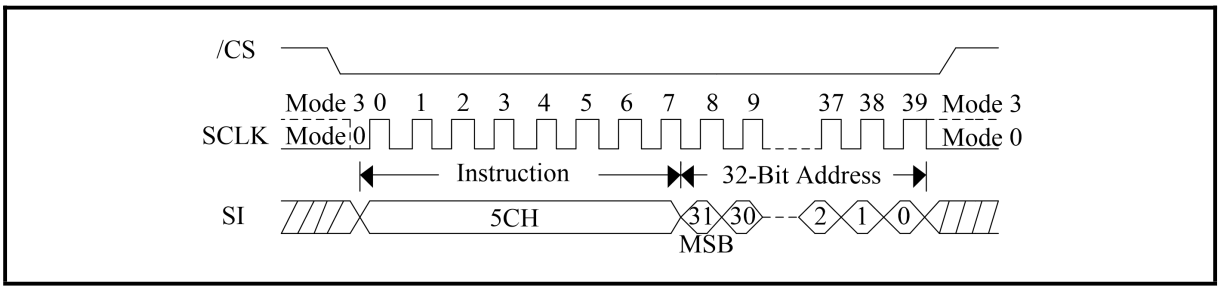
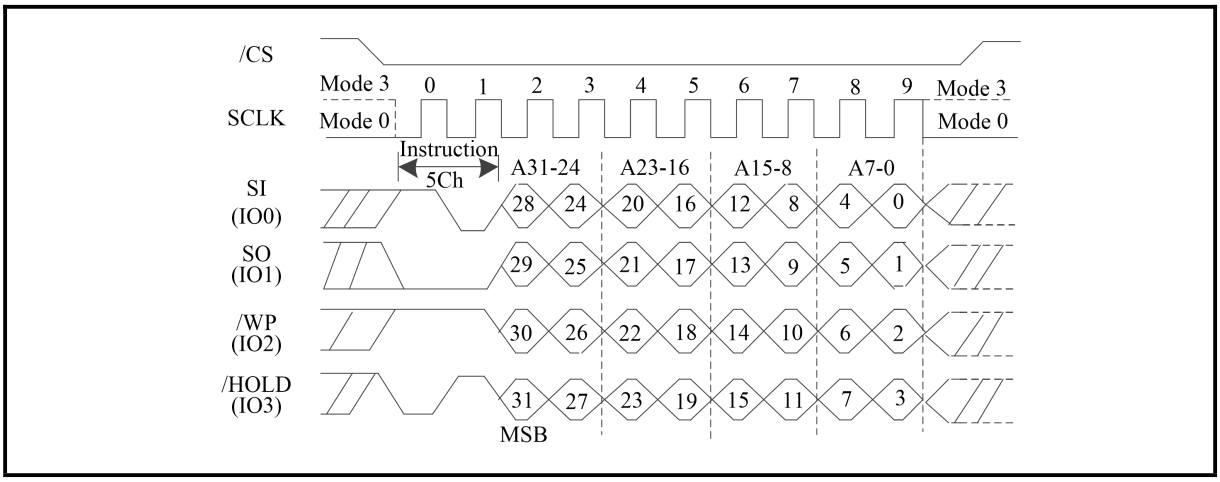


Figure 136. 32KB Block Erase with 4-Byte Address (QPI Mode)



7.4.9 64KB Block Erase (D8H)

The 64KB Block Erase instruction is for erasing the all data of the chosen block. A Write Enable instruction must previously have been executed to set the Write Enable Latch bit. The 64KB Block Erase instruction is entered by driving /CS low, followed by the instruction code, and 3-byte/4-byte address on SI. Any address inside the block is a valid address for the 64KB Block Erase instruction. /CS must be driven low for the entire duration of the sequence.

See ***Figure 137-Figure 140***, the 64KB Block Erase instruction sequence: /CS goes low sending 64KB Block Erase instruction 3-byte/4-byte address on SI /CS goes high. /CS must be driven high after the eighth bit of the last address byte has been latched in; otherwise the 64KB Block Erase instruction is not executed. As soon as /CS is driven high, the self-timed Block Erase cycle (whose duration is tBE) is initiated. While the Block Erase cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Block Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch bit is reset. A 64KB Block Erase instruction applied to a block which is protected by the Block Protect (BP4, BP3, BP2, BP1, BP0) bits (see ***Table 7-Table 8***) is not executed.

Figure 137. 64KB Block Erase Sequence Diagram (SPI Mode/3-Byte Address Mode)

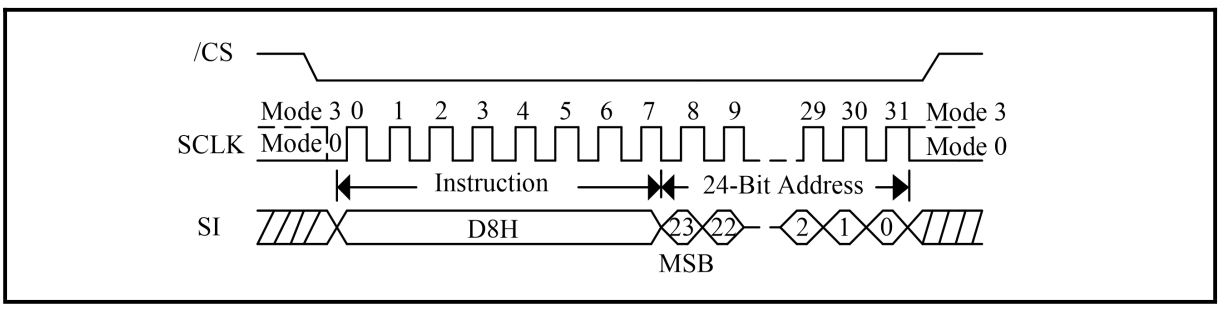


Figure 138. 64KB Block Erase Sequence Diagram (SPI Mode/4-Byte Address Mode)

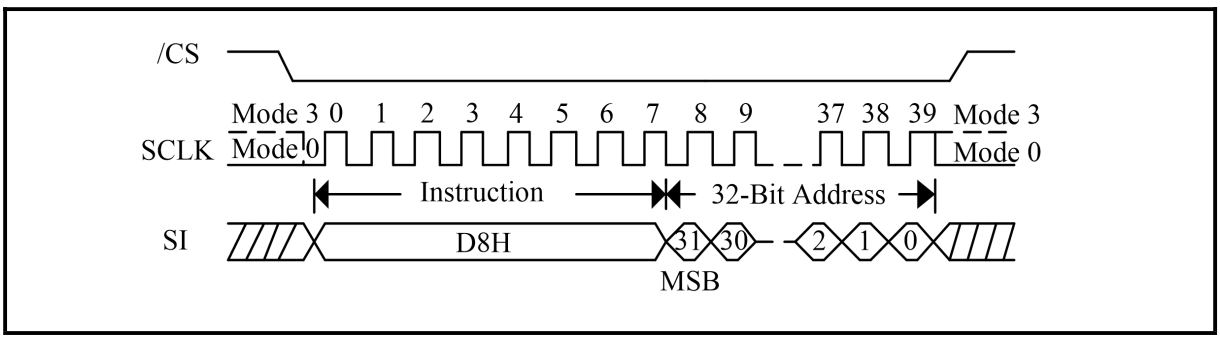


Figure 139. 64KB Block Erase Sequence Diagram (QPI Mode/3-Byte Address Mode)

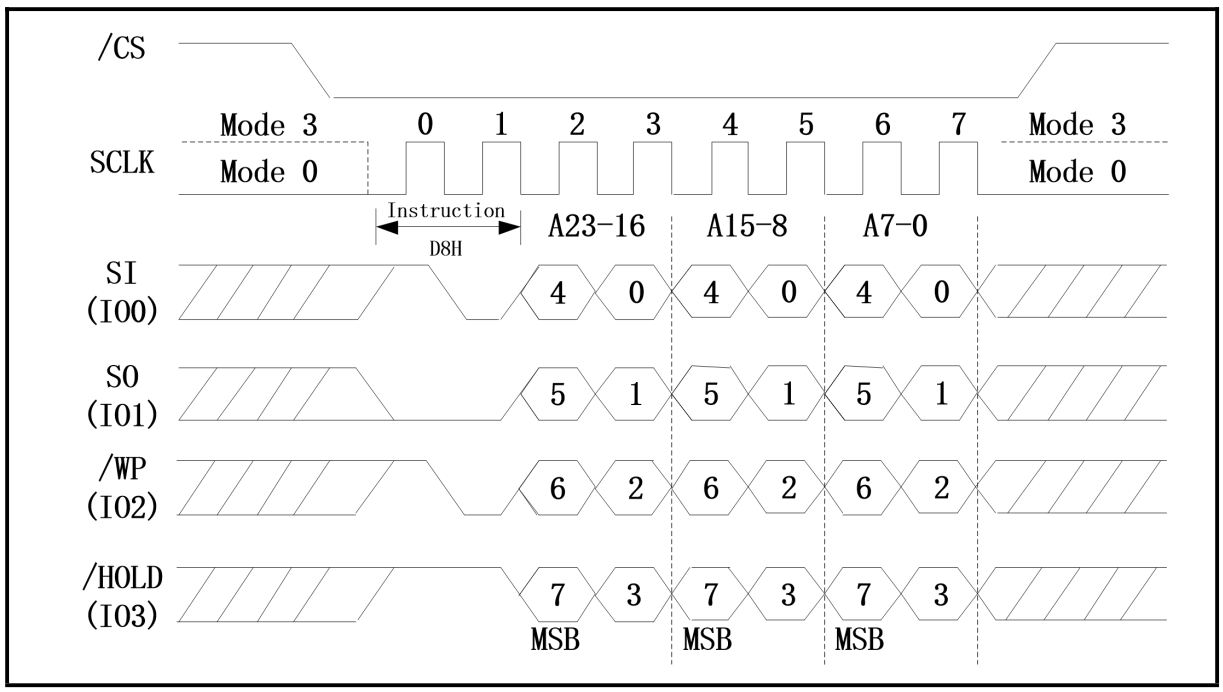
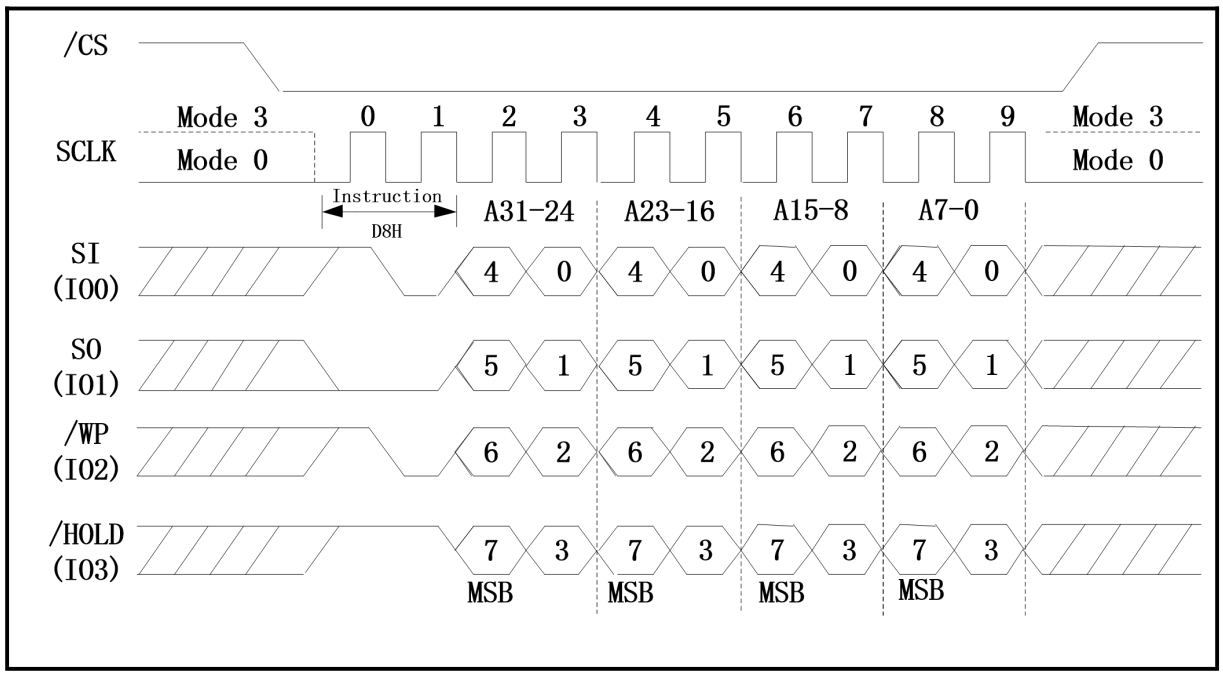


Figure 140. 64KB Block Erase Sequence Diagram (QPI Mode/4-Byte Address Mode)



7.4.10 64KB Block Erase with 4-Byte Address (DCH)

The 64KB Block Erase with 4-Byte Address instruction is similar to the 64KB Block Erase instruction except that it requires 32-bit address instead of 24-bit address. No matter the device is operating in 3-Byte Address Mode or 4-byte Address Mode, the 64KB Block Erase with 4-Byte Address instruction will always require 32-bit address to access the entire 256Mb memory.

Figure 141. 64KB Block Erase with 4-Byte Address (SPI Mode)

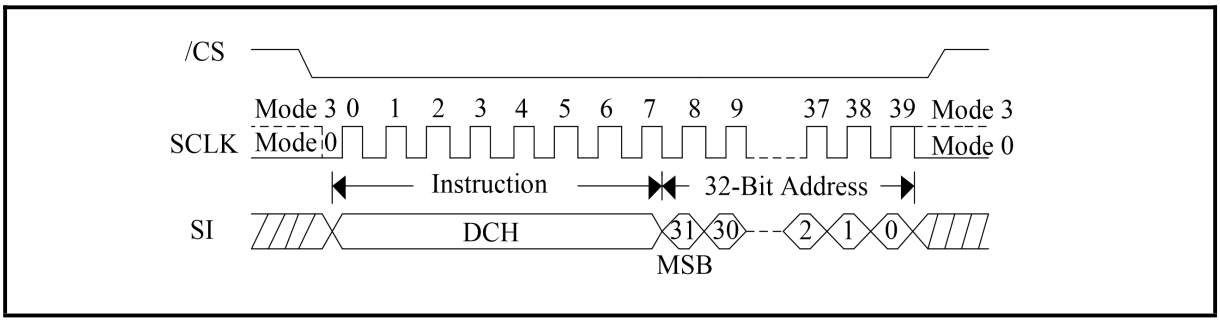
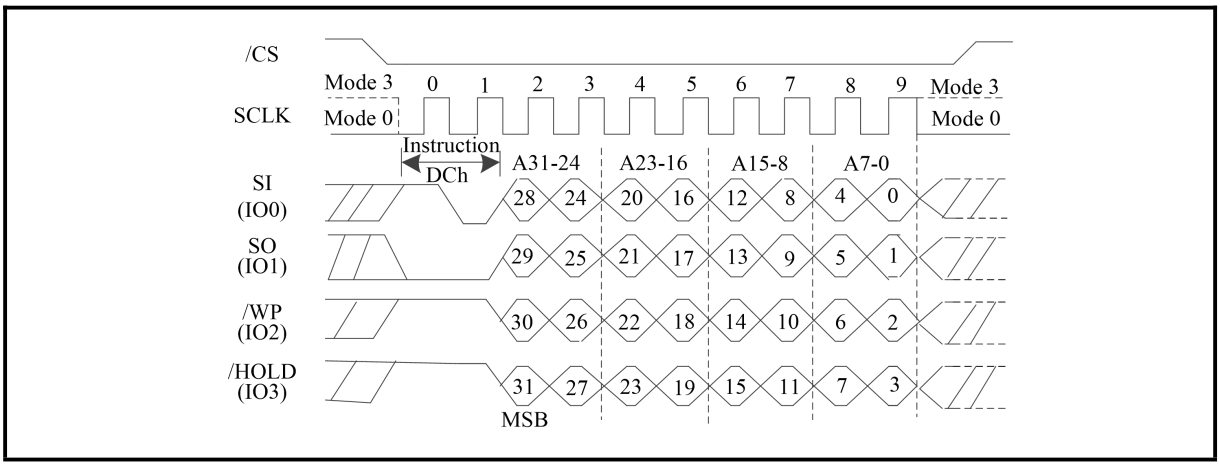


Figure 142. 64KB Block Erase with 4-Byte Address (QPI Mode)



7.4.11 Chip Erase (60/C7H)

The Chip Erase instruction sets all memory within the device to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Chip Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the /CS pin low and shifting the instruction code “C7h” or “60h”. The Chip Erase instruction sequence is shown in ***Figure 143-Figure 144***.

The /CS pin must be driven high after the eighth bit has been latched. If this is not done the Chip Erase instruction will not be executed. After /CS is driven high, the self-timed Chip Erase instruction will commence for a time duration of tCE. While the Chip Erase cycle is in progress, the Read Status Register instruction may still be accessed to check the status of the WIP bit.

The WIP bit is a 1 during the Chip Erase cycle and becomes a 0 when finished and the device is ready to accept other Instructions again. After the Chip Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Chip Erase instruction is executed only if all Block Protect (BP2, BP1, and BP0) bits are 0.The Chip Erase instruction is ignored if one or more sectors are protected.

Figure 143. Chip Erase Sequence Diagram (SPI Mode)

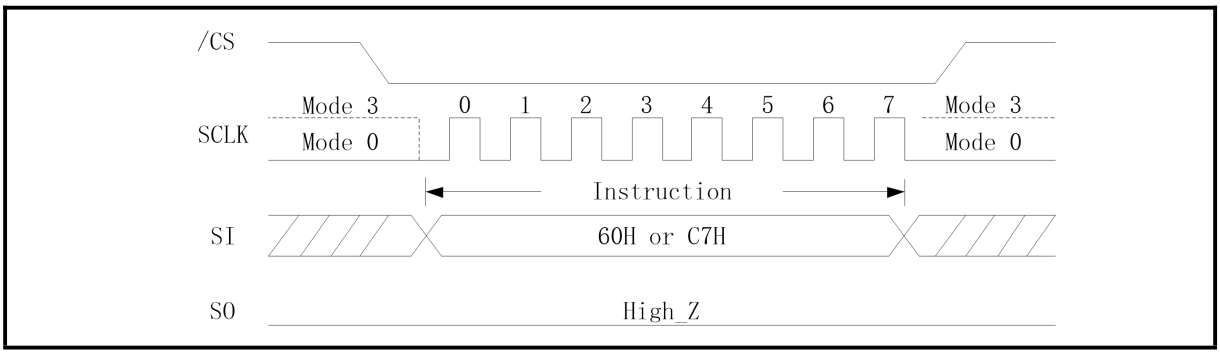
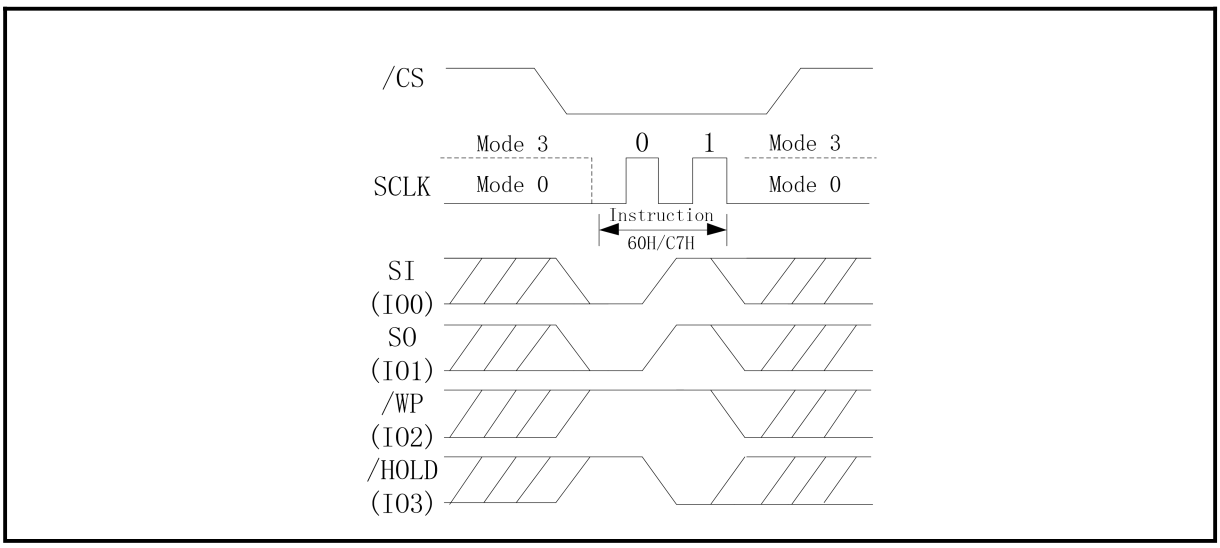


Figure 144. Chip Erase Sequence Diagram (QPI Mode)



7.4.12 Program/Erase Suspend (75H)

The Program/Erase Suspend instruction “75h” allows the system to interrupt a Page Program or a Sector/32K/64K Block Erase operation (The time between the Program/Erase instruction and the Program/Erase Suspend instruction is tPS/tES). After the program operation has entered the suspended state, the memory array can be read except for the page being programmed. And after the erase operation has entered the suspended state, the memory array can be read or programed except for the sector/32kb block/64kb block being erased. Write status register operation can't be suspended. The Program/Erase Suspend instruction sequence is shown in ***Figure 145-Figure 146***.

Table 17. Readable or Erasable Area of Memory While a Program Operation is Suspended

Suspended operation	Readable Region Of Memory Array
Page Program	All but the Page being programmed
Page Program with 4-Byte Address	All but the Page being programmed
Quad Page Program	All but the Page being programmed
Quad Page Program with 4-Byte Address	All but the Page being programmed

Table 18. Readable or Programmable Area of Memory While an Erase Operation is Suspended

Suspended operation	Readable Region or Programmable Of Memory Array
Sector Erase(4KB)	All but the Sector being Erased
Sector Erase with 4-Byte Address (4KB)	All but the Sector being Erased
Block Erase(32KB)	All but the 32kb Block being Erased
Block Erase with 4-Byte Address (32KB)	All but the 32kb Block being Erased
Block Erase(64KB)	All but the 64kb Block being Erased
Block Erase with 4-Byte Address (64KB)	All but the 64kb Block being Erased

When the Serial NOR Flash receives the Suspend instruction, there is a latency of tPSL or tESL before the Write Enable Latch (WEL) bit clears to “0” and the SUS2 or SUS1 sets to “1”, after which the device is ready to accept one of the instructions listed in "Table Acceptable Instructions During Program/Erase Suspend after tPSL/tESL" (e.g. FAST READ). Refer to " AC Characteristics" for tPSL and tESL timings. "Table Acceptable instructions During Suspend (tPSL/tESL not required)" lists the Instructions for which the tPSL and tESL latencies do not apply. For example, “05h”, “66h” and “99h” can be issued at any time after the Suspend instruction.

Status Register bit 15 (SUS2) and bit 10 (SUS1) can be read to check the suspend status. The SUS2 (Program Suspend Bit) sets to “1” when a program instruction is suspended. The SUS1 (Erase Suspend Bit) sets to “1” when an erase operation is suspended. The SUS2 or SUS1 clears to “0” when the program or erase instruction is resumed.

Table 19. Acceptable instructions During Program/Erase Suspend after tPSL/tESL

Instruction Name	Instruction code	Suspend Type	
		Program Suspend	Erase Suspend
Write Enable	06h	*	*
Write Disable	04h	*	*
Read Extended Address Register	C8H	*	*
Write Extended Address Register	C5H	*	*
Enter 4-Byte Address Mode	B7h	*	*
Exit 4-Byte Address Mode	E9h	*	*
Enter QPI Mode	38h	*	*
Exit QPI Mode	FFh	*	*
Read Extended Address Register	C8h	*	*

Instruction Name	Instruction code	Suspend Type	
		Program Suspend	Erase Suspend
Read Data	03h	*	*
Read Data with 4-Byte Address	13h	*	*
Fast Read	0Bh	*	*
Fast Read with 4-Byte Address	0Ch	*	*
Dual Output Fast Read	3Bh	*	*
Fast Read Dual Output with 4-Byte Address	3Ch	*	*
Quad Output Fast Read	6Bh	*	*
Fast Read Quad Output with 4-Byte Address	6Ch	*	*
Dual I/O Fast Read	BBh	*	*
Fast Read Dual I/O with 4-Byte Address	BCh	*	*
Quad I/O Fast Read	EBh	*	*
DTR Fast Read Quad I/O	EDh	*	*
Fast Read Quad I/O with 4-Byte Address	ECh	*	*
DTR Quad I/O Fast Read with 4- Byte Address	EEh	*	*
Set Burst with Wrap	77h	*	*
Set Read Parameters	C0h	*	*
Read Mftr./Device ID	90h	*	*
Dual IO Read Mftr./Device ID	92h	*	*
Quad IO Read Mftr./Device ID	94h	*	*
Read JEDEC ID	9Fh	*	*
Read Unique ID Number	4Bh	*	*
Release Powen-down/Device ID	ABh	*	*
Read Securty Registers	48h	*	*
Read SFDP	5Ah	*	*
Page Program	02h		*
Page Program with 4-Byte Address	12h		*
Quad Page Program	32h		*
Quad Input Page Program with 4-Byte Address	34h		*
Program/Erase Resume	7Ah	*	*
Read Block/Sector Lock	3Dh	*	*

Table 20. Acceptable Instructions During Suspend（tPSL/tESL not required）

Instruction Name	Instruction code	Suspend Type	
		Program Suspend	Erase Suspend
Read Status Register-1	05H	*	*
Read Status Register-2	35H	*	*
Read Status Register-3	15H	*	*
Enable Reset	66H	*	*
Reset Device	99H	*	*

tPSL: Program Suspend Latency; tESL: Erase Suspend Latency.

Figure 145. Program/Erase Suspend Instruction Sequence (SPI Mode)

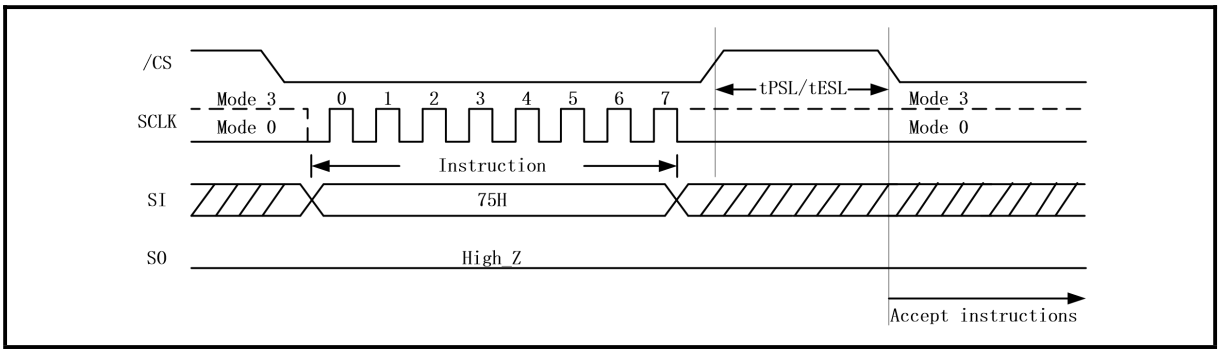
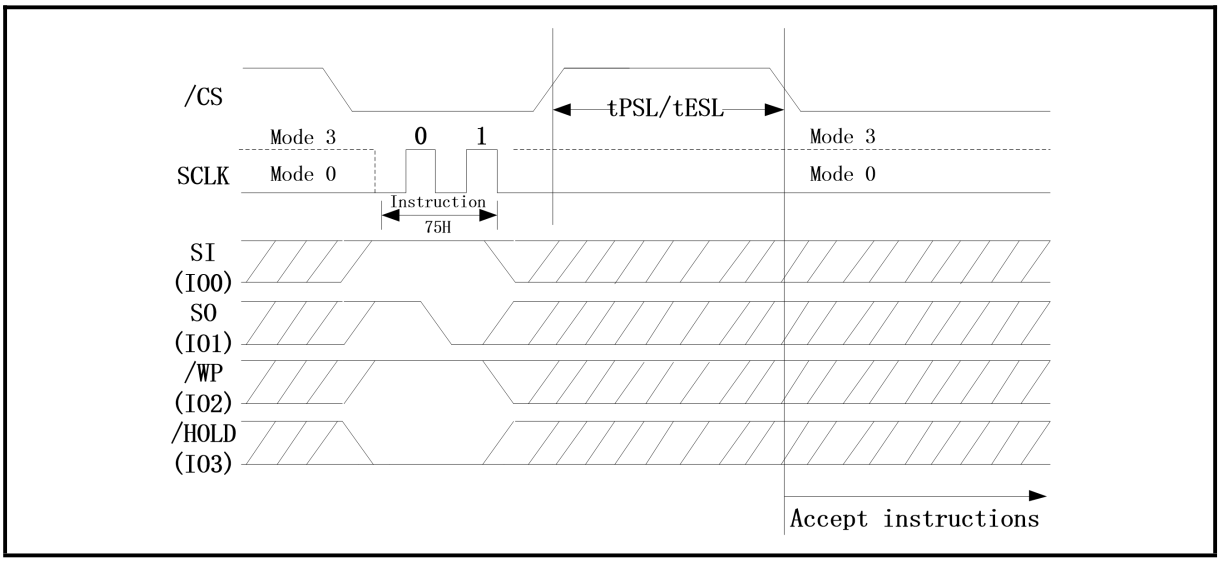


Figure 146. Program/Erase Suspend Instruction Sequence (QPI Mode)



7.4.13 Program/Erase Resume (7AH)

The Program/Erase Resume instruction “7Ah” must be written to resume the Sector or Block Erase operation or the Page Program operation after an Program/Erase Suspend. The Resume instruction “7AH” will be accepted by the device only if the SUS bit in the Status Register equals to 1 and the WIP bit equals to 0.

After the Resume instruction is issued the SUS bit will be cleared from 1 to 0 immediately, the WIP bit will be set from 0 to 1 within 200 ns and the Sector or Block will complete the erase operation or the page will complete the program operation. If the SUS bit equals to 0 or the WIP bit equals to 1, the Resume instruction “7Ah” will be ignored by the device. The Program/Erase Resume instruction sequence is shown in ***Figure 147-Figure 148***.

Figure 147. Program/Erase Resume Instruction Sequence (SPI Mode)

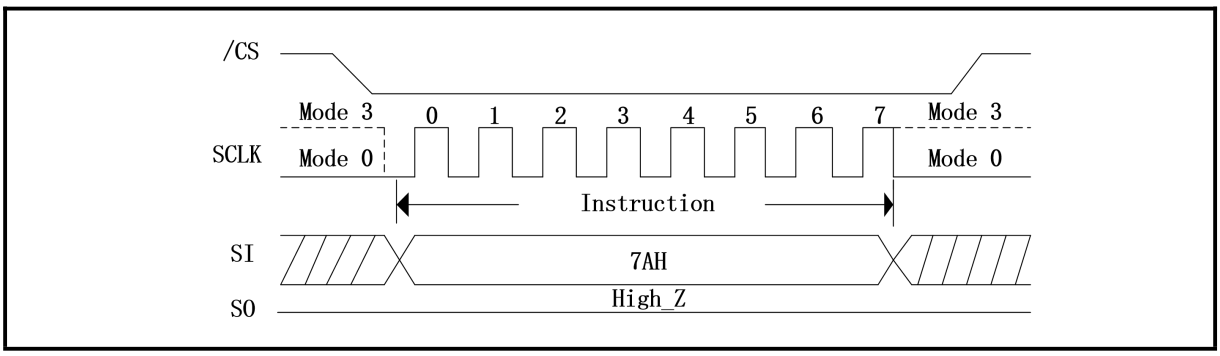
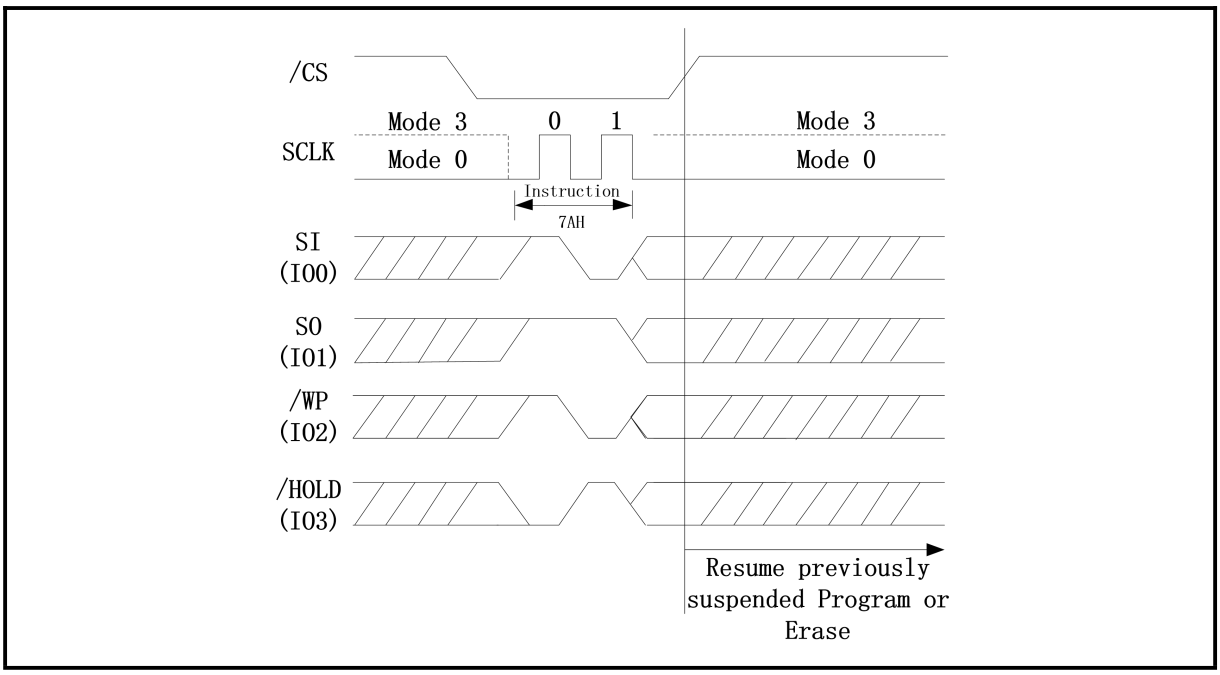


Figure 148. Program/Erase Resume Instruction Sequence (QPI Mode)



7.5 Individual Block Memory Protection Instructions

7.5.1 Read Block/Sector Lock (3DH)

The Read Block/Sector Lock (3Dh) instruction reads the status of the Individual Block/Sector Lock bit of a sector or block. The Read Block/Sector Lock instruction returns 00h if the Individual Block/Sector Lock bit is “0”, indicating write-protection is disabled. The Read Block/Sector Lock instruction returns FFh if the Individual Block/Sector Lock bit is “1”, indicating write-protection is enabled.

The Individual Block/Sector Lock bits are volatile bits for quickly and easily enabling or disabling write-protection to sectors and blocks. A Individual Block/Sector Lock bit is assigned to each 4KB sector in the bottom and top 64KB of memory and to each 64KB block in the rest of the memory. When a Individual Block/Sector Lock bit is “1”, the associated sector or block will be write-protected, preventing any program or erase operation on the sector or block. All Individual Block/Sector Lock bits default to “1” after power-on or reset.

See ***Figure 149-Figure 152***, to read out the Individual Block/Sector Lock bit value of a specific block or sector, the Read Block/Sector Lock (3Dh) instruction must be issued by driving /CS low, shifting the instruction code “3Dh” into the Data Input (SI or IO0-IO3) pin on the rising edge of CLK, followed by a 24/32-bit address. The Individual Block/Sector Lock bit value will be shifted out on the SO or IO0-IO3 pin at the falling edge of CLK with most significant bit (MSB) first as shown in Figure, and then driving /CS high. Please note that if not driven /CS high, the Individual Block/Sector Lock bit value will be repeatedly output.

Figure 149. Read Block/Sector Lock (SPI Mode/3-Byte Address Mode)

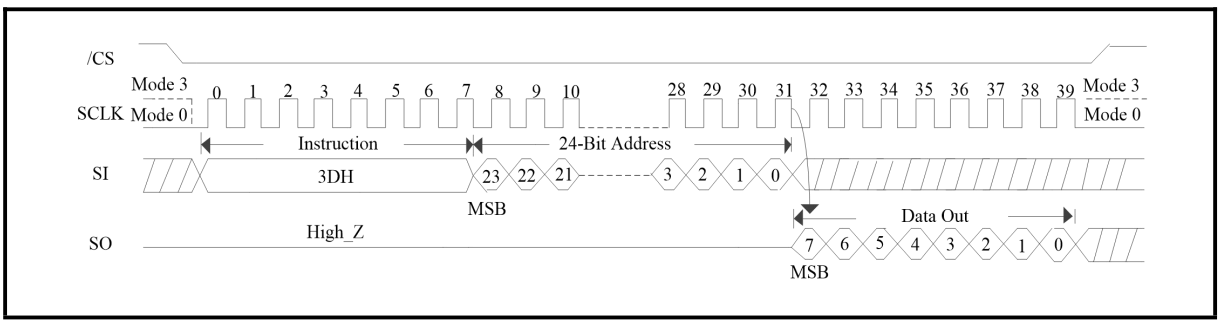


Figure 150. Read Block/Sector Lock (SPI Mode/4-Byte Address Mode)

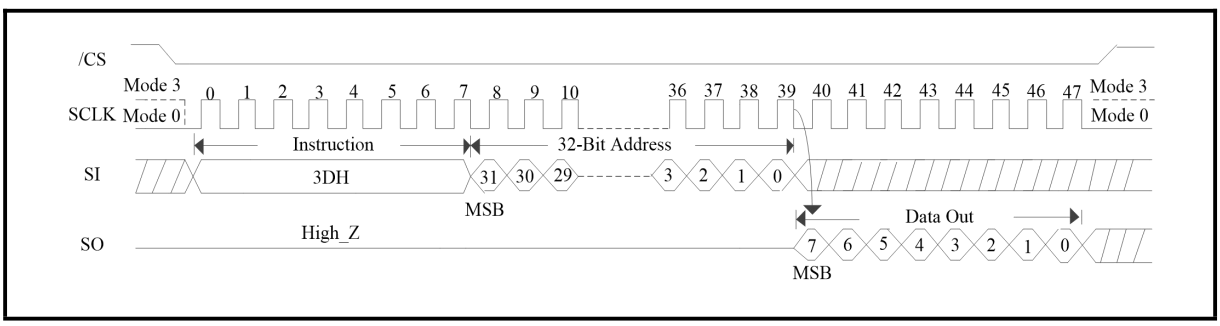


Figure 151. Read Block/Sector Lock (QPI Mode/3-Byte Address Mode)

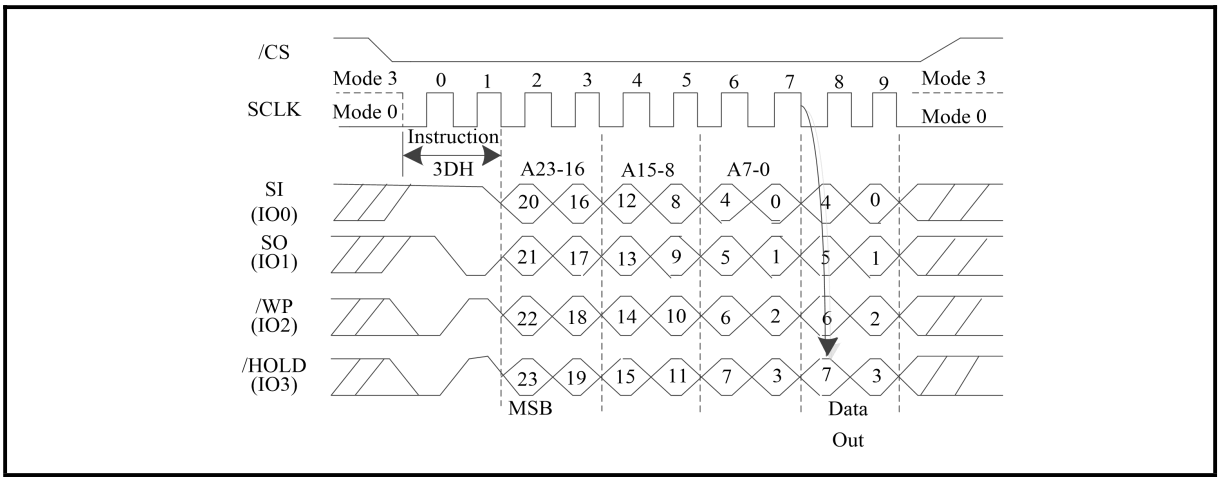
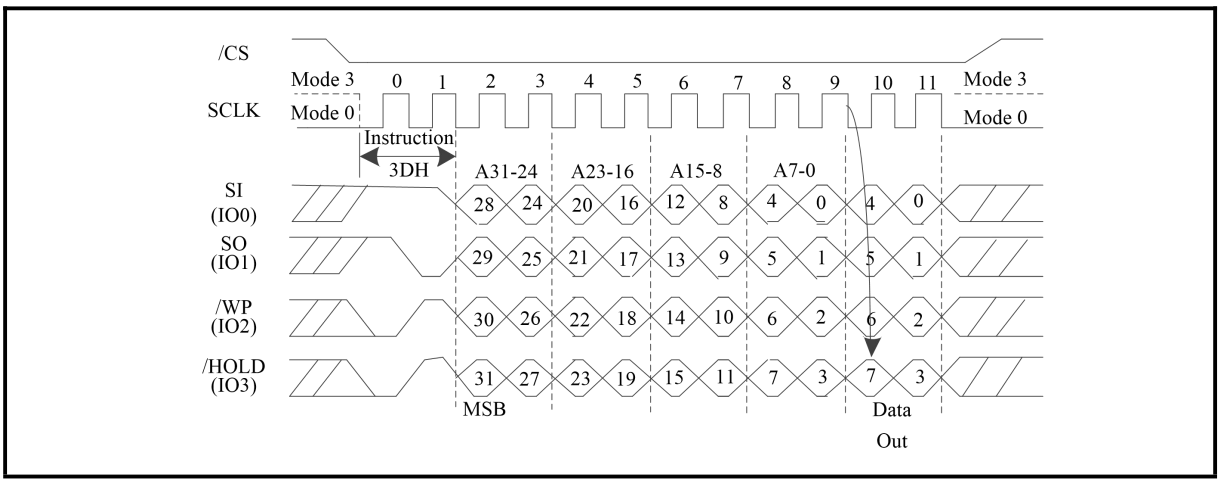


Figure 152. Read Block/Sector Lock (QPI Mode/4-Byte Address Mode)



7.5.2 Individual Block/Sector Lock (36H)

The Individual Block/Sector Lock (36h) instruction can individually set Individual Block/Sector Lock bits to “1”. When a Individual Block/Sector Lock bit is “1”, the associated sector or block will be write-protected, preventing any program or erase operation on the sector or block. All Individual Block/Sector Lock bits default to “1” after power-on or reset.

A Write Enable (06h) instruction must be executed to set the WEL bit before sending the Individual Block/Sector Lock instruction.

See ***Figure 153-Figure 156***, to set Individual Block/Sector Lock bit to “1”, the Individual Block/Sector Lock (36h) instruction must be issued by driving /CS low, shifting the instruction code “36h” into the Data Input (SI or IO0-IO3) pin on the rising edge of CLK, followed by a 24/32-bit address, and then driving /CS high.

Figure 153. Individual Block/Sector Lock (SPI Mode/3-Byte Address Mode)

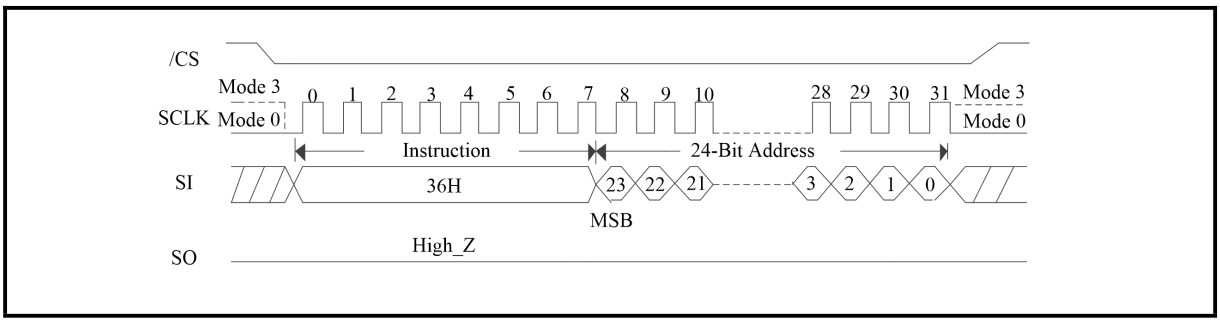


Figure 154. Individual Block/Sector Lock (SPI Mode/4-Byte Address Mode)

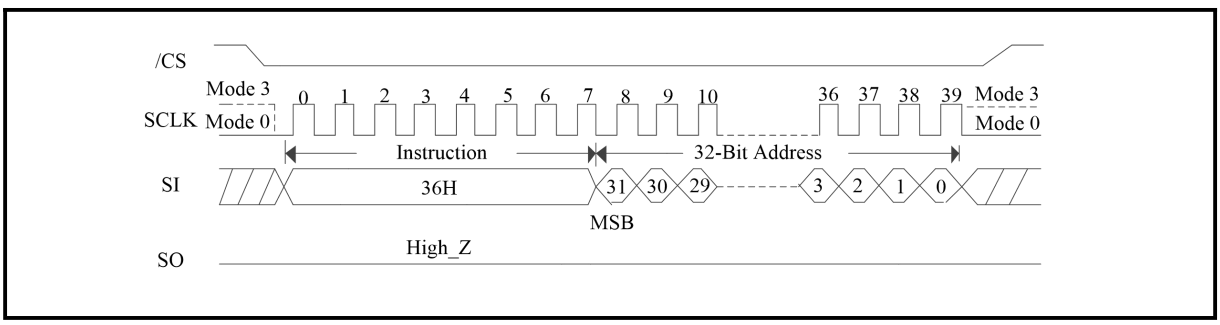


Figure 155. Individual Block/Sector Lock (QPI Mode/3-Byte Address Mode)

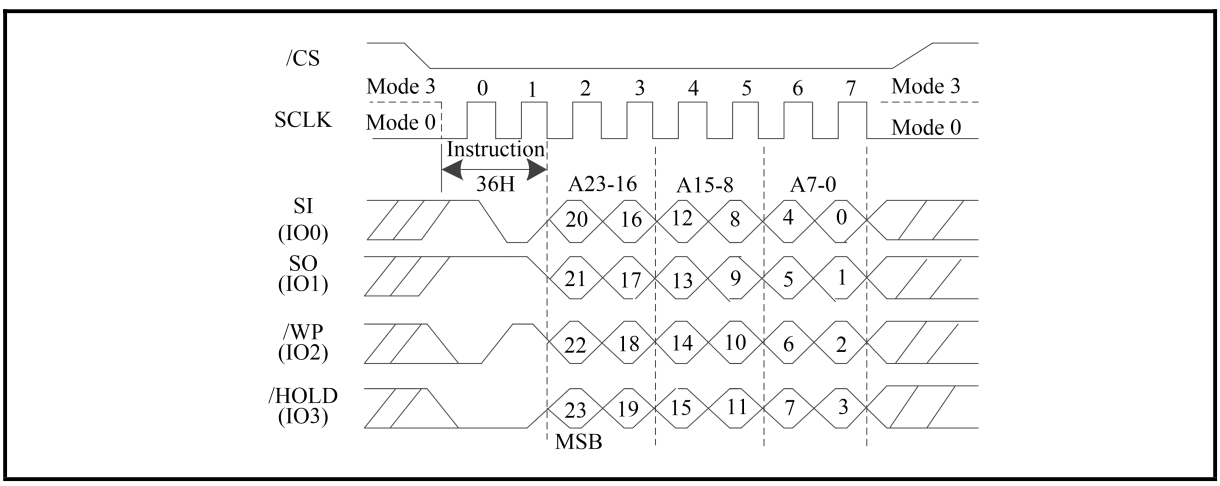
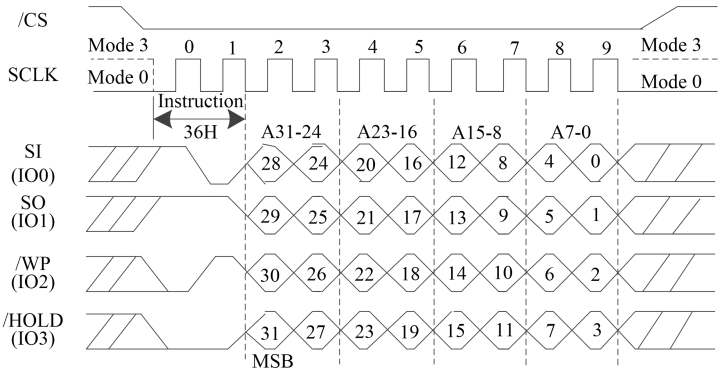


Figure 156. Individual Block/Sector Lock (QPI Mode/4-Byte Address Mode)



7.5.3 Individual Block/Sector Unlock (39H)

The Individual Block/Sector Unlock (39h) instruction can individually set Individual Block/Sector Lock bits to “0”.

A Write Enable (06h) instruction must be executed to set the WEL bit before sending the Individual Block/Sector Unlock instruction.

See ***Figure 157-Figure 160***, to set Individual Block/Sector Lock bit to “0”, the Individual Block/Sector Unlock (39h) instruction must be issued by driving /CS low, shifting the instruction code “39h” into the Data Input (SI or IO0-IO3) pin on the rising edge of CLK, followed by a 24/32-bit address, and then driving /CS high.

Figure 157. Individual Block/Sector Unlock (SPI Mode/3-Byte Address Mode)

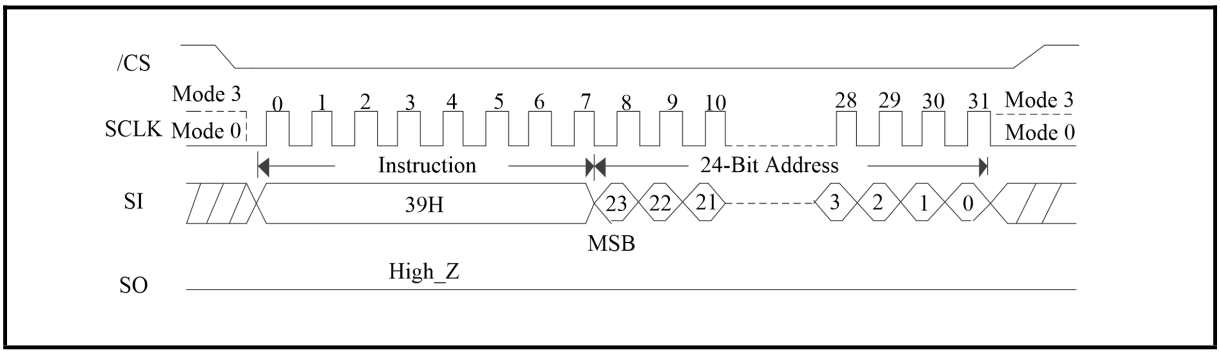


Figure 158. Individual Block/Sector Unlock (SPI Mode/4-Byte Address Mode)

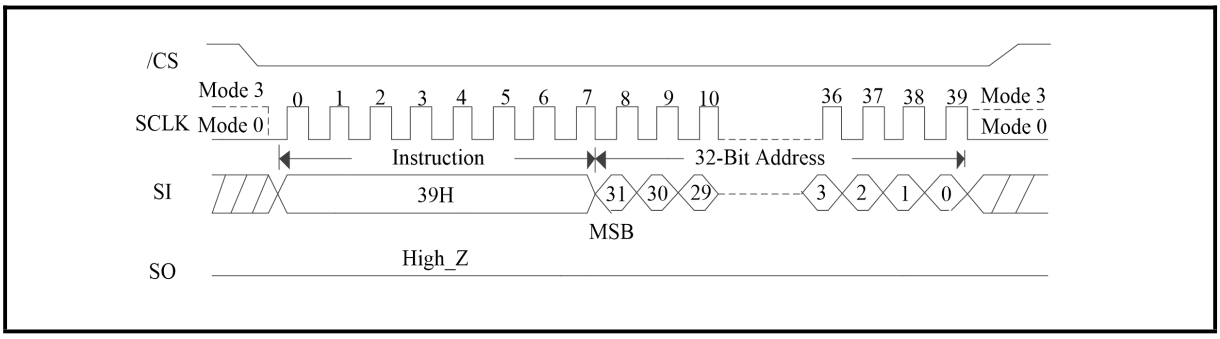


Figure 159. Individual Block/Sector Unlock (QPI Mode/3-Byte Address Mode)

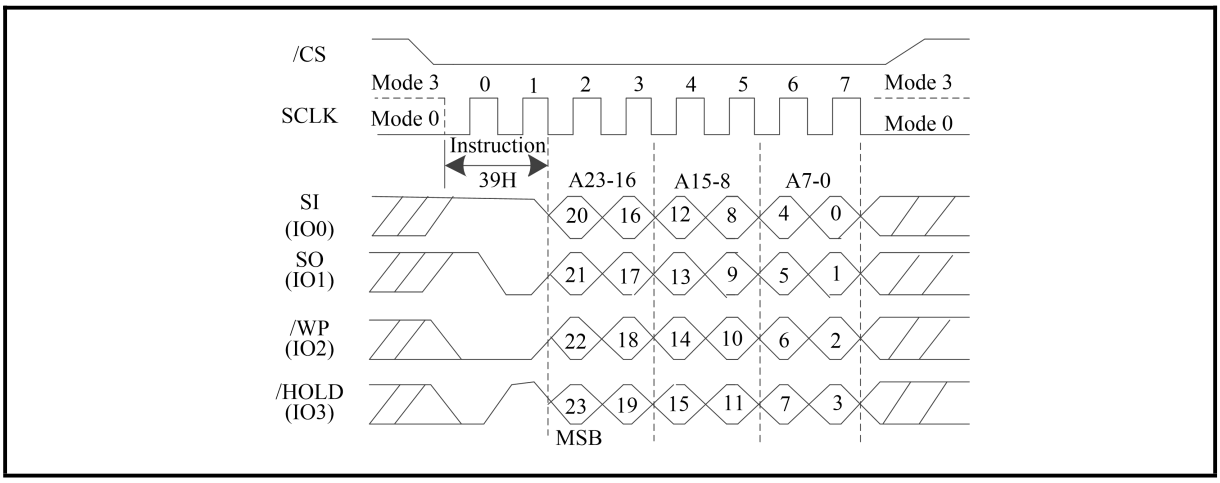
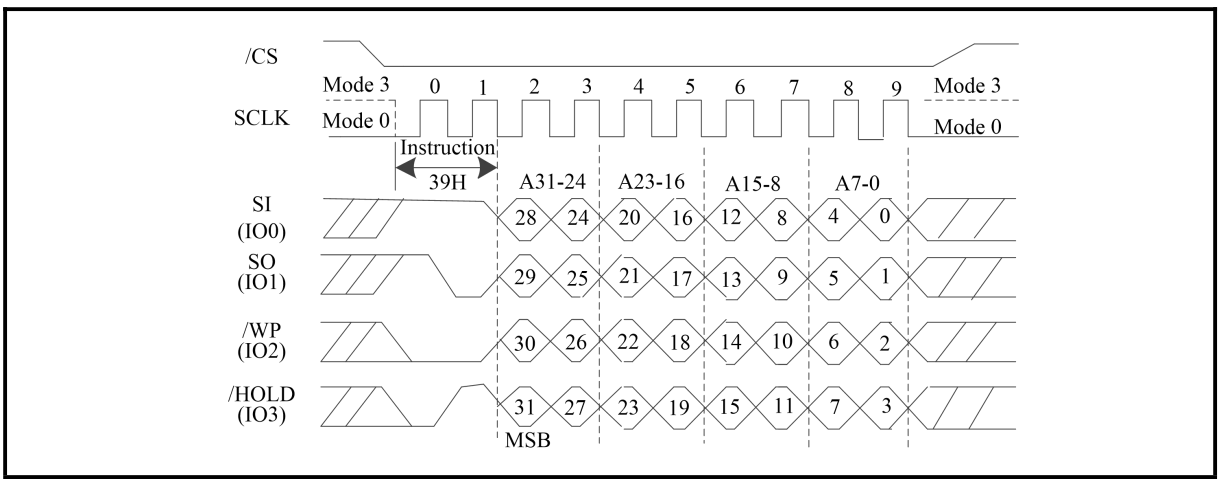


Figure 160. Individual Block/Sector Unlock (QPI Mode/4-Byte Address Mode)



7.5.4 Global Block/Sector Lock (7Eh)

The Global Block/Sector Lock (7Eh) instruction can set all Individual Block/Sector Lock bits to 1.

A Write Enable (06h) instruction must be executed to set the WEL bit before sending the Global Block/Sector Lock instruction.

See ***Figure 161-Figure 162***, to set all Individual Block/Sector Lock bits to "1", the Global Block/Sector Lock (7Eh) instruction must be issued by driving /CS low, shifting the instruction code "7Eh" into the Data Input (SI or IO0-IO3) pin on the rising edge of CLK, and then driving /CS high.

Figure 161. Global Block/Sector Lock (SPI Mode)

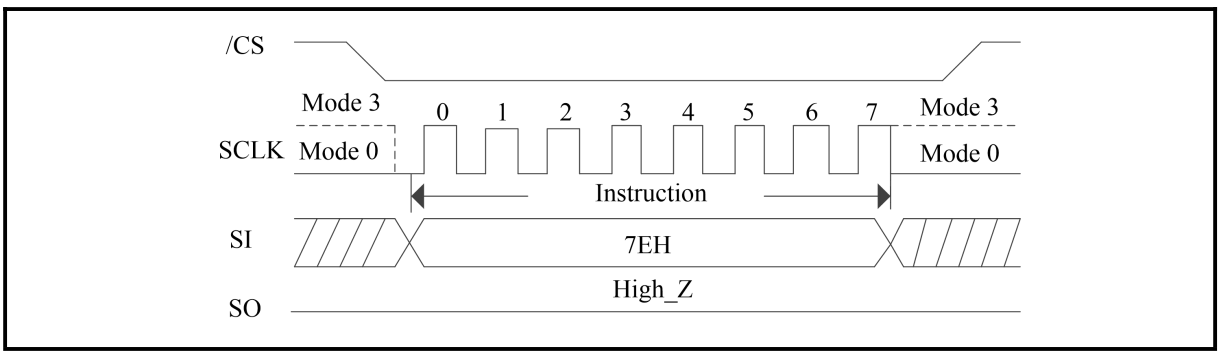
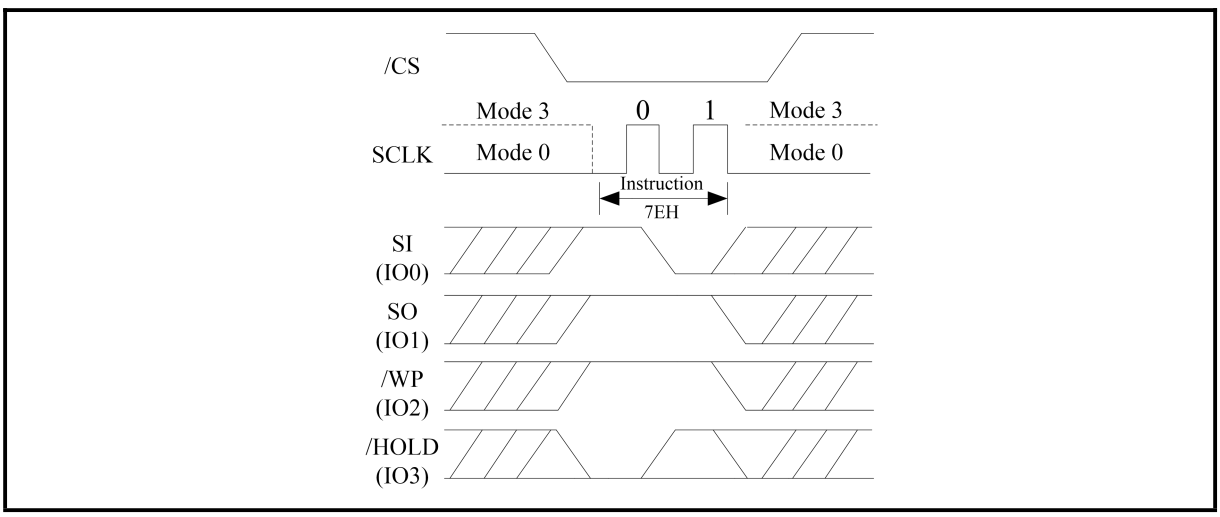


Figure 162. Global Block/Sector Lock (QPI Mode)



7.5.5 Global Block/Sector Unlock (98h)

The Global Block/Sector Unlock (98h) instruction can set all Individual Block/Sector Lock bits to 0.

A Write Enable (06h) instruction must be executed to set the WEL bit before sending the Global Block/Sector Unlock instruction.

See ***Figure 163-Figure 164***, to set all Individual Block/Sector Lock bits "0", the Global Block/Sector Unlock (98h) instruction must be issued by driving /CS low, shifting the instruction code "98h" into the Data Input (SI or IO0-IO3) pin on the rising edge of CLK, and then driving /CS high.

Figure 163. Global Block/Sector Unlock (SPI Mode)

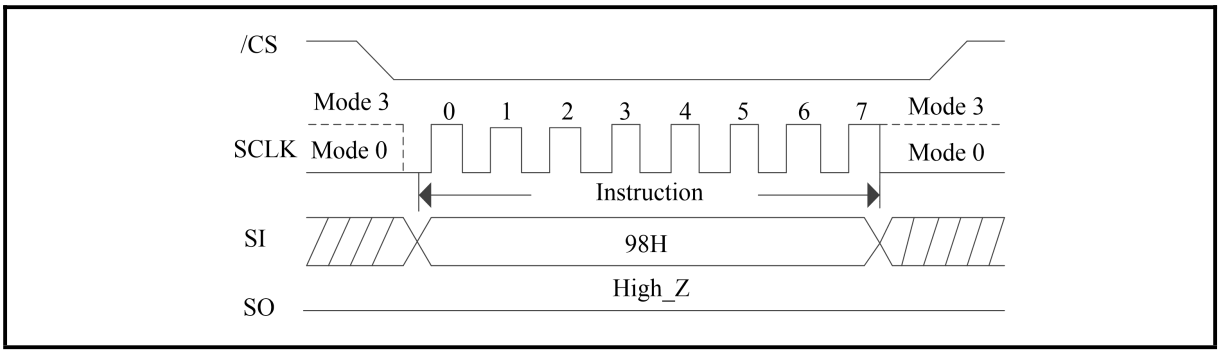
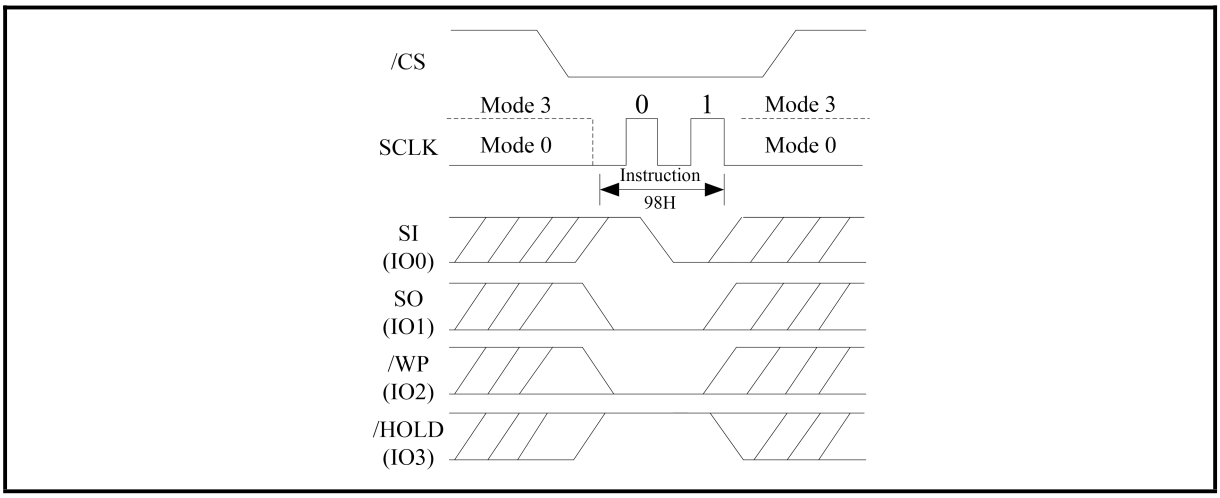


Figure 164. Global Block/Sector Unlock (QPI Mode)



8. Electrical Characteristics

8.1 Absolute Maximum Ratings

Parameter	Symbol	Conditions	Range	Unit.
Supply Voltage	VCC		–0.5 to 4	V
Voltage Applied to Any Pin	VIO	Relative to Ground	–0.5 to 4	V
Transient Voltage on any Pin	VIOT	<20nS Transient Relative to Ground	–2.0V to VCC+2.0V	V
Storage Temperature	TSTG		–65 to +150	°C
Electrostatic Discharge Voltage	VESD	Human Body Model(1)	–2000 to +2000	V

Notes:

1. JEDEC Std JESD22-A114 (C1=100pF, R1=1500 ohms, R2=500 ohms)

8.2 Operating Ranges

Parameter	Symbol	Conditions	Spec		Unit.
			Min	Max	
Supply Voltage	VCC		2.7	3.6	V
Temperature Operating	TA	Commercial	–40	+85	°C
		Industrial	–40	+105	
		Industrial	–40	+125	

8.3 Latch Up Characteristics

Parameter	Min	Max
Input Voltage Respect To VSS On I/O Pins	-1.0V	VCC+1.0V
VCC Current	-100mA	100mA

8.4 Power-up and Power-Down Timing

Symbol	Parameter	Min	Typ.	Max	Unit.
tVSL	VCC(min) To /CS Low	2.5			ms
V_{WI}	Write Inhibit Threshold Voltage V_{WI}	1.8		2.3	V
tVR	VCC rise time (from 0V to VCCmin)		1	6000 (1)	μs/V
tPWD	VCC brown-out low time	300			μs
V_{PWDMAX}	Maximum VCC brown-out			0.7	V

Notes:
1. 30000 μs/V at -10°C to 85°C.

Figure 165. Power-up Timing and Voltage Levels

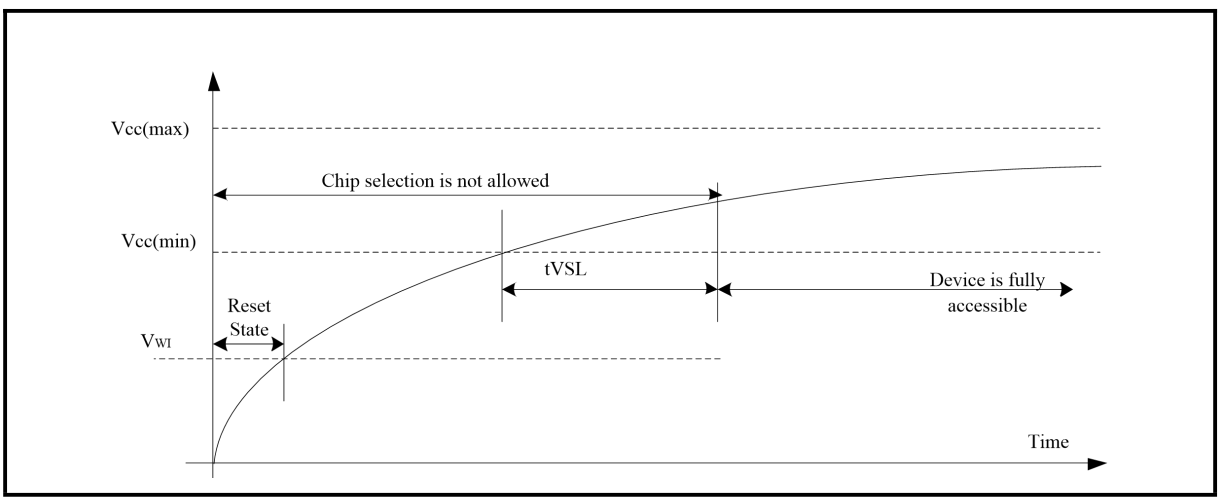
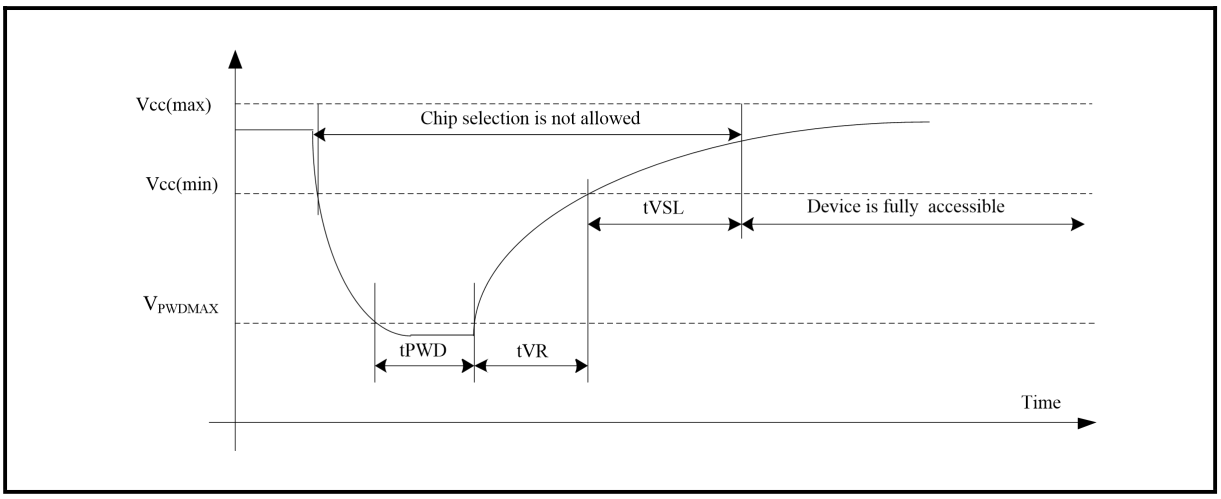


Figure 166. Power-Down Timing and Voltage Drop



8.5 DC Electrical Characteristics

(T= -40℃~85℃, VCC=2.7~3.6V)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
ILI	Input Leakage Current				±2	μA
ILO	Output Leakage Current				±2	μA
ICC1	Standby Current	/CS=VCC, VIN=VCC or VSS		14	50	μA
ICC2	Deep Power-Down Current	/CS=VCC, VIN=VCC or VSS		1	15	μA
ICC3	Operating Current: (Read)	SCLK=0.1VCC/ 0.9VCC, at 133MHz,Q=Open(*1,*,2*4 I/O)		12	18	mA
		SCLK=0.1VCC/ 0.9VCC, at 80MHz,Q=Open(*1,*,2*4 I/O)		10	13	mA
		SCLK=0.1VCC/ 0.9VCC, at 100MHz,DTR, Q=Open(*4 I/O)				
ICC4	Operating Current(Page Program)	/CS=VCC		10	15	mA
ICC5	Operating Current(WRSR)	/CS=VCC		12	20	mA
ICC6	Operating Current(Sector Erase)	/CS=VCC		12	20	mA
ICC7	Operating Current(Block Erase)	/CS=VCC		12	20	mA
ICC8	Operating Current (Chip Erase)	/CS=VCC		12	20	mA
VIL	Input Low Voltage		-0.5		0.2VCC	V
VIH	Input High Voltage		0.8VCC		VCC+0.4	V
VOL	Output Low Voltage	IOL =100μA			0.2	V
VOH	Output High Voltage	IOH =-100μA	VCC-0.2			V

(T= -40℃~105℃, VCC=2.7~3.6V)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
ILI	Input Leakage Current				±2	μA
ILO	Output Leakage Current				±2	μA
ICC1	Standby Current	/CS=VCC, VIN=VCC or VSS		14	100	μA
ICC2	Deep Power-Down Current	/CS=VCC, VIN=VCC or VSS		1	35	μA
ICC3	Operating Current: (Read)	SCLK=0.1VCC/ 0.9VCC, at 133MHz,Q=Open(*1,*,2*4 I/O)		12	20	mA
		SCLK=0.1VCC/ 0.9VCC, at 80MHz,Q=Open(*1,*,2*4 I/O)		10	18	mA
		SCLK=0.1VCC/ 0.9VCC, at 100MHz,DTR, Q=Open(*4 I/O)				
ICC4	Operating Current(Page Program)	/CS=VCC		10	20	mA
ICC5	Operating Current(WRSR)	/CS=VCC		12	25	mA
ICC6	Operating Current(Sector Erase)	/CS=VCC		12	25	mA
ICC7	Operating Current(Block Erase)	/CS=VCC		12	25	mA
ICC8	Operating Current (Chip Erase)	/CS=VCC		12	25	mA
VIL	Input Low Voltage		-0.5		0.2VCC	V
VIH	Input High Voltage		0.8VCC		VCC+0.4	V
VOL	Output Low Voltage	IOL =100μA			0.2	V
VOH	Output High Voltage	IOH =-100μA	VCC-0.2			V

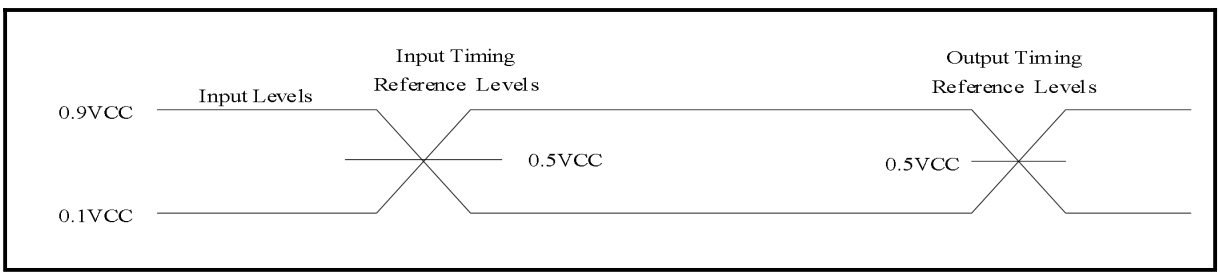
(T= -40℃~125℃, VCC=2.7~3.6V)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
ILI	Input Leakage Current				±2	μA
ILO	Output Leakage Current				±2	μA
ICC1	Standby Current	/CS=VCC, VIN=VCC or VSS		14	200	μA
ICC2	Deep Power-Down Current	/CS=VCC, VIN=VCC or VSS		1	60	μA
ICC3	Operating Current: (Read)	SCLK=0.1VCC/ 0.9VCC, at 133MHz,Q=Open(*1,*,2*4 I/O)		12	20	mA
		SCLK=0.1VCC/ 0.9VCC, at 80MHz,Q=Open(*1,*,2*4 I/O)		10	18	mA
		SCLK=0.1VCC/ 0.9VCC, at 100MHz,DTR, Q=Open(*4 I/O)				
ICC4	Operating Current(Page Program)	/CS=VCC		10	20	mA
ICC5	Operating Current(WRSR)	/CS=VCC		12	25	mA
ICC6	Operating Current(Sector Erase)	/CS=VCC		12	25	mA
ICC7	Operating Current(Block Erase)	/CS=VCC		12	25	mA
ICC8	Operating Current (Chip Erase)	/CS=VCC		12	25	mA
VIL	Input Low Voltage		-0.5		0.2VCC	V
VIH	Input High Voltage		0.8VCC		VCC+0.4	V
VOL	Output Low Voltage	IOL =100μA			0.2	V
VOH	Output High Voltage	IOH =-100μA	VCC-0.2			V

8.6 AC Measurement Conditions

Symbol	Parameter	Min	Tpy.	Max	Unit.	Conditions
CL	Load Capacitance			30	pF	
TR, TF	Input Rise And Fall time			5	ns	
VIN	Input Pause Voltage	0.1VCC to 0.9VCC			V	
IN	Input Timing Reference Voltage	0.5VCC			V	
OUT	Output Timing Reference Voltage	0.5VCC			V	

Figure 167. AC Measurement I/O Waveform



8.7 AC Electrical Characteristics

(T= -40℃~85℃, VCC=2.7~3.6V)

Symbol	Parameter	Min.	Typ.	Max.	Unit.
fR	Clock freq. for Read Array instructions (03H, 13H)	DC.		80	MHz
Fc	Clock frequency for Fast Read instructions (0BH, 0CH)			133	MHz
Fc	Clock frequency for DualOut / QuadOut Read instructions (3BH, 3CH, 6BH, 6CH)			133	MHz
Fc	Clock frequency for Read Array instructions (BBH, BCH, EBH, ECH)	Please refer to ***DC1/DC0 bit*** and ***Set Read Parameters*** (C0H)			MHz
F_R	Clock freq. for DTR instructions (EDH, EEH, 0EH)	Please refer to ***DC1/DC0 bit*** and ***Set Read Parameters*** (C0H)			MHz
Fc	Clock frequency for all instructions, except all Read Array Instructions, 2.7v~2.9V			133	MHz
Fc	Clock frequency for all instructions, except all Read Array Instructions, 3.0v~3.6v			166	MHz
tCLH	Serial Clock High Time	45% (1/FC)			ns
tCLL	Serial Clock Low Time	45% (1/FC)			ns
tCLCH	Serial Clock Rise Time (Slew Rate)	0.2(1)			V/ns

tCHCL	Serial Clock Fall Time (Slew Rate)	0.2(1)			V/ns
tSLCH	/CS Active Setup Time	5			ns
tCHSH	/CS Active Hold Time	5			ns
tSHCH	/CS Not Active Setup Time	5			ns
tCHSL	/CS Not Active Hold Time	5			ns
tSHSL	/CS High Time（read/write）	22			ns
tSHQZ	Output Disable Time			6	ns
tCLQX	Output Hold Time	2			ns
tDVCH	Data In Setup Time	2			ns
tCHDX	Data In Hold Time	2			ns
tHLCH	/Hold Low Setup Time (relative to Clock)	5			ns
tHHCH	/Hold High Setup Time (relative to Clock)	5			ns
tCHHL	/Hold High Hold Time (relative to Clock)	5			ns
tCHHH	/Hold Low Hold Time (relative to Clock)	5			ns
tHLQZ	/Hold Low To High-Z Output			6	ns
tHHQX	/Hold Low To Low-Z Output			6	ns
tCLQV	Clock Low To Output Valid (C_L=30pF)			7	ns
	Clock Low To Output Valid (C_L=10pF)			5	ns
tWHSL	Write Protect Setup Time Before /CS Low	20			ns
tSHWL	Write Protect Hold Time After /CS High	100			ns
tDP	/CS High To Deep Power-Down Mode			3	μs
tRES1	/CS High To Standby Mode Without Electronic Signature Read			20	μs
tRES2	/CS High To Standby Mode With Electronic Signature Read			20	μs
tESL	Erase Suspend Latency			20	μs
tPSL	Program Suspend Latency			20	μs
tPRS	Latency between Program Resume and next Suspend(3)	40			μs
tERS	Latency between Erase Resume and next Suspend(4)	40			μs
tRST	/CS High To Next Instruction After Reset in standby/read			1	μs
	/CS High To Next Instruction After Reset in program/DeepPower-Down			40	μs
	/CS High To Next Instruction After Reset in erase			10	ms
	/CS High To Next Instruction After Reset in write SR	Align to tW			
tW	Write Status Register Cycle Time		1.5	30	ms
tBP1	Byte Program Time (First Byte) (2)		40	100	μs
tBP2	Additional Byte Program Time (After First Byte) (2)		3	10	μs
tPP	Page Programming Time		0.3	2.4	ms
tSE	Sector Erase Time		25	300	ms
tBE	Block Erase Time(32K Bytes/64K Bytes)		0.06/	1/	S

			0.1	1.5	
tCE	Chip Erase Time		45	200	S

Notes:
1. Tested with clock frequency lower than 50 MHz.
2. For multiple bytes after first byte within a page, tBPn = tBP1 + tBP2 * N, where N is the number of bytes programmed.
3. For tPRS. minimum timing must be observed before issuing the next program suspend command. However, a period equal to or longer than the typical timing is required in order for the program operation to make progress.
4. For tERS, minimum timing must be observed before issuing the next erase suspend command. However, a period equal to or longer than the typical timing is required in order for the erase operation to make progress.
5. Value guaranteed by design and/or characterization, not 100% tested in production.

(T= -40℃~105℃, VCC=2.7~3.6V)

Symbol	Parameter	Min.	Typ.	Max.	Unit.
fR	Clock freq. for Read Array instructions (03H, 13H)	DC.		80	MHz
Fc	Clock frequency for Fast Read instructions (0BH, 0CH) and DualOut Read instructions (3BH, 3CH)			133	MHz
Fc	Clock frequency for QuadOut Read instructions (6BH, 6CH), Vcc 3.0V~3.6V			133	MHz
Fc	Clock frequency for QuadOut Read instructions (6BH, 6CH), Vcc 2.7V~2.9V			120	MHz
Fc	Clock frequency for Read Array instructions (BBH, BCH, EBH, ECH)	Please refer to ***DC1/DC0 bit*** and ***Set Read Parameters*** (C0H)			MHz
F_R	Clock freq. for DTR instructions (EDH, EEH, 0EH)	Please refer to ***DC1/DC0 bit*** and ***Set Read Parameters*** (C0H)			MHz
Fc	Clock frequency for all instructions, except all Read Array Instructions, 2.7v~2.9V			133	MHz
Fc	Clock frequency for all instructions, except all Read Array Instructions, 3.0v~3.6v			166	MHz
tCLH	Serial Clock High Time	45% (1/FC)			ns
tCLL	Serial Clock Low Time	45% (1/FC)			ns
tCLCH	Serial Clock Rise Time (Slew Rate)	0.2(1)			V/ns
tCHCL	Serial Clock Fall Time (Slew Rate)	0.2(1)			V/ns
tSLCH	/CS Active Setup Time	5			ns
tCHSH	/CS Active Hold Time	5			ns
tSHCH	/CS Not Active Setup Time	5			ns
tCHSL	/CS Not Active Hold Time	5			ns
tSHSL	/CS High Time（read/write）	22			ns
tSHQZ	Output Disable Time			6	ns
tCLQX	Output Hold Time	2			ns
tDVCH	Data In Setup Time	2			ns
tCHDX	Data In Hold Time	2			ns
tHLCH	/Hold Low Setup Time (relative to Clock)	5			ns
tHHCH	/Hold High Setup Time (relative to Clock)	5			ns
tCHHL	/Hold High Hold Time (relative to Clock)	5			ns
tCHHH	/Hold Low Hold Time (relative to Clock)	5			ns

tHLQZ	/Hold Low To High-Z Output			6	ns
tHHQX	/Hold Low To Low-Z Output			6	ns
tCLQV	Clock Low To Output Valid (C_L=30pF)			7	ns
	Clock Low To Output Valid (C_L=10pF)			5	ns
tWHSL	Write Protect Setup Time Before /CS Low	20			ns
tSHWL	Write Protect Hold Time After /CS High	100			ns
tDP	/CS High To Deep Power-Down Mode			3	μs
tRES1	/CS High To Standby Mode Without Electronic Signature Read			20	μs
tRES2	/CS High To Standby Mode With Electronic Signature Read			20	μs
tESL	Erase Suspend Latency			30	μs
tPSL	Program Suspend Latency			30	μs
tPRS	Latency between Program Resume and next Suspend(3)	60			μs
tERS	Latency between Erase Resume and next Suspend(4)	60			μs
tRST	/CS High To Next Instruction After Reset in standby/read			1	μs
	/CS High To Next Instruction After Reset in program/DeepPower-Down			70	μs
	/CS High To Next Instruction After Reset in erase			30	ms
	/CS High To Next Instruction After Reset in write SR	Align to tW			
tW	Write Status Register Cycle Time		2	30	ms
tBP1	Byte Program Time (First Byte) (2)		70	175	μs
tBP2	Additional Byte Program Time (After First Byte) (2)		3	10	μs
tPP	Page Programming Time		0.3	2.4	ms
tSE	Sector Erase Time		25	300	ms
tBE	Block Erase Time(32K Bytes/64K Bytes)		0.075 /0.13	1/ 1.5	S
tCE	Chip Erase Time		65	200	S

Notes:
1. Tested with clock frequency lower than 50 MHz.
2. For multiple bytes after first byte within a page, tBPn = tBP1 + tBP2 * N, where N is the number of bytes programmed.
3. For tPRS. minimum timing must be observed before issuing the next program suspend command. However, a period equal to or longer than the typical timing is required in order for the program operation to make progress.
4. For tERS, minimum timing must be observed before issuing the next erase suspend command. However, a period equal to or longer than the typical timing is required in order for the erase operation to make progress.
5. Value guaranteed by design and/or characterization, not 100% tested in production.

(T= -40℃~125℃, VCC=2.7~3.6V)

Symbol	Parameter	Min.	Typ.	Max.	Unit.
fR	Clock freq. for Read Array instructions (03H, 13H)	DC.		75	MHz
Fc	Clock frequency for Fast Read instructions (0BH, 0CH) and DualOut Read instructions (3BH, 3CH)			133	MHz
Fc	Clock frequency for QuadOut Read instructions (6BH, 6CH), Vcc 3.0V~3.6V			133	MHz
Fc	Clock frequency for QuadOut Read instructions (6BH, 6CH), Vcc 2.7V~2.9V			120	MHz
Fc	Clock frequency for Read Array instructions (BBH, BCH, EBH, ECH)	Please refer to ***DC1/DC0 bit*** and ***Set Read Parameters*** (C0H)			MHz
F_R	Clock freq. for DTR instructions (EDH, EEH, 0EH)	Please refer to ***DC1/DC0 bit*** and ***Set Read Parameters*** (C0H)			MHz
Fc	Clock frequency for all instructions, except all Read Array Instructions, 2.7v~2.9V			133	MHz
Fc	Clock frequency for all instructions, except all Read Array Instructions, 3.0v~3.6v			166	MHz
tCLH	Serial Clock High Time	45% (1/FC)			ns
tCLL	Serial Clock Low Time	45% (1/FC)			ns
tCLCH	Serial Clock Rise Time (Slew Rate)	0.2(1)			V/ns
tCHCL	Serial Clock Fall Time (Slew Rate)	0.2(1)			V/ns
tSLCH	/CS Active Setup Time	5			ns
tCHSH	/CS Active Hold Time	5			ns
tSHCH	/CS Not Active Setup Time	5			ns
tCHSL	/CS Not Active Hold Time	5			ns
tSHSL	/CS High Time（read/write）	22			ns
tSHQZ	Output Disable Time			6	ns
tCLQX	Output Hold Time	2			ns
tDVCH	Data In Setup Time	2			ns
tCHDX	Data In Hold Time	2			ns
tHLCH	/Hold Low Setup Time (relative to Clock)	5			ns
tHHCH	/Hold High Setup Time (relative to Clock)	5			ns
tCHHL	/Hold High Hold Time (relative to Clock)	5			ns
tCHHH	/Hold Low Hold Time (relative to Clock)	5			ns

tHLQZ	/Hold Low To High-Z Output			6	ns
tHHQX	/Hold Low To Low-Z Output			6	ns
tCLQV	Clock Low To Output Valid (C_L=30pF)			7	ns
	Clock Low To Output Valid (C_L=10pF)			6	ns
tWHSL	Write Protect Setup Time Before /CS Low	20			ns
tSHWL	Write Protect Hold Time After /CS High	100			ns
tDP	/CS High To Deep Power-Down Mode			3	μs
tRES1	/CS High To Standby Mode Without Electronic Signature Read			20	μs
tRES2	/CS High To Standby Mode With Electronic Signature Read			20	μs
tESL	Erase Suspend Latency			30	μs
tPSL	Program Suspend Latency			30	μs
tPRS	Latency between Program Resume and next Suspend(3)	60			μs
tERS	Latency between Erase Resume and next Suspend(4)	60			μs
tRST	/CS High To Next Instruction After Reset in standby/read			1	μs
	/CS High To Next Instruction After Reset in program/DeepPower-Down			70	μs
	/CS High To Next Instruction After Reset in erase			30	ms
	/CS High To Next Instruction After Reset in write SR	Align to tW			
tW	Write Status Register Cycle Time		2	30	ms
tBP1	Byte Program Time (First Byte) (2)		70	175	μs
tBP2	Additional Byte Program Time (After First Byte) (2)		3	10	μs
tPP	Page Programming Time		0.3	2.4	ms
tSE	Sector Erase Time		25	300	ms
tBE	Block Erase Time(32K Bytes/64K Bytes)		0.075 /0.13	1/ 1.5	S
tCE	Chip Erase Time		65	200	S

Notes:
1. Tested with clock frequency lower than 50 MHz.
2. For multiple bytes after first byte within a page, tBPn = tBP1 + tBP2 * N, where N is the number of bytes programmed.
3. For tPRS. minimum timing must be observed before issuing the next program suspend command. However, a period equal to or longer than the typical timing is required in order for the program operation to make progress.
4. For tERS, minimum timing must be observed before issuing the next erase suspend command. However, a period equal to or longer than the typical timing is required in order for the erase operation to make progress.
5. Value guaranteed by design and/or characterization, not 100% tested in production.

Figure 168. Serial input Timing

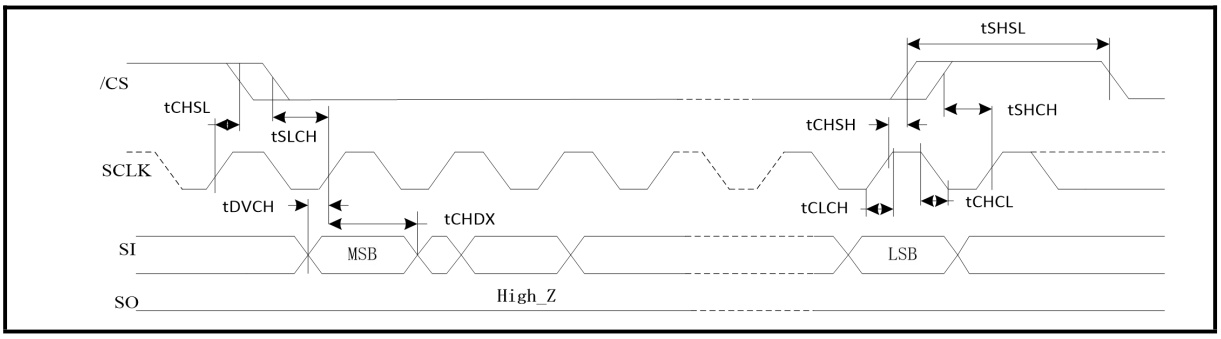


Figure 169. Output Timing

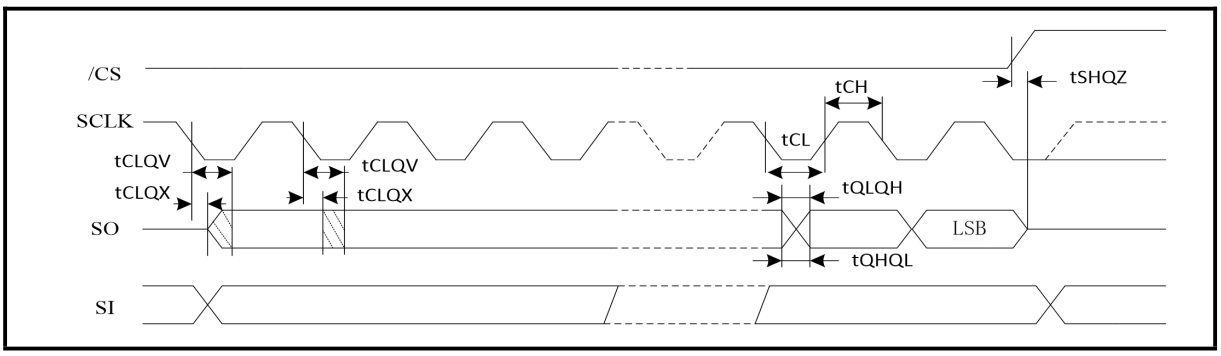


Figure 170. Hold Timing

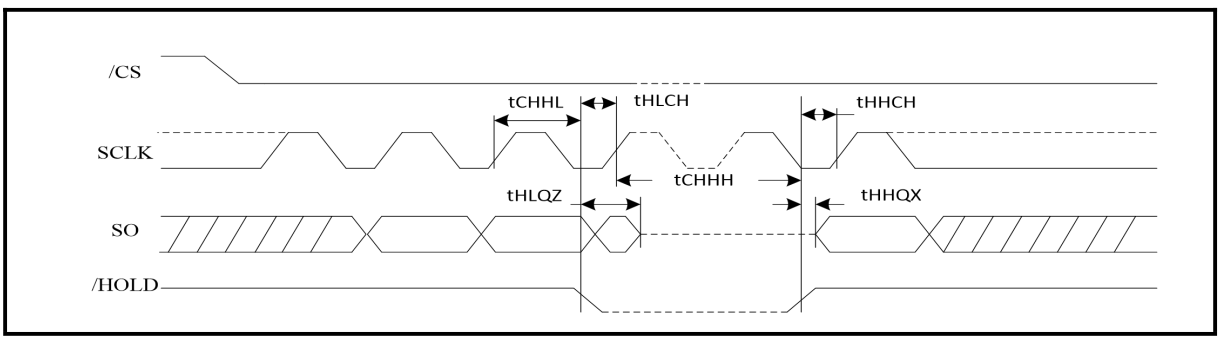
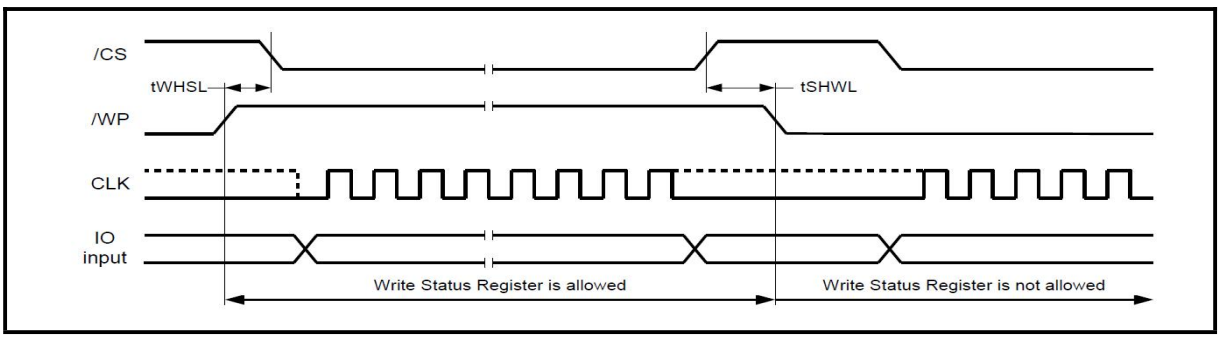
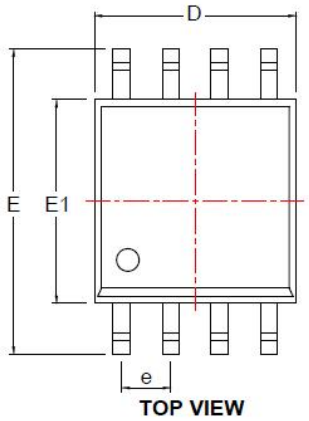


Figure 171. /WP Timing

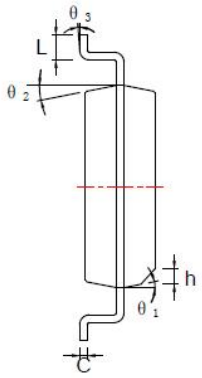


9. Package Information

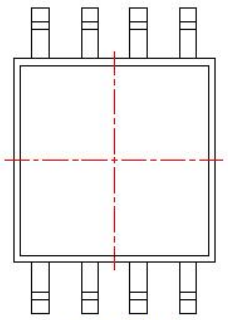
9.1 Package 8-Pin SOP 208-mil

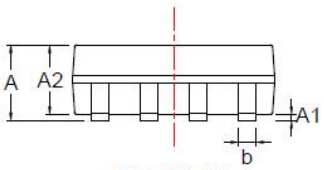


TOP VIEW



SIDE VIEW


BTM VIEW

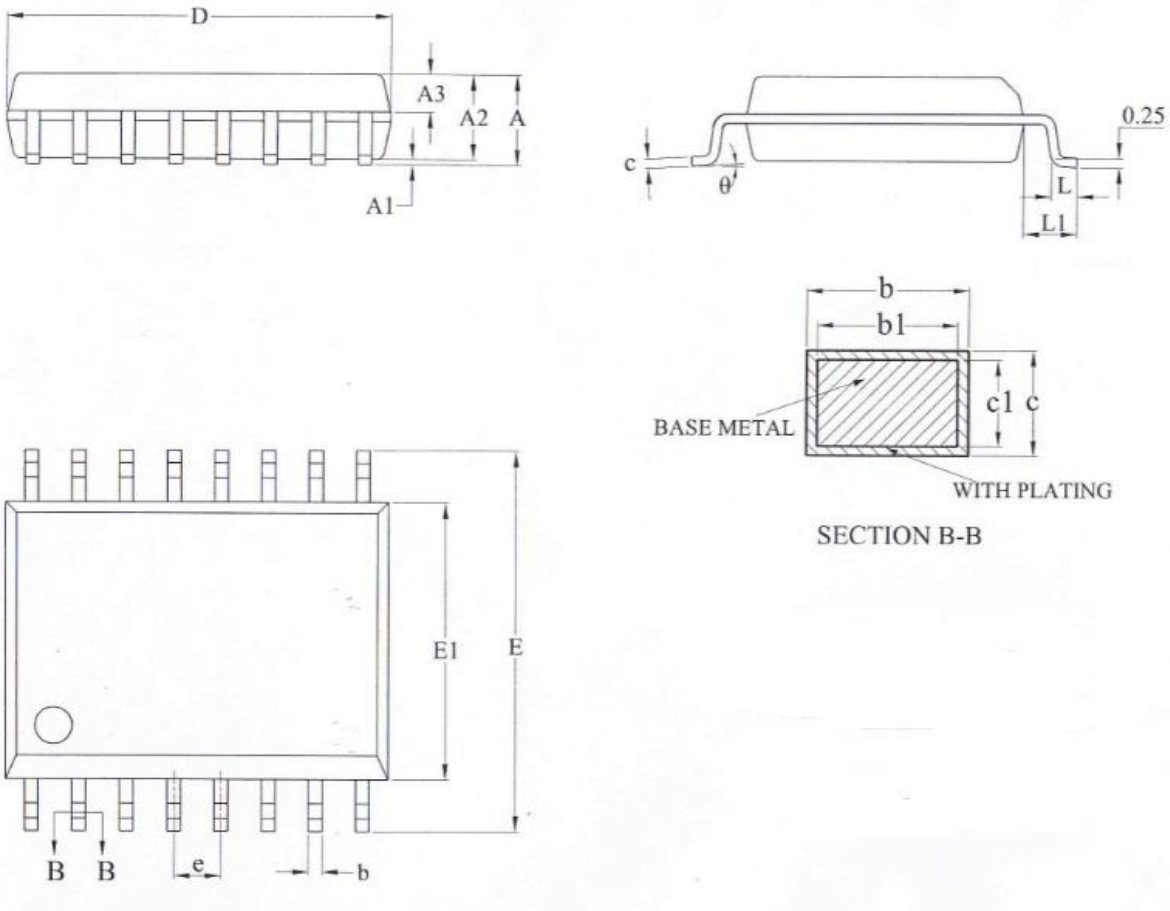


SIDE VIEW

DIMENSIONS IN MUILLIMETERS

SYMBOL	MIN	NOM	MAX
A	1.75	1.95	2.15
A_1	0.05	0.15	0.25
A_2	1.70	1.80	1.90
b	0.40	0.45	0.50
c	0.19	0.20	0.21
D	5.13	5.23	5.33
E	7.70	7.90	8.10
E_1	5.10	5.25	5.40
e	1.17	1.27	1.37
L	0.50	0.65	0.80
h	0.30	0.40	0.50
θ_1	••••	——	••••
θ_2	••••••	——	••••••
θ_3	••••••	——	••••••

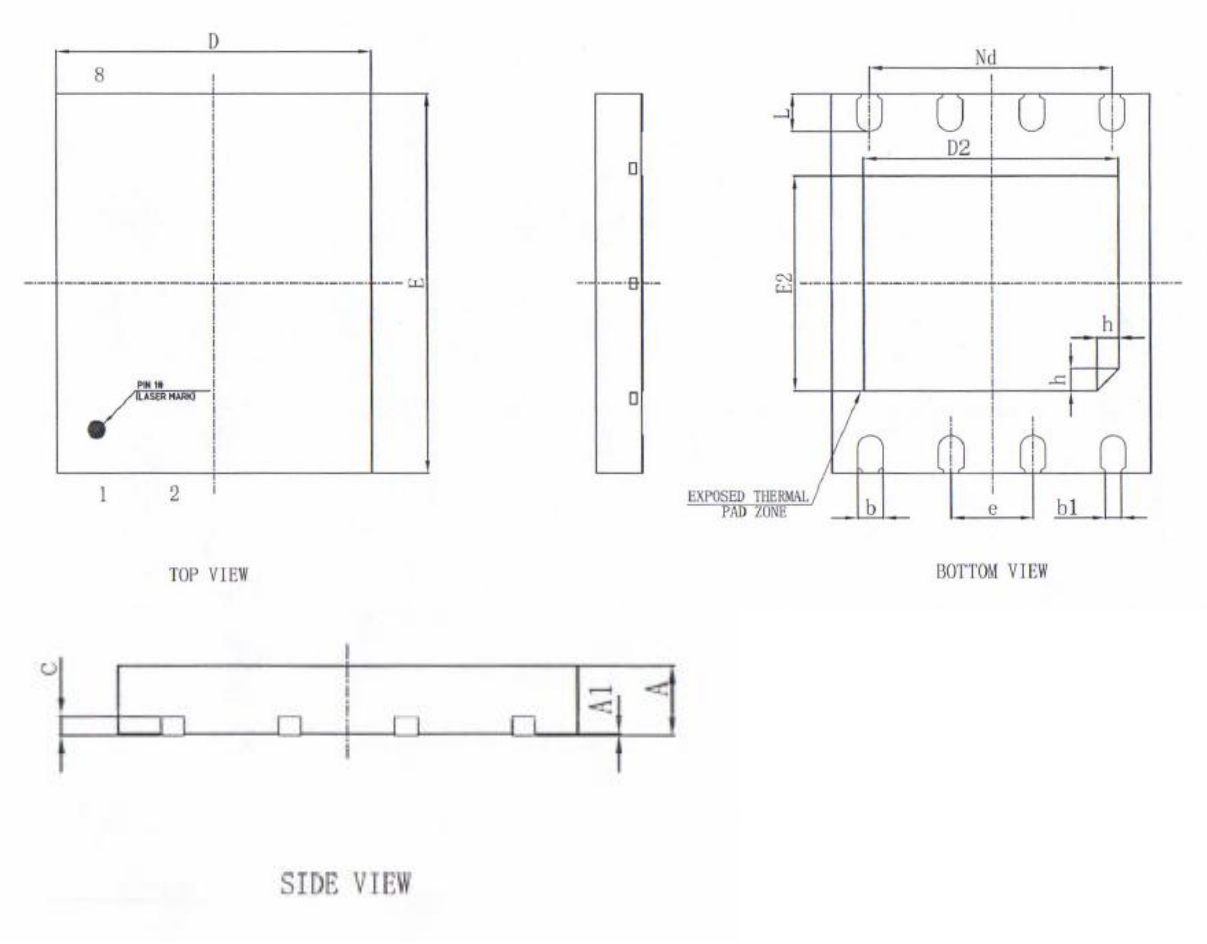
9.2 Package SOP16-300mil



Dimensions

Symbol / Unit		A	A1	A2	A3	b	b1	c	c1	D	E	E1	e	L	L1	θ
mm	Min	-	0.10	2.25	0.97	0.35	0.34	0.25	0.24	10.20	10.10	7.40	1.27BSC	0.55	1.40REF	0°
	Nom	-	-	2.30	1.02	-	0.37	-	0.25	10.30	10.30	7.50		-		-
	Max	2.65	0.30	2.35	1.07	0.43	0.40	0.29	0.26	10.40	10.50	7.60		0.85		8°

9.3 Package 8-Pad WSON (5x6mm)



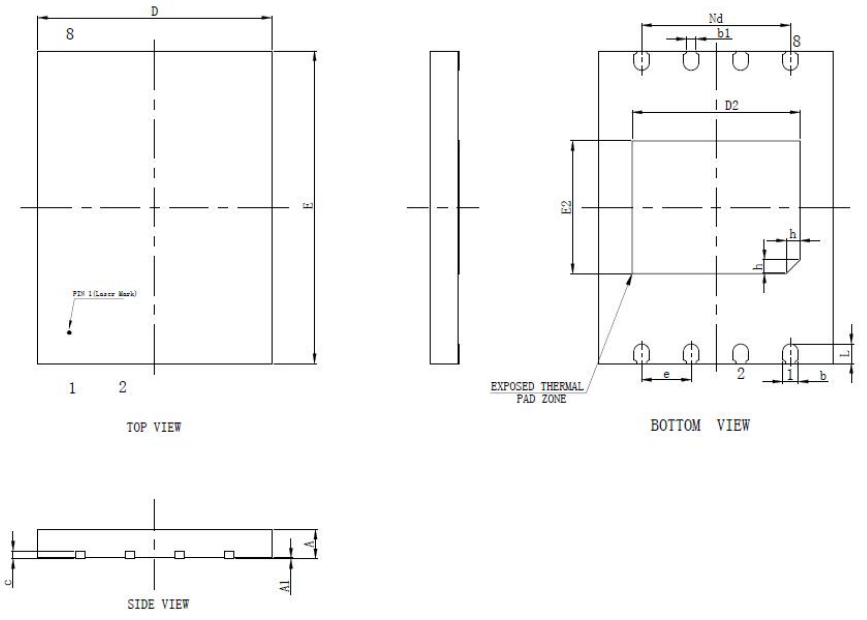
Dimensions

Symbol / Unit		A	A1	b	b1	c	D	Nd	e	E	D2	E2	L	h
mm	Min	0.70	0	0.35	0.25REF	0.18	4.90	3.81BSC	1.27BSC	5.90	3.90	3.30	0.55	0.30
	Nom	0.75	0.02	0.40		0.203	5.00			6.00	4.00	3.40	0.60	0.35
	Max	0.80	0.05	0.45		0.25	5.10			6.10	4.10	3.50	0.65	0.40

Note:

1. The exposed metal pad area on the bottom of the package is floating.

9.4 Package 8-Pad WSON (6x8mm)

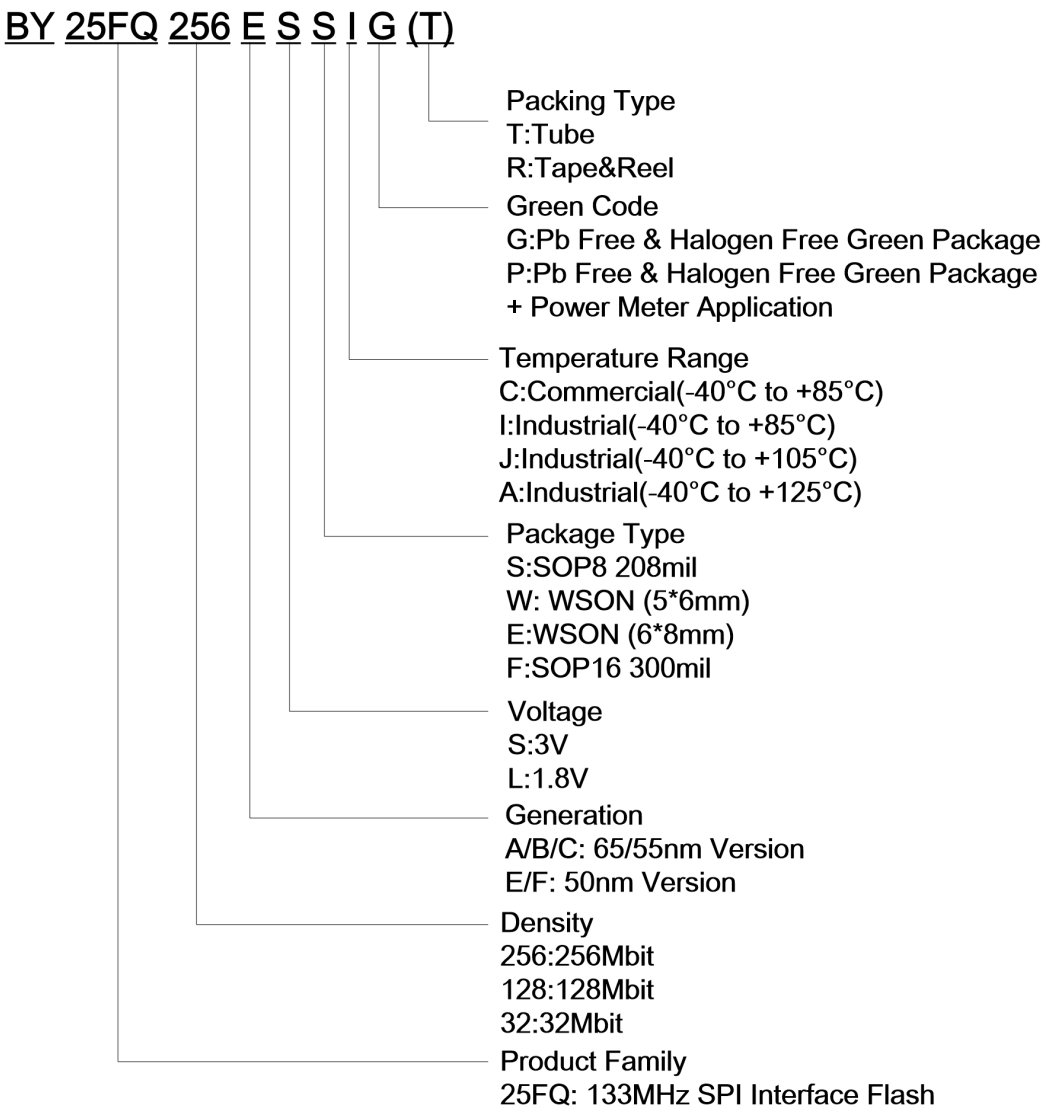


SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.35	0.40	0.45
b1	0.25REF		
c	0.18	0.203	0.25
D	5.90	6.00	6.10
Nd	3.81BSC		
e	1.27BSC		
E	7.90	8.00	8.10
D2	4.20	4.30	4.40
E2	3.30	3.40	3.50
L	0.45	0.50	0.55
h	0.30	0.35	0.40

Note:

1. The exposed metal pad area on the bottom of the package is floating.

10. Order Information



10.1 Valid part Numbers and Top Side Marking

The following table provides the valid part numbers for BY25FQ256 SPI Flash Memory. Pls contact BoyaMicro for specific availability by density and package type.

For consumer and industry application (-40C~+85C):

Package Type	Density	Product Number	Top Side Marking
S SOP8 208mil	256M-bit	BY25FQ256ESSIG	BYT 25FQ256ESSIG YYWW
W WSON8 6*5mm	256M-bit	BY25FQ256ESWIG	BYT 25FQ256ESWIG YYWW
E WSON8 6*8mm	256M-bit	BY25FQ256ESEIG	BYT 25FQ256ESEIG YYWW
F SOP16 300mil	256M-bit	BY25FQ256ESFIG	BYT 25FQ256ESFIG YYWW

10.2 Minimum Packing Quantity (MPQ)

Package Type	Packing Type	Qty for 1 Tube or Reel	Vacuum bag/ Inner Box	MPQ
SOP8 208mil	Tube	95ea/Tube	100Tubes/Bag 1Bag/InnerBox	9,500
	Tape&Reel (13inch, 16mm)	2000ea/Reel	1Reel/Bag 2Bags/InnerBox	4,000
WSON8 5*6mm	Tape&Reel (13inch)	3000ea/Reel	1Reel/Bag 1Bag/InnerBox	3,000
WSON8 6*8mm	Tape&Reel (13inch)	3000ea/Reel	1Reel/Bag 1Bag/InnerBox	3,000
SOP16 300mil	Tube	44ea/Tube	80Tubes/Bag 1Bag/InnerBox	3,520
	Tape&Reel (13inch, 16mm)	1500ea/Reel	1Reel/Bag 1Bags/InnerBox	1500

11. Document Change History

REVISION	CHANGE DESCRIPTION	CLAUSE	ORIGINATOR DATE
1.0	Initiate	/	Zuohuan Yu 2023-02-01
1.1	Add the note of the DFN package	/	Zuohuan Yu 2023-07-19
1.2	Update AC/DC information	/	Zuohuan Yu 2024-01-06
1.3	Update AC/DC information	/	Zuohuan Yu 2024-3-12
1.4	Update AC/DC information	/	Zuohuan Yu 2024-4-3
1.5	Update AC/DC information	/	Zuohuan Yu 2024-8-6
1.6	Add T&R MPQ of SOP16-300mil	P150 Cl.10.2	Guoshun Wu 2024-9-27