# HX18B20-T High-Precision Digital Temperature Sensor

HX18B20-T is a high-precision digital temperature sensor with a wide range from -55°C to +125°C. It boasts excellent ESD performance >8000V (HBM) & >1000V (CDM), and LU >200mA.Its temperature resolution is configurable from 9 to= 12-bit digital output to meet various application needs.

Each HX18B20-T features a unique 64-bit code and a 3-byte non-volatile memory, allowing multiple HX18B20-Ts to be easily connected and operated simultaneously via a single bus in distributed applications. This design facilitates networking and distributed applications.

HX18B20-T's NV mem stores temp alert thresholds, resolution info, boosting flexibility & configurability. Minimal externals needed, simplifying circuit design. Reducing overall system complexity.

HX18B20-T is a powerful, high-performance, and easy-to-use digital temperature sensor suitable for various temperature measurement and monitoring applications.

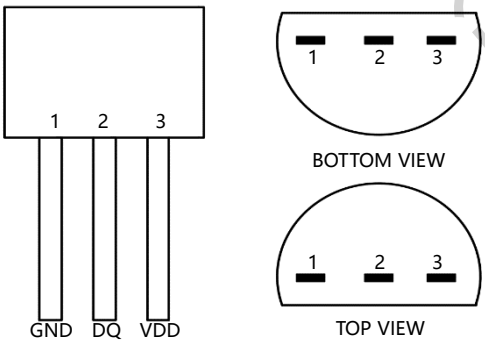
TO-92

## Characteristic

- Single-bus interface simplifies connections and saves resources.
- Highly integrated, no external components needed, reducing system complexity.
- With a broad temperature range from -55°C to +125°C, it offers ±0.5°C accuracy between -10°C and +85°C.
- It features programmable temperature resolution with digital output ranging from 9 to 12 bits.
- Each HX18B20-T features a unique 64-bit ROM code, facilitating its use in distributed temperature measurement systems.
- Customizable alarm thresholds allow for quick identification of alerting chips via alarm search commands.
- Compatible with working voltages from 3V to 5.5V, suitable for various power supply environments.
- It offers products in TO-92 packaging.

## Application

- Thermosensitive System
- Consumer Electronics Products
- Industrial environments such as HVAC, buildings, large machinery, etc.
- Temperature measurement instruments such as thermometers, etc.
- Temperature Monitor




| CHIP PIN DESCRIPTION | | |
|---|---|---|
| **PIN** | **NAME** | **FUNCTION** |
| 1 | GND | Grounding Pin |
| 2 | DQ | DIO pin (Data Input/Output pin) in parasitic power supply mode for chip powering. |
| 3 | VDD | Power Pin |

| CHIP CHARACTERISTICS | |
|---|---|
| **Max. Ratings** | |
| Voltage Value from Any Pin to Ground | -0.5V to +6.0V |
| Operating Temperature Range | -55°C to +125°C |
| Storage Temperature Range | -55°C to +125°C |

**Non volatile memory (test conditions: from -40 ℃ to+85 ℃; VDD power supply from 3V to 5.5V)**

| Parameter | OT | MIN | Typ. values | MAX | UNIT |
|---|---|---|---|---|---|
| Write cycle time | From-40℃ to +85℃ | | 4 | | ms |
| Write frequency | From-40℃ to +85℃ | 10k | | | 次数 |
| Data storage time | ≤85℃ | | 10 | | 年 |

**DC electrical characteristics (test conditions: from -55 ℃ to+125 ℃; VDD power supply from 3V to 5.5V)**

| Parameter | Symbol | | MIN | Typ. values | MAX | UNIT | NOTES |
|---|---|---|---|---|---|---|---|
| Vcc | $V_{DD}$ | | 3 | | 5.5 | V | |
| Pull-up Voltage | $V_{PU}$ | | 3 | | 5.5 | V | |
| Temperature Error | $t_{ERR}$ | -10 to +85℃ | ±0.5 | | | ℃ | |
| | $t_{ERR}$ | -55 to +125℃ | ±2.0 | | | | |
| Inject current | $I_L$ | | 4 | | | mA | |
| Idle Current | $I_{DDS}$ | | | | 500 | nA | A,B |
| working current | $I_{DD}$ | | | 0.2 | 0.5 | mA | C |
| DQ input current | $I_{DQ}$ | | 1 | | | uA | |

**AC electrical characteristics (test conditions: from -55 ℃ to+125 ℃; VDD power supply from 3V to 5.5V)**

| Parameter | Symbol | CONDITION | MIN | Typ. values | MAX | UNIT |
|---|---|---|---|---|---|---|
| Temperature conversion time | $t_{CONV}$ | 9-bit resolution | | | 62.5 | ms |
| | | 10-bit resolution | | | 125 | ms |
| | | 11-bit resolution | | | 250 | ms |
| | | 12-bit resolution | | | 500 | ms |
| Time slot length | $t_{SLOT}$ | D | 60 | | 120 | us |
| Recovery time | $t_{REC}$ | D | 1 | | | us |
| Low-Level Time | $t_{LOW0}$ | D | 60 | | 120 | us |
| Write 1 low level time | $t_{LOW1}$ | D | 1 | | 15 | us |
| Read data validity time | $t_{RDV}$ | D | | | 15 | us |
| High Reset Time | $t_{RSTH}$ | D | 480 | | | us |
| Low Reset Time | $t_{RSTL}$ | D | 480 | | | us |
| Online Detection | $t_{PDH}$ | D | 15 | | 60 | us |
| Online Low-time Detection | $t_{PDLOW}$ | D | 60 | | 240 | us |

## Notes;

A. The standby current is defined within the range of -55℃ to 70℃, with a typical value of 3uA at 125℃.

B. To minimize IDDS, the DQ signal must satisfy the following conditions: GND ≤ DQ ≤ GND +0.3V or VDD - 0.3V ≤ DQ ≤ VDD.

C. The dynamic current refers to the temperature transition current.

D. Avoid having the time interval between any two falling edges fall within the range of 200-300 microseconds.

E. Please refer to Figures 3, 4, 5, and 6 for the timing diagrams.

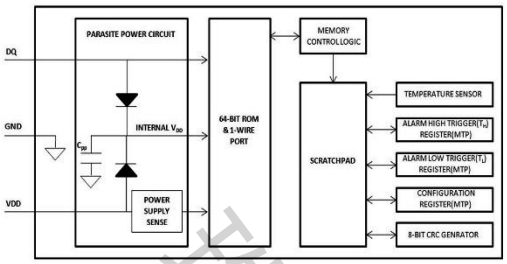



Figure 1 Simplified principle

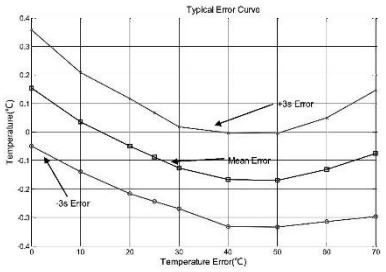



Figure 2 Typical Error Curve

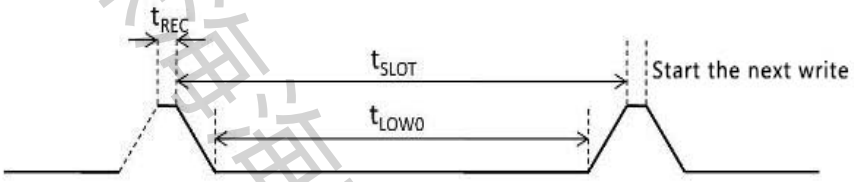



Figure 3: Time sequence diagram for writing 0

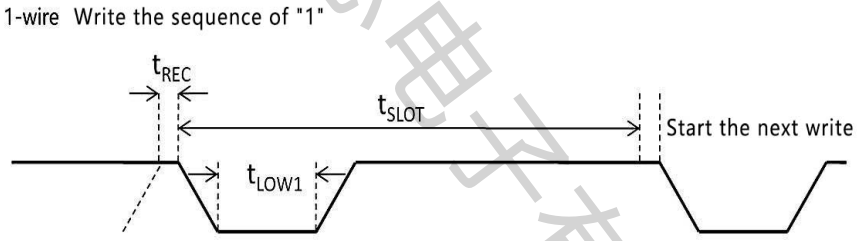



Figure 4: Write 1 timing diagram

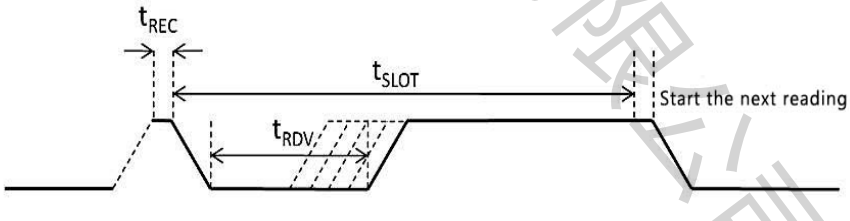



Figure 5 Reading timing (including read 1 and read 0)

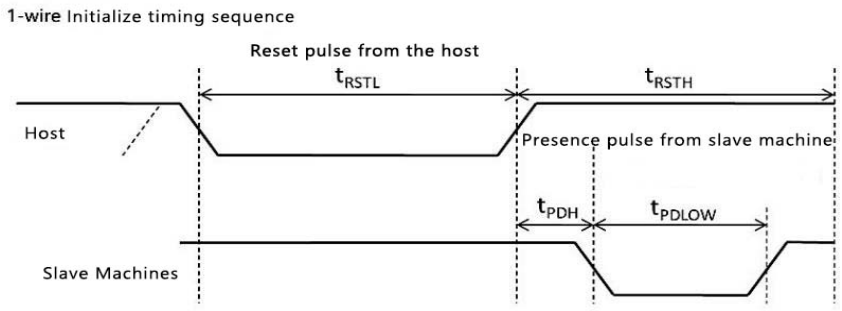



Figure 6 Initialization timing (host timing above, slave timing below)

## Overview

To ensure sufficient energy for the HX18B20-T during temperature conversion or EEPROM operations, a strong pullup must be provided to the single bus using a MOSFET, as shown in Figure 8. The bus must switch to this state within 10 microseconds after issuing the relevant command and remain so during the operation.

Alternatively, the HX18B20-T can be powered externally through the VDD pin, eliminating the need for a strong pullup and keeping the bus from staying high during temperature conversion, as shown in Figure 9.

Parasitic power supply mode is not recommended above 100°C due to increased leakage current. In such cases, powering the HX18B20-T through the VDD pin is strongly advised.

The HX18B20-T can indicate its power supply mode to the host by responding to specific commands. If the device is in parasitic power supply mode, it will pull the bus low, indicating to the host that a strong pullup is needed during temperature conversion.

The HX18B20-T offers a reliable temperature alarm mechanism and can be powered either externally or in parasitic mode, making it useful in various applications. However, during high-current operations like temperature conversion or EEPROM writes, additional current may be required that cannot be provided by parasitic power alone.

## Temperature measurement operation

HX18B20-T is a direct digital temperature sensor that supports programmable resolutions ranging from 9 to 12 bits, corresponding to temperature resolutions of 0.5°C to 0.0625°C. Upon powering up, it defaults to a 12-bit resolution and maintains a low-power standby state. When temperature measurement is required, the host sends a command to initiate AD conversion, and the converted data is stored in the temperature register upon completion. When powered by an external source, the host can determine the conversion status through read timing; however, this is not possible when powered by a parasitic source. HX18B20-T is suitable for efficient digital temperature measurement in various power supply scenarios.

## Alarm operation

After completing the temperature conversion, HX18B20-T compares the measured temperature value with user-defined alarm thresholds stored in the TH and TL registers (as shown in Figure 11). **This function is only applicable in 11-bit and 12-bit modes**. The comparison result is indicated by a sign bit (S), where S=0 represents a positive temperature and S=1 represents a negative temperature. Notably, the TH and TL registers are non-volatile (EEPROM), meaning their stored data remains preserved even after power loss.

| BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|---|---|---|---|---|---|---|---|
| S | $2^6$ | $2^5$ | $2^4$ | $2^3$ | $2^2$ | $2^1$ | $2^0$ |

**Figure 7TH and TL register formats**

## Power supply for HX18B20-T

TH and TL are 8-bit registers compared with bits 4-11 of the temperature register. An alarm is triggered if the temperature exceeds TH or falls below TL, setting an internal flag. This flag is updated with each temperature conversion and turned off if the alarm condition clears.

The host controller detects alarm flags by sending an alarm search command. Responsive HX18B20-Ts pinpoint alarm conditions. Changing TH or TL while an alarm is active reconfirms the condition.

HX18B20-T offers a reliable temperature alarm mechanism and can operate with external power or in parasitic mode, useful for remote and space-constrained applications.

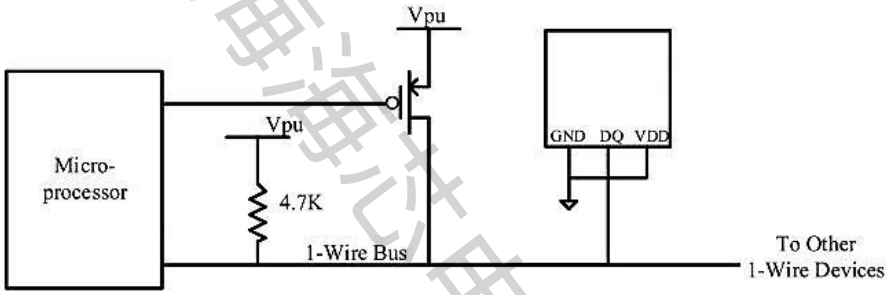
In parasitic mode, the device "steals" energy from the bus and stores it in an internal capacitor. The VDD pin must be grounded. While sufficient current is usually provided, during temperature conversion or EEPROM writing, the current may require more than the parasitic supply can offer. To ensure sufficient energy for the HX18B20-T during temperature conversion or EEPROM operations, a strong pullup must be provided to the single bus using a MOSFET, as shown in Figure 8. The bus must switch to this state within 10 microseconds after issuing the relevant command and remain so during the operation.

Alternatively, the HX18B20-T can be powered externally through the VDD pin, eliminating the need for a strong pullup and keeping the bus from staying high during temperature conversion, as shown in Figure 9.

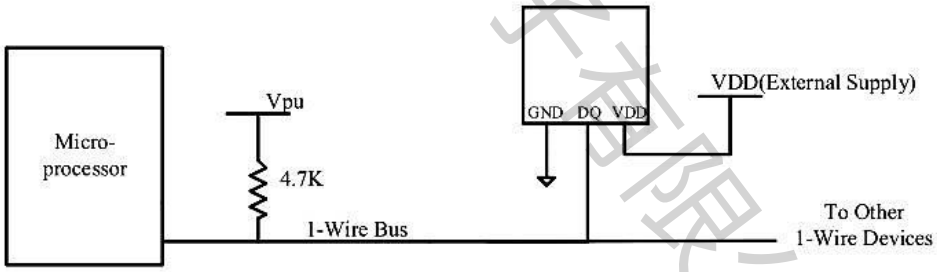
Parasitic power supply mode is not recommended above 100°C due to increased leakage current. In such cases, powering the HX18B20-T through the VDD pin is strongly advised.

The HX18B20-T can indicate its power supply mode to the host by responding to specific commands. If the device is in parasitic power supply mode, it will pull the bus low, indicating to the host that a strong pullup is needed during temperature conversion.

The HX18B20-T offers a reliable temperature alarm mechanism and can be powered either externally or in parasitic mode, making it useful in various applications. However, during high-current operations like temperature conversion or EEPROM writes, additional current may be required that cannot be provided by parasitic power alone.




Parasitic Power Supply Control Circuit (Fig. 8)




Power Supply Circuit for VDD Pin (Fig. 9)

## Detailed Description

Figure 1 illustrates the functional block diagram of the HX18B20-T, which includes a 64-BIT ROM for storing a unique chip serial number. The scratchpad has two bytes dedicated to storing temperature data, two bytes for the alarm threshold registers Th and Tl, and one byte for the configurable register Tc, which holds the user-set temperature conversion resolution value. The values in the alarm threshold registers and the configurable register can be copied to EEPROM using the copy scratchpad command (data is retained after power loss and automatically recalled to the registers upon power-on, or can be recalled using commands introduced below).

## Register

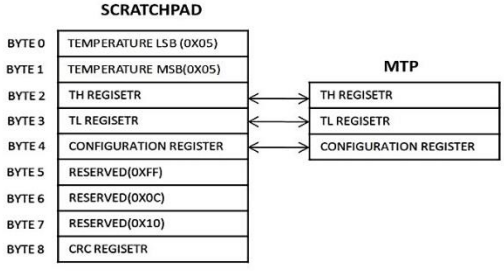



Figure 10: Block diagram of temporary memory

### BYTE 0~1:

The first two registers are used to store temperature data and are read-only. Bits 11 to 15 of the temperature data represent the sign bit, bits 4 to 11 represent the integer part, and bits 0 to 3 represent the fractional part.
The number of bits read for temperature data varies based on the resolution. When the resolution is 9 bits, bits 3 t o 11 are read; for 10 bits, bits 2 to 11; for 11 bits, bits 1 to 11; and for 12 bits, bits 0 to 11 are read.
The detailed information is shown in Figure 11, where LSB represents low data bits and MSB represents high data bits

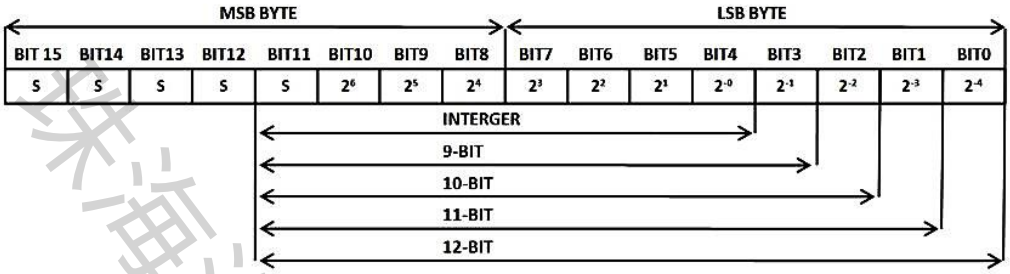



**Figure 11: Distribution of Temperature Register Data**

### BYTE 2~4:

BYTE2 and BYTE3 are configured with temperature alarm upper and lower thresholds; BYTE 4 is a register for configuring temperature conversion resolution, and its format is shown in Figure 8.

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| S | R1 | R2 | 1 | 1 | 1 | 1 | 1 |

**Figure 12 Format of Resolution Configuration Register**

The specific values for setting the resolution (configuring R1 and R2) are as follows

| R1 | R2 | Resolution |
|---|---|---|
| 0 | 0 | 9-bit |
| 0 | 1 | 10-bit |
| 1 | 0 | 11-bit |
| 1 | 1 | 12-bit |

**Resolution configuration values and corresponding resolutions**

### BYTE 5~7:

Reserved byte positions, with read-only attributes, and default values as shown in Figure 7.

### BYTE 8:

The CRC check bit stores the check data, and the check principle is described in the CRC check code generator below.

## 64 bit ROM encoding with flexible settings

Each chip has a unique 64-bit ROM code. Figure 13 illustrates the format of the 64-bit ROM code, with the lowest 8 bits being the coding for the HX18B20-T series: 28h. Following this is a 48-bit unique serial number. The highest 8 bits are the CRC code of the preceding 56 bits. For a detailed explanation of CRC, see the CRC generator section. The 64-bit ROM and ROM control area allow the HX18B20-T to function as a single-bus device and operate according to the detailed single-bus protocol.

| | | |
|---|---|---|
| 8-bit CRC | 48-bit Serial Number | 8-bit Family Code(0x80) |

**Figure 13 illustrates the format of the 64-bit ROM code.**

## EEPROM

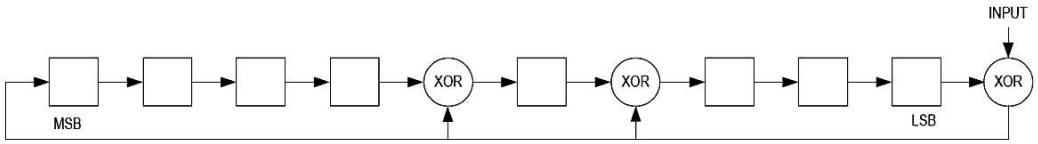
This function module stores user-defined information, including temperature alarm values and resolution settings. Users can copy these data from registers to EEPROM to prevent loss during power failure. After power-on, users can retrieve the data from EEPROM to registers by executing the Recall E² command at any time.

## CRC Checksum Generator

After power-on, the CRC checksum generator recalculates the CRC checksum every time the scratchpad data is updated, as the data stored in the scratchpad is included in the CRC calculation.

The CRC calculation formula is as follows: CRC=X8+X5+X4+1

Figure 14 is a schematic diagram of the CRC checksum generator.




**The principle of the CRC checksum generator in Figure 14.**

## Temperature/Data Relationship Table

The main function of this sensor is to convert the sensed temperature into a digital signal output. Below is the corresponding output when the temperature conversion resolution is 12 bits.

| Temperature℃ | Digital output (binary) | Digital output (hexadecimal) |
|---|---|---|
| 125 | 0000011111010000 | 07D0h |
| 85 | 0000010101010000 | 0550h |
| 25.0625 | 0000000110010001 | 0191h |
| 10.125 | 0000000010100010 | 00A2h |
| 0.5 | 0000000000001000 | 0008h |
| 0 | 0000000000000000 | 0000h |
| -0.5 | 1111111111111000 | FFF8h |
| -10.125 | 1111111101011110 | FF5Eh |
| -25.0625 | 1111111001101111 | FE6Fh |
| -55 | 1111110010010000 | FC90h |

**The correspondence between temperature T and digital signals**

The positive temperature value = ADC digital output * 0.0625;

"Negative temperature value = (~ADC_digital_output + 1) * 0.0625;"

## Instruction Description

### HX18B20-T Rom Command Search ROM[F0h]:

To search for the number of HX18B20-T devices attached to the bus and their corresponding ROM codes, the host needs to continuously execute this command until the last HX18B20-T is found.

### Read ROM[33h]:

Perform this when only one HX18B20-T is present on the bus to obtain its ROM code. If more than one HX18B20-T is connected to the bus, executing this command will cause a conflict.

### Match ROM[55h]:

Execute on the known ROM-coded HX18B20-T to allow the host to operate it. Other HX18B20-Ts will wait for the reset pulse.

### Skip ROM[CCh]:

Use Skip ROM [CCh] for same op on all HX18B20-Ts. Note: Only one HX18B20-T for Read Scratchpad [BEh] after Skip ROM to avoid undefined values.

### Alarm Search[ECh]:

When the alarm flag is triggered on an HX18B20-T, execute to allow the alerting HX18B20-T to respond to the host. It does not support 9-bit and 10-bit operations and will remain in the alarm state indefinitely.

### HX18B20-T Function Command

### Convert T[44h]:

Execute a single instruction to perform a temperature conversion, and enter standby mode upon completion. If the conversion is not completed, send '0' to the bus; if completed, send '1'. Write Scratchpad [4Eh ]: Allows writing 3 bytes of data to the scratchpad of HX18B20-T. (Abbreviation meanings remain unchanged.)

### Read Scratchpad[BEh]:

Read all data from the register, starting from the least significant bit of byte 0 up to byte 8. The command can be terminated at any time by issuing a reset instruction.

**Copy Scratchpad[48h]:**

Copy data from BYTE 2, BYTE 3, and BYTE 4 of the register to the EEPROM. After executing this command, delay for 12ms before performing other operations.

**Recall E²[B8h]:**

Load EEPROM data into regs BYTE 2-4 auto/manual. Send '0' during, '1' upon finish. Wait 2ms post-execution.

**Read Power Supply [B4h]:**

To determine the operating mode (parasitic mode or externally powered mode) of the HX18B20-T, the bus level is used for judgment.

## HX18B20-T Function Instruction Table

| COMMAND | DESCRIPTION | PROTOCOL | 1-Wire Bus Activity after Command is Issued | Notes |
|---|---|---|---|---|
| **TEMPERATURE CONVERSION COMMANDS** | | | | |
| Conv T | Initiates temperature conversion | 44h | HX18B20-T transmits conversion status to master | A |
| **MEMORY COMMANDS** | | | | |
| Read Scratchpad | Reads the entire scratchpad including the CRC byte. | BEh | HX18B20-T transimits up to 9 data bytes to master | B |
| Write Scratchpad | Writes data to scratchpad bytes2,3,and4(TH,TL,and configuration registers) | 4Eh | Master transmits 3 data bytes to HX18B20-T | C |
| Copy Scratchpad | Copies TH,TL and configuration register data from the scrathchpad to EEPROM | 48h | None | A |
| Recall E² | Recalls TH,TL,config register and User Bytes data from EEPROM to the scrachpad | B8h | HX18B20-T transmits recall status to | |
| Read Power Supply | Signals HX18B20-T power supply mode to the master | B4h | HX18B20-T transmit supply status to | |

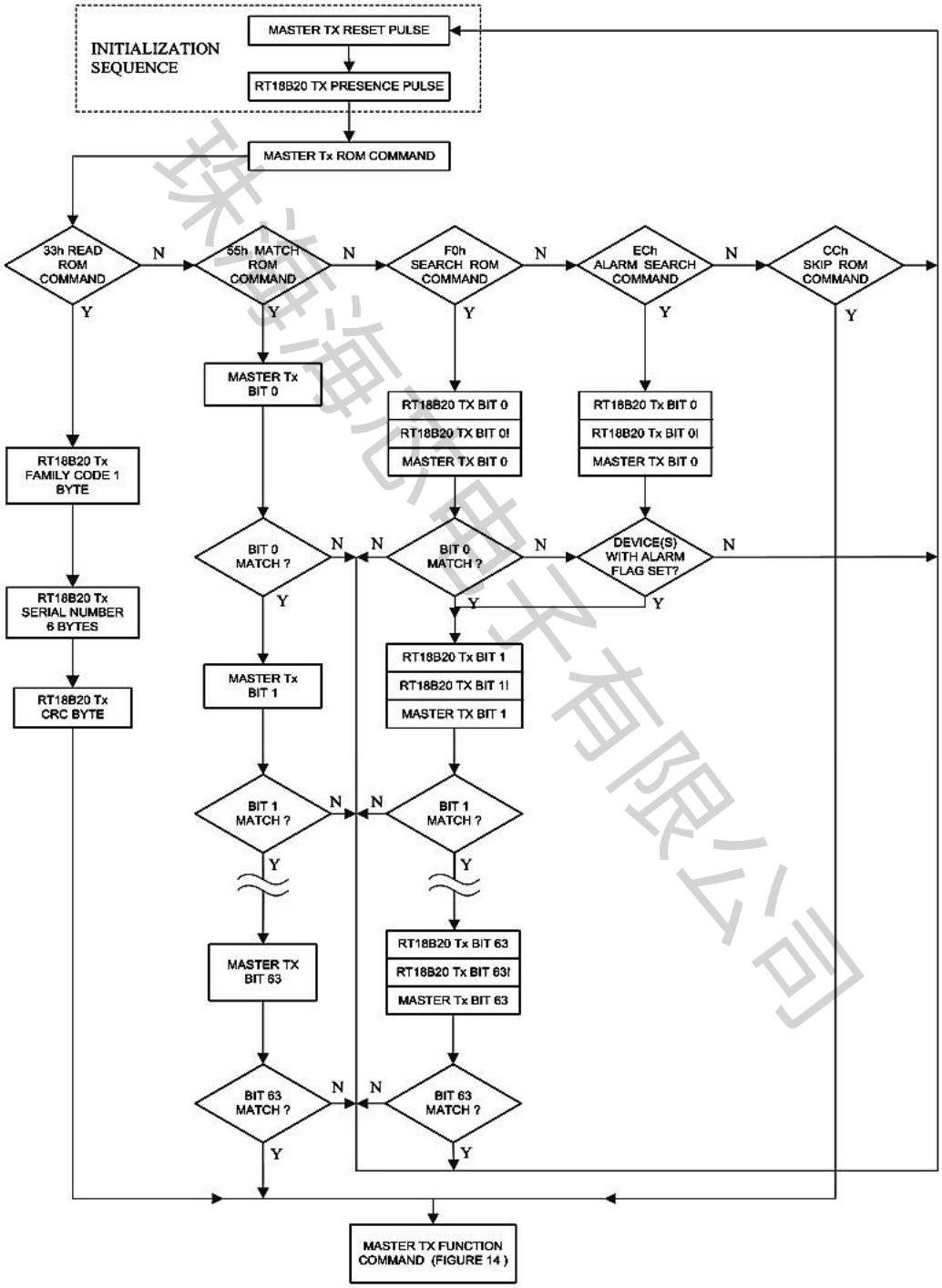
## Notes

A. During temperature conversion and data copying to EEPROM in parasite power mode, HX18B20-T requires a strong pullup on the bus, with no other bus activity during this time.

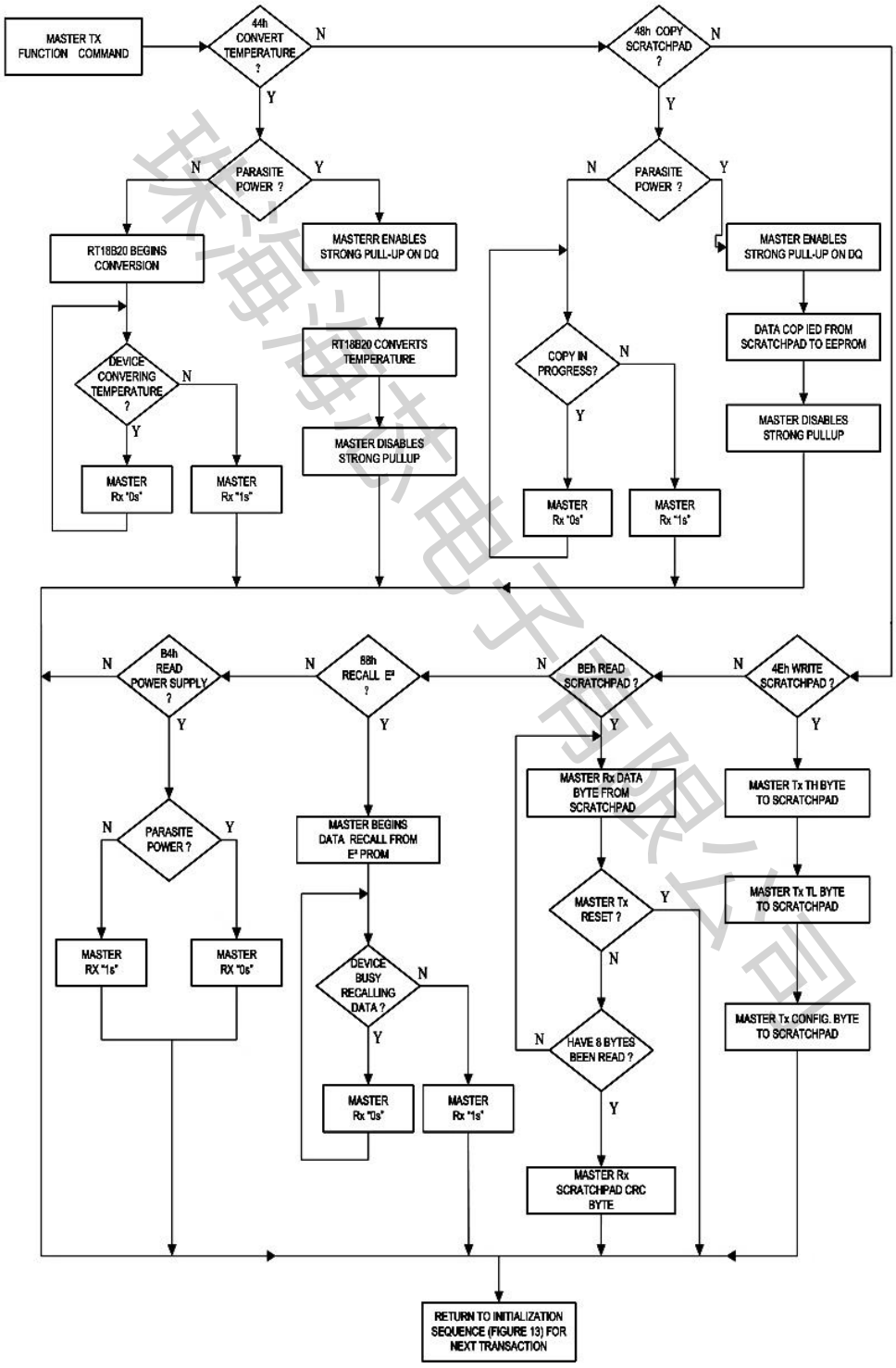
B. The bus controller can terminate data transmission at any time by issuing a reset signal.

C. The writing of the three bytes: TH, TL, and the configuration register, must be completed before initiating the reset signal.

## ROM instruction flowchart



## Functional Instruction Flow Chart



## Instruction Execution Flow and Timing Sequence

As shown in Figure 15, the entire instruction execution process consists of three steps: initialization, ROM command execution, and function command execution. After completing one operation, it returns to Step 1 for reinitialization, and this cycle repeats. It is important to note that the reset command has a fixed timing sequence, while the timing sequences for ROM and function commands vary depending on the specific operation. The execution of all commands is based on read and write timing sequences.


Figure 15: Instruction Execution Flow

### Initialization

The initialization process involves the host sending a reset pulse and receiving a presence pulse from the HX18B20-T. During the reset signal, the host pulls the bus low for at least 480us, then releases it and waits for 15 to 60 us. The HX18B20-T responds with a presence pulse of 60us to 240us in width. Upon receiving the presence pulse from the HX18B20-T, the complete reset process ends. After ending the reset pulse, the host must wait at least 480us before releasing the bus.

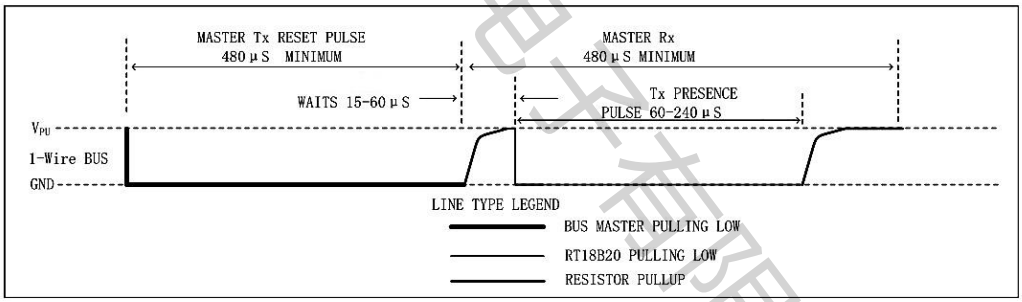



Figure 16 Initialization Timing

Note: Initialization cannot be performed repeatedly; an instruction must be executed between two INIT operations.

### Write Time Slot

This timing sequence is for writing a single bit (0 or 1) to the HX18B20-T. To write a 0, the host pulls the bus low between 60us and 120us. To write a 1, the bus is pulled low for at least 1us and released within 15us. The HX18B20-T samples the bus between 15us and 60us after the start of the write slot. If the bus is low during sampling, the received data is 0; if high, it's 1. All write slots must last at least 60us, with at least 1us recovery time between consecutive slots, as shown in Figure 17.

### Read Time Slot

This timing sequence is for reading a single bit (0 or 1) from the HX18B20-T. When the host initiates a read sequence, it pulls the bus low for at least 1 microsecond and then immediately releases it. The HX18B20-T responds by transmitting one bit of data to the host. During data transmission, the HX18B20-T transmits a '1' or '0' by pulling the bus high or low, respectively. After transmitting a '0', the bus is released and returns to its high, idle state due to the pullup resistor. The data output by the HX18B20-T is valid within 15 microseconds of the falling edge of the read sequence, so the host must release the bus and read its state within this 15-microsecond window after initiating the read sequence. As with write slots, all read slots must last at least 60 microseconds, and there must be at least a 1-microsecond gap between consecutive read slots.

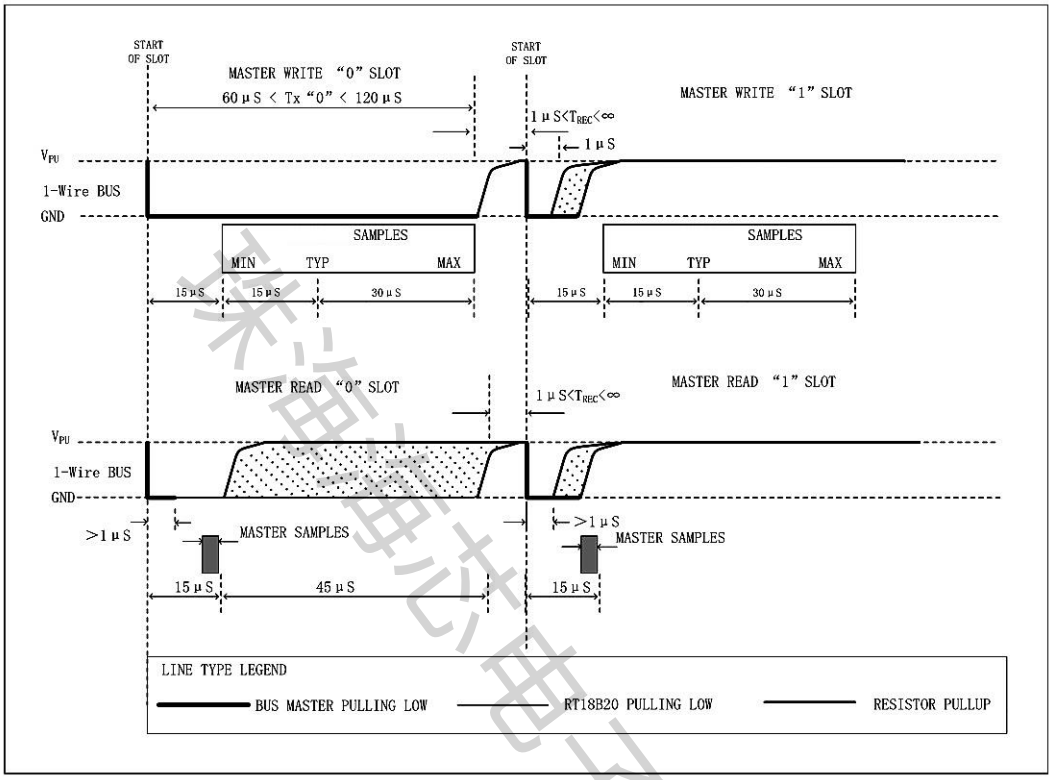



**Figure 17 Read/Write Time Slot Timing Diagram**

Figure 18 indicates that the sum of TINT, TRC, and TSAMPLE must be less than 15us. Figure 19 highlights how to maximize system timing by keeping TINT and TRC as short as possible and positioning the host's sampling time at the end of the 15us cvcle.

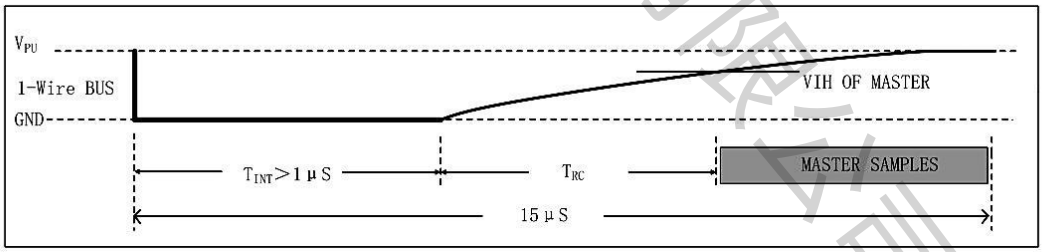
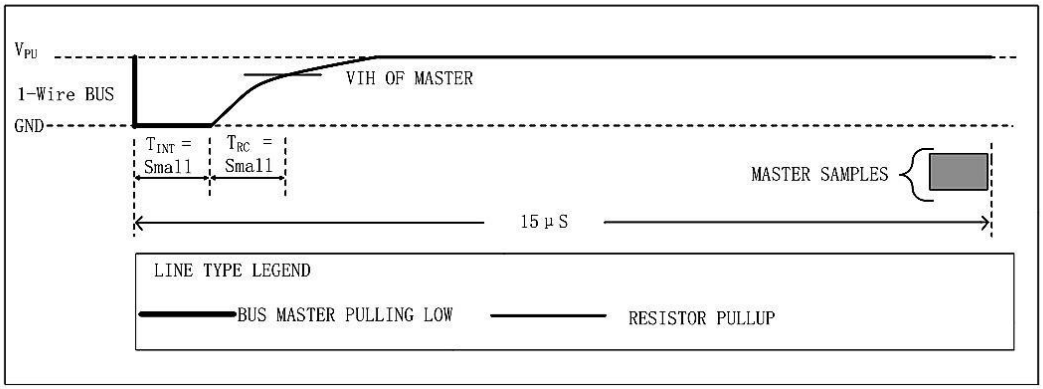



**Figure 18 Detailed timing seq uence for reading ' 1'**




**Recommended timing seq uence for reading ' 1' in Figure 19**

# Application Information

## Interface Configuration

In idle state, the single bus is high (pulled up). To abort a transmission, the bus must return to idle before resuming. Thus, the recovery time between read/write slots can be infinite as long as the bus stays high (idle). If the bus is pulled low for more than 480us, the chip will reset unconditionally. Fig. 20 shows the connection between the host and slave, with a minimum 4.7K resistor required on the bus.

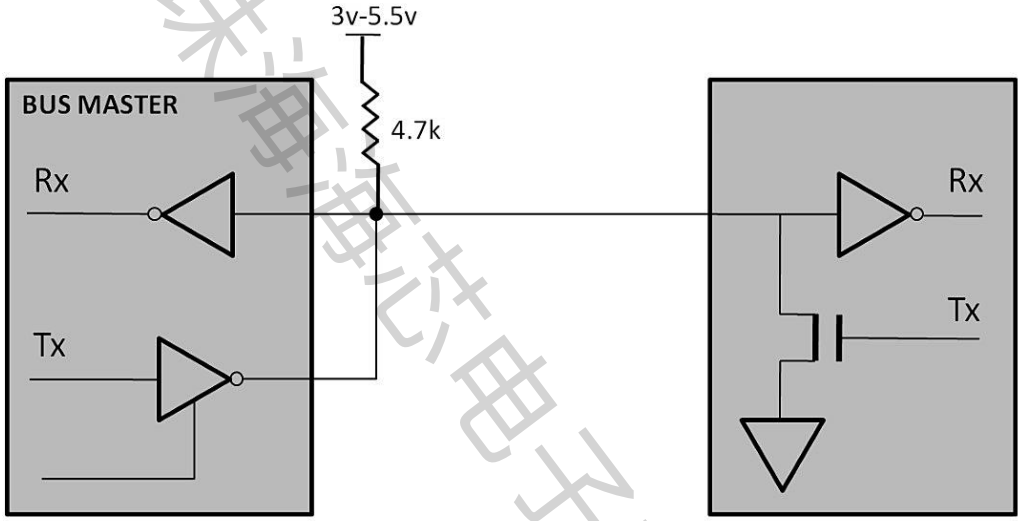



**Figure 20HX18B20-T and Host Connection Diagram**

X18B20-T Operation Example 1

| MASTER MODE | DATA(LSB FIRST) | COMMENTS |
|---|---|---|
| Tx | Reset | Master issues reset pulse. |
| Rx | Presence | HX18B20-Ts respond with presence pulse. |
| Tx | 55h | Master issues Match Rom command. |
| Tx | 64-bit ROM code | Master sends HX18B20-T ROM code. |
| Tx | 44h | Master issues Conver T command. |
| Tx | DQ line held high by strong pullup | Master applies strong pullup to DQ for the duration of the conversion(tCONV) |
| Tx | Reset | Master issues reset pulse. |
| Rx | Presence | HX18B20-Ts respond with presence pulse. |
| Tx | 55h | Master issues Match Rom command. |
| Tx | 64-bit ROM code | Master sends HX18B20-T ROM code. |
| Tx | BEh | Master issues Read Scratchpad command.. |
| Rx | 9 data bytes | Master reads entire scratchpad including CRC.The master then recalculates the CRC of the first eight data bytes from the scratchpad and compares the calclulated CRC with the read CRC (byte 9). if they match, the master continues; if not, the read operation is repeated. |

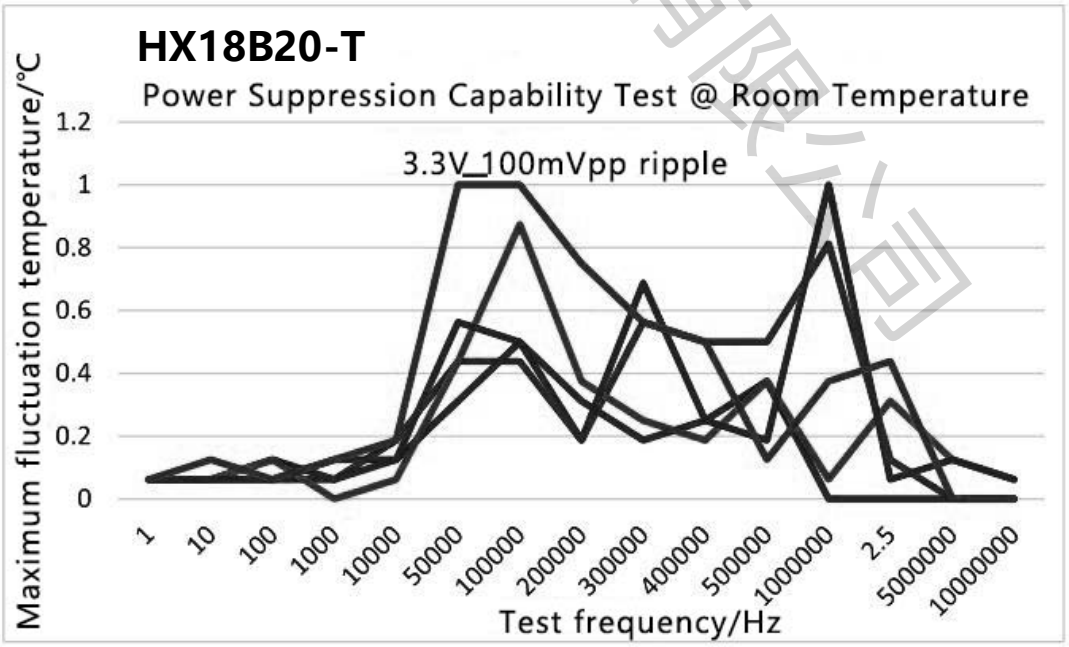
## Example of HX18B20-T Operation 2

In this example, there is only one HX18B20-T chip on the bus, operating in parasitic power mode. The bus controller first writes to the TH, TL, and configuration registers, then reads the register results and verifies data accuracy using a CRC checksum algorithm. Afterward, the host copies the data from the registers to the EEPROM using a COPY command.

| MASTER MODE | DATA (LSB FIRST) | COMMENTS |
|---|---|---|
| Tx | Reset | Master issues reset pulse. |
| Rx | Presence | HX18B20-Ts respond with presence pulse. |
| Tx | CCh | Master issues Skip ROM command |
| Tx | 4Eh | Master issues Write Scratchpad command. |
| Tx | 3 data bytes | Master sends three data bytes to |
| Tx | Reset | Master issues reset pulse. |
| Rx | Presence | HX18B20-Ts respond with presence pulse. |
| Tx | CCh | Master issues Skip ROM command |
| Tx | BEh | Master sends HX18B20-T ROM command. |

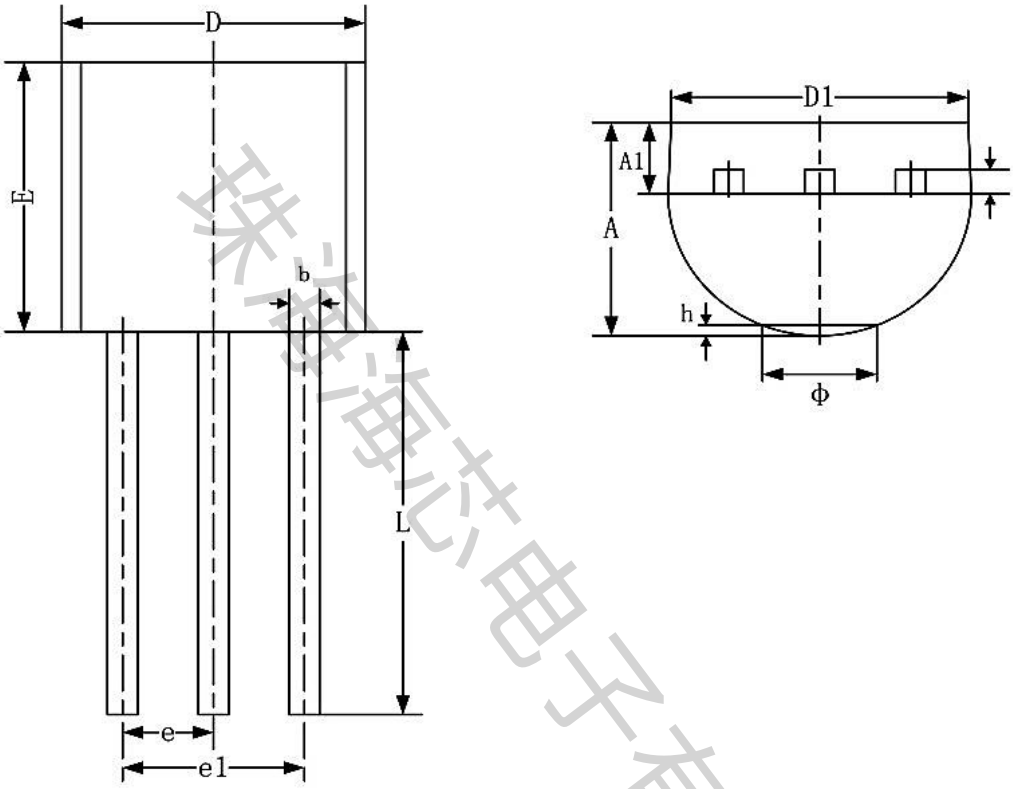
## Precautions

1. After powering on the chip, wait for 2ms before operating it to ensure the first command is received p roperly.
2. To ensure a stable temperature output of the chip, it is recommended to filter the power supply with a ripple of at least 1KHz.



## Package Specifications

### TO-92 (Package Outline Dimensions)






| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| A | 3.300 | 3.700 | 0.130 | 0.146 |
| A1 | 1.100 | 1.400 | 0.043 | 0.055 |
| b | 0.380 | 0.550 | 0.015 | 0.022 |
| c | 0.360 | 0.510 | 0.014 | 0.020 |
| D | 4.400 | 4.700 | 0.173 | 0.185 |
| D1 | 3.430 | | 0.135 | |
| E | 4.300 | 4.700 | 0.169 | 0.185 |
| e | 1.270TYP | | 0.050TYP | |
| e1 | 2.440 | 2.640 | 0.096 | 0.104 |
| L | 14.100 | 14.500 | 0.555 | 0.571 |
| φ | | 1.600 | | 0.063 |
| h | 0.000 | 0.380 | 0.000 | 0.015 |