

Silicon N-Channel Power MOSFET

Description

The IRF740STRL uses advanced technology and design to provide excellent $R_{DS(ON)}$. It can be used in a wide variety of applications.

General Features

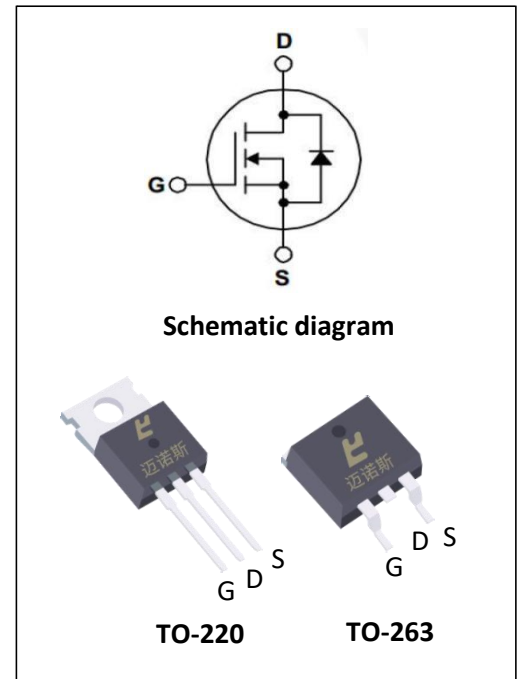
- ① $V_{DS}=400V, I_D=10A$
- ② Low ON Resistance
- ③ Low Reverse transfer capacitance
- ④ 100% Single Pulse avalanche energy Test

Application

- ① Power switching application
- ② Adapter and charger

Package Marking And Ordering Information:

| Ordering Codes | Package | Product Code | Packing |
|----------------|---------|--------------|---------|
| IRF740PBF | TO-220 | IRF740 | Tube |
| IRF740STRL | TO-263 | IRF740S | Tube |



Absolute Maximum Ratings ($T_c=25^\circ\text{C}$ unless otherwise specified)

| Symbol | Parameter | Value | Units |
|-----------|--|-------|------------------|
| V_{DSS} | Drain-to-Source Breakdown Voltage | 400 | V |
| I_D | Drain Current (continuous) at $T_c=25^\circ\text{C}$ | 10 | A |
| I_{DM} | Drain Current (pulsed) | 40 | A |
| V_{GS} | Gate to Source Voltage | +/-30 | V |
| P_{tot} | Total Dissipation at $T_c=25^\circ\text{C}$ | 100 | W |
| T_j | Max. Operating Junction Temperature | 175 | $^\circ\text{C}$ |
| E_{AS} | Single Pulse Avalanche Energy | 424 | mJ |

Thermal characteristics

| Symbol | Parameter | Typ | Units |
|-----------------|------------------|-----|---------------------------|
| $R_{\theta JC}$ | Junction-to-Case | 1.5 | $^\circ\text{C}/\text{W}$ |

Electrical Parameters(at $T_c = 25^\circ\text{C}$, unless otherwise specified)

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|--------------|--------------------------------------|-----------------------------------|-----|------|------|------------|
| V_{DS} | Drain-source Voltage | $V_{GS}=0V, I_D=250\mu A$ | 400 | -- | -- | V |
| $R_{DS(on)}$ | Static Drain-to-Source on-Resistance | $V_{GS}=10V, I_D=5A$ | -- | 400 | 500 | m Ω |
| $V_{GS(th)}$ | Gated Threshold Voltage | $V_{DS}=V_{GS}, I_D=250\mu A$ | 2.0 | -- | 4.0 | V |
| I_{DSS} | Drain to Source leakage Current | $V_{DS}=400V, V_{GS}=0V$ | -- | -- | 1.0 | μA |
| $I_{GSS(F)}$ | Gated Body Forward Leakage | $V_{GS}=+30V$ | -- | -- | 100 | nA |
| $I_{GSS(R)}$ | Gated Body Reverse Leakage | $V_{GS}=-30V$ | -- | -- | -100 | nA |
| C_{iss} | Input Capacitance | $V_{GS}=0V, V_{DS}=25V, f=1.0MHz$ | -- | 1162 | -- | pF |
| C_{oss} | Output Capacitance | | -- | 160 | -- | pF |
| C_{rss} | Reverse Transfer Capacitance | | -- | 17 | -- | pF |

Switching Characteristics

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|--------------|---------------------|--------------------------------------|-----|------|-----|------|
| $t_{d(on)}$ | Turn-on Delay Time | $V_{DD}=200V, I_D=11A, R_G=10\Omega$ | -- | 16.5 | -- | nS |
| t_r | Turn-on Rise Time | | -- | 20.8 | -- | nS |
| $t_{d(off)}$ | Turn-off Delay Time | | -- | 46.9 | -- | nS |
| t_f | Turn-off Fall Time | | -- | 18.5 | -- | nS |
| Q_g | Total Gate Charge | $V_{DS}=320V, I_D=11A, V_{GS}=10V$ | -- | 32 | -- | nC |
| Q_{gs} | Gate-Source Charge | | -- | 5 | -- | nC |
| Q_{gd} | Gate-Drain Charge | | -- | 15 | -- | nC |

Source-Drain Diode Characteristics

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|--|--------------------------------|--|-----|-----|------|---------|
| I_{SD} | S-D Current(Body Diode) | | -- | -- | 10 | A |
| I_{SDM} | Pulsed S-D Current(Body Diode) | | -- | -- | 40 | A |
| V_{SD} | Diode Forward Voltage | $V_{GS}=0V, I_{DS}=18A$ | -- | -- | 1.5 | V |
| t_{rr} | Reverse Recovery Time | $T_J=25^\circ C, I_F=18A, di/dt=100A/us$ | -- | -- | 216 | nS |
| Q_{rr} | Reverse Recovery Charge | | -- | -- | 1640 | μC |
| *Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$ | | | | | | |

Characteristics Curves

Figure 1a Safe Operating Area (No FullPAK)

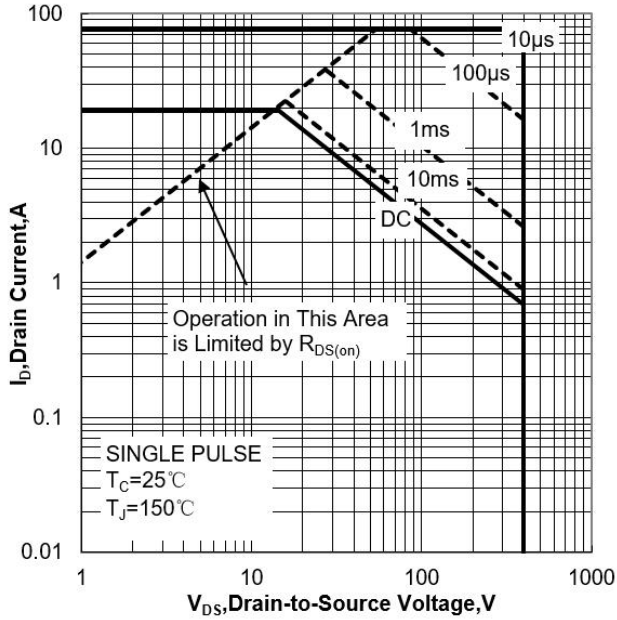


Figure 1b Safe Operating Area (FullPAK)

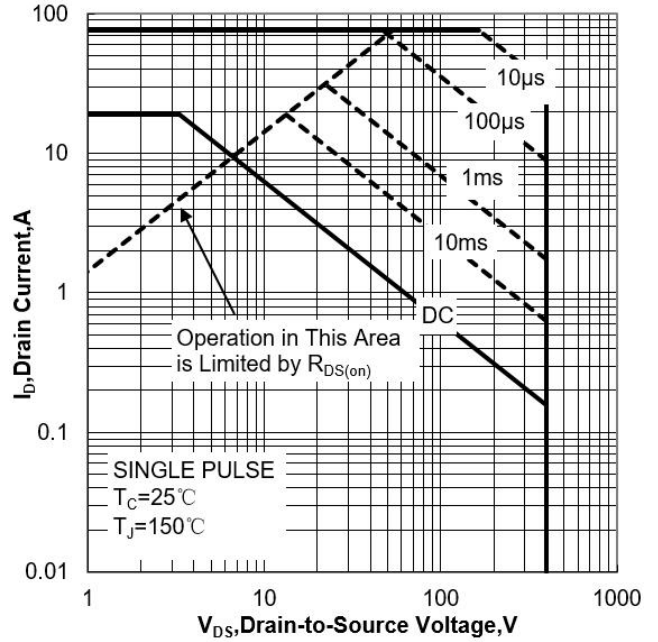


Figure 2a Power Dissipation (No FullPAK)

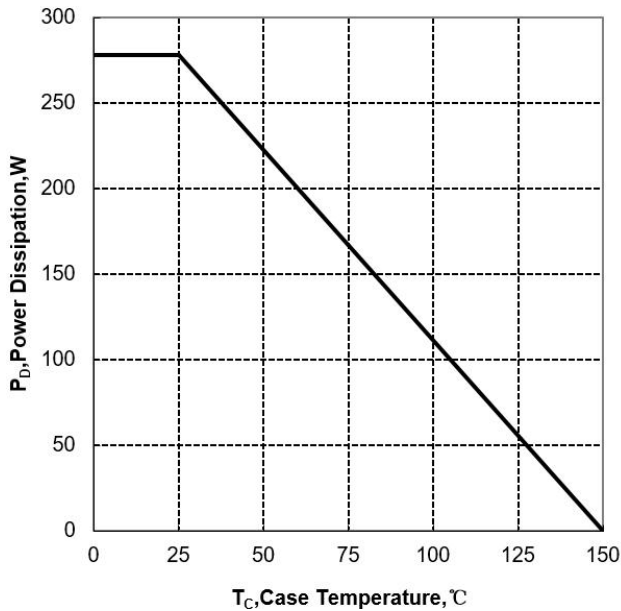


Figure 2b Power Dissipation (FullPAK)

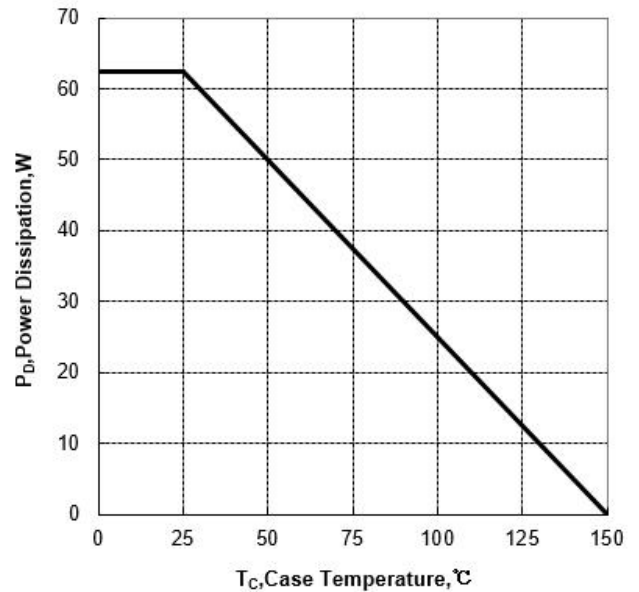


Figure 3a Max Thermal Impedance (No FullPAK)

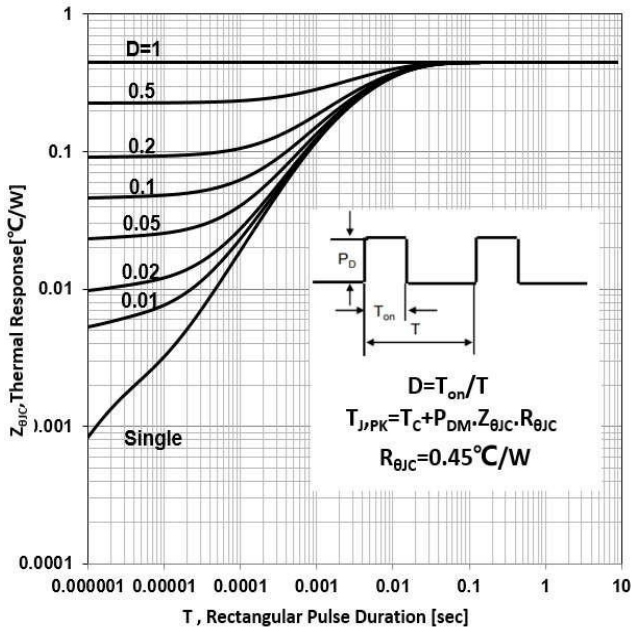


Figure 3b Max Thermal Impedance (FullPAK)

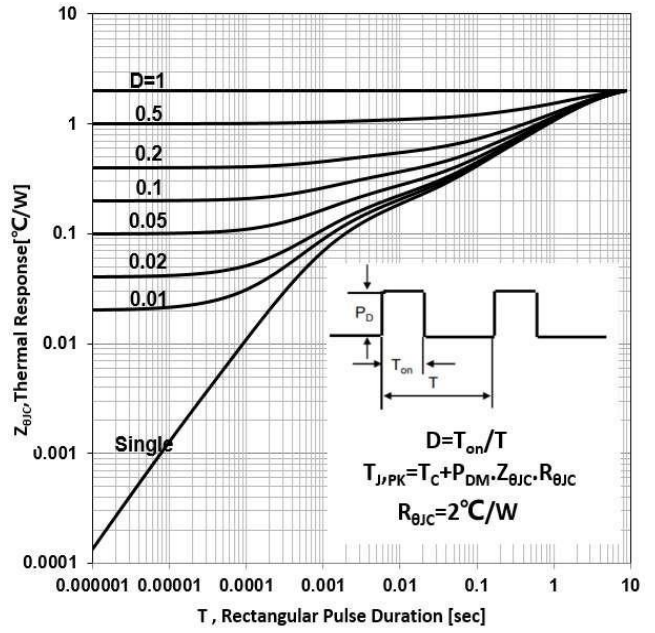


Figure 4 Typical Output Characteristics

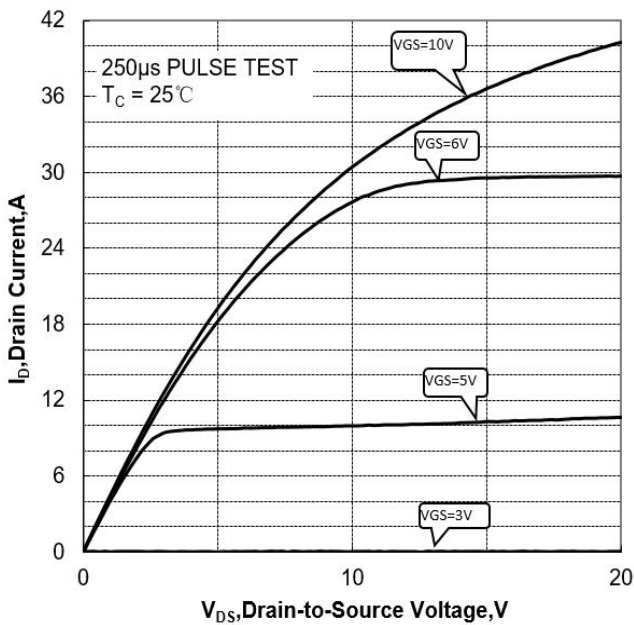


Figure 5 Typical Transfer Characteristics

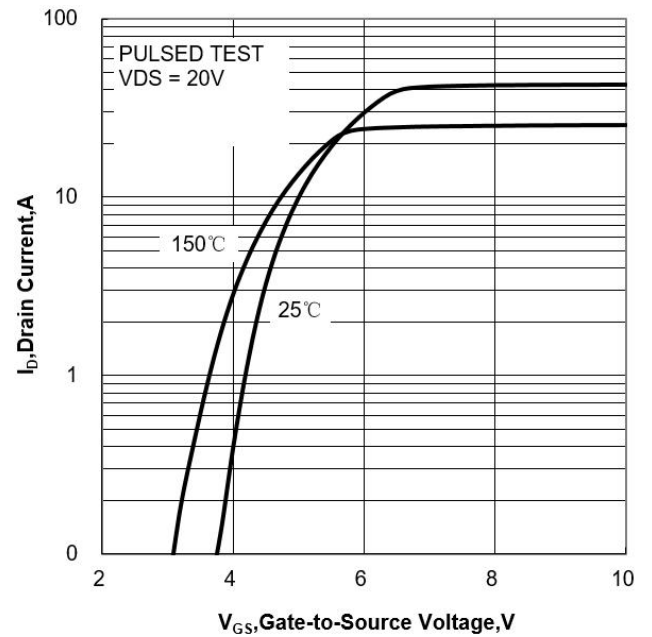


Figure 6 Typical Drain to Source ON Resistance vs Drain Current

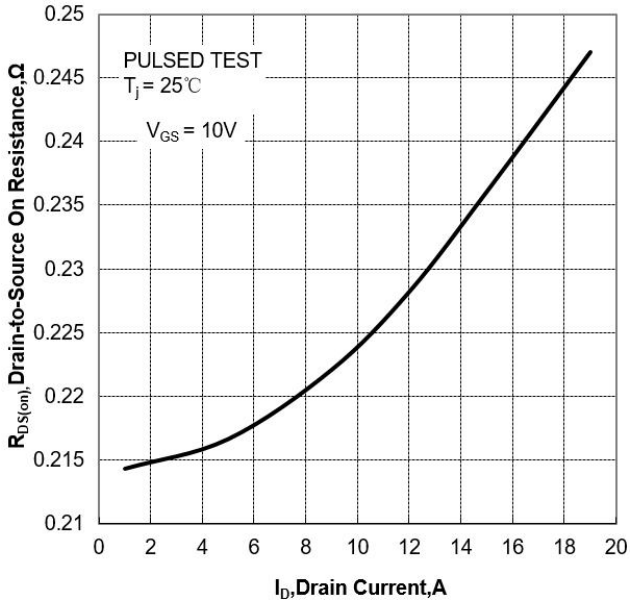


Figure 7 Typical Drain to Source on Resistance vs Junction Temperature

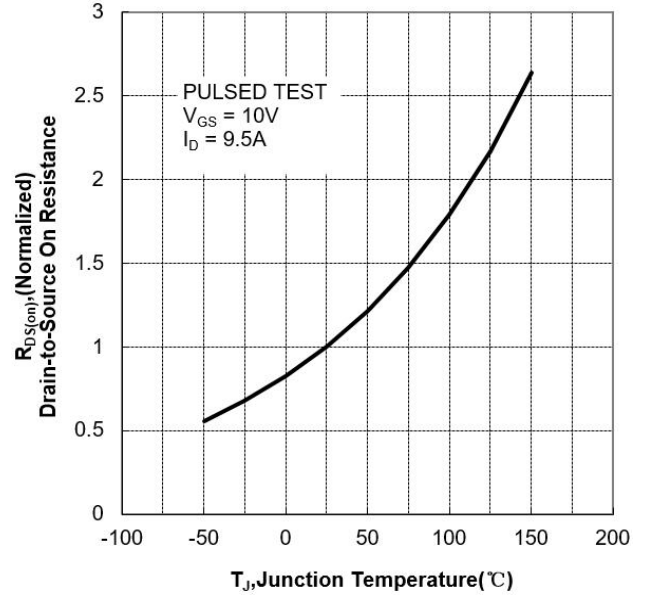


Figure 8 Typical Theshold Voltage vs Junction Temperature

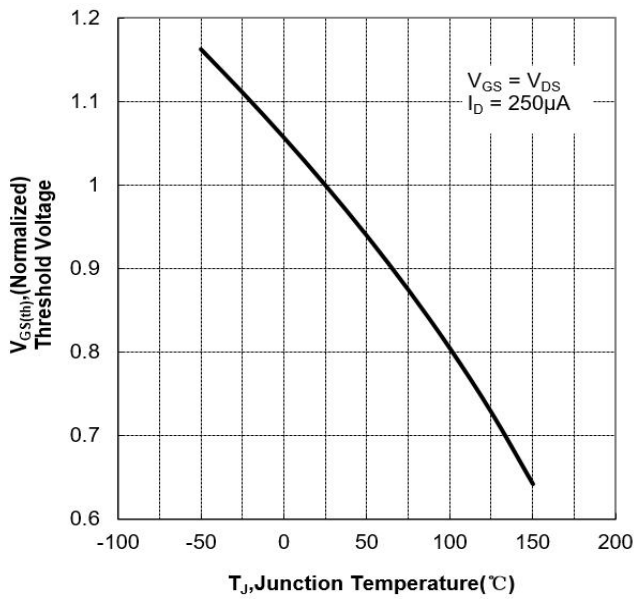


Figure 9 Typical Breakdown Voltage vs Junction Temperature

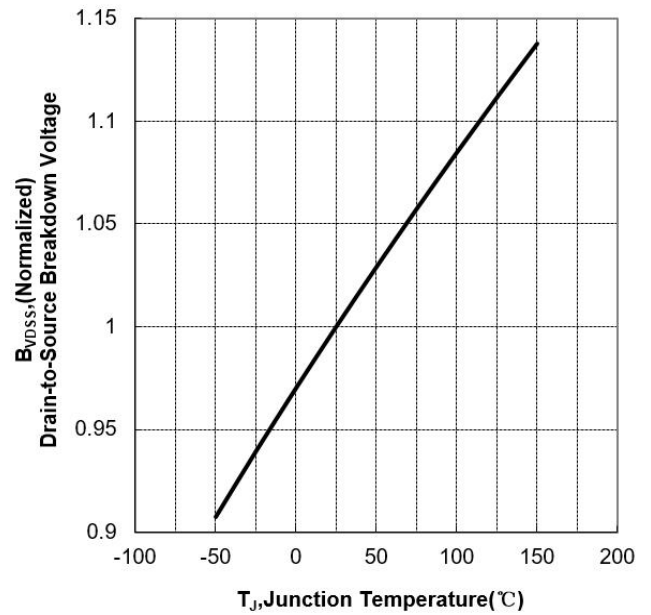


Figure 10 Typical Capacitance vs Drain to Source Voltage

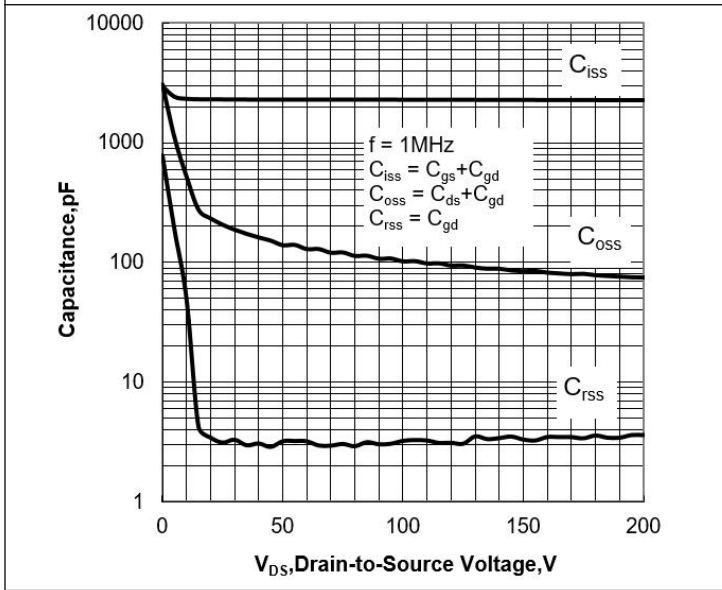
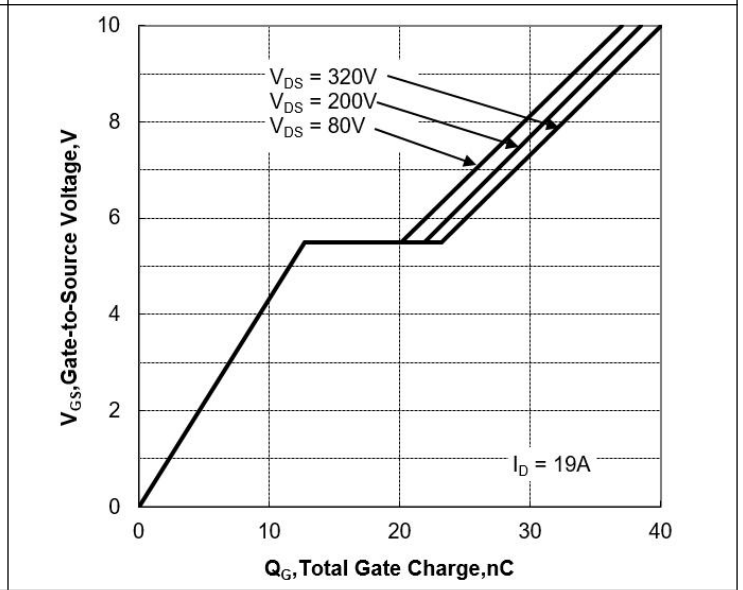
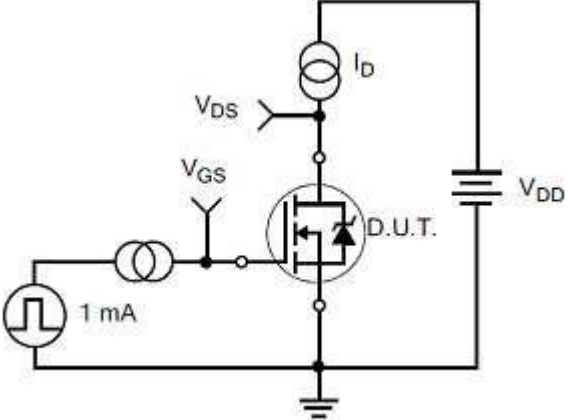
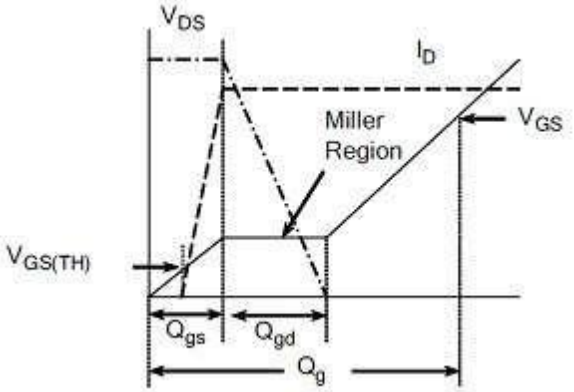
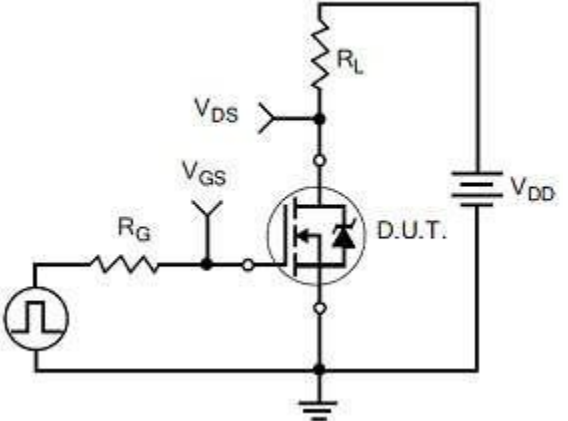
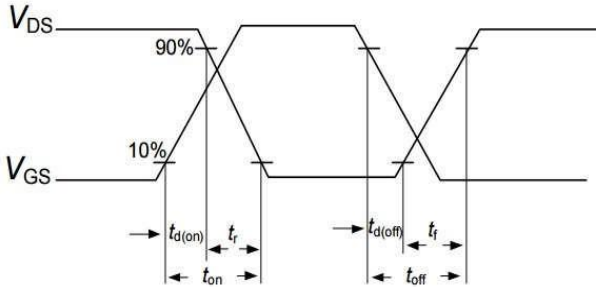
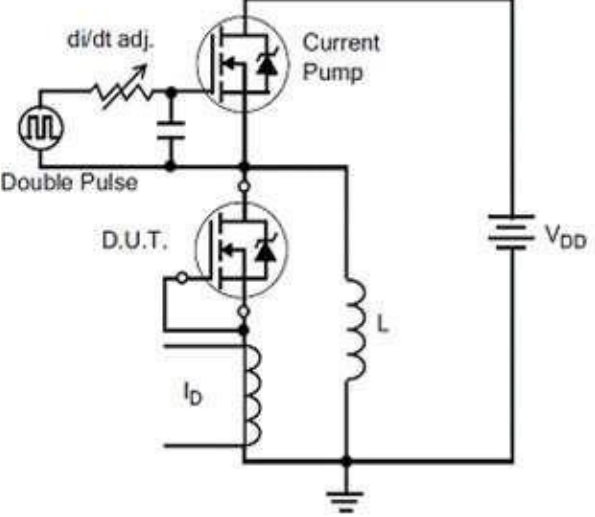
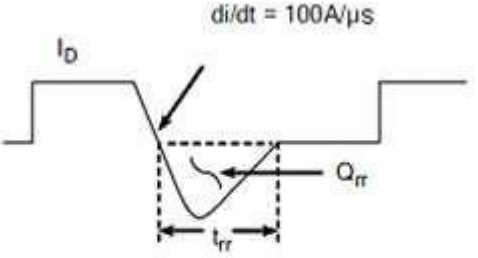
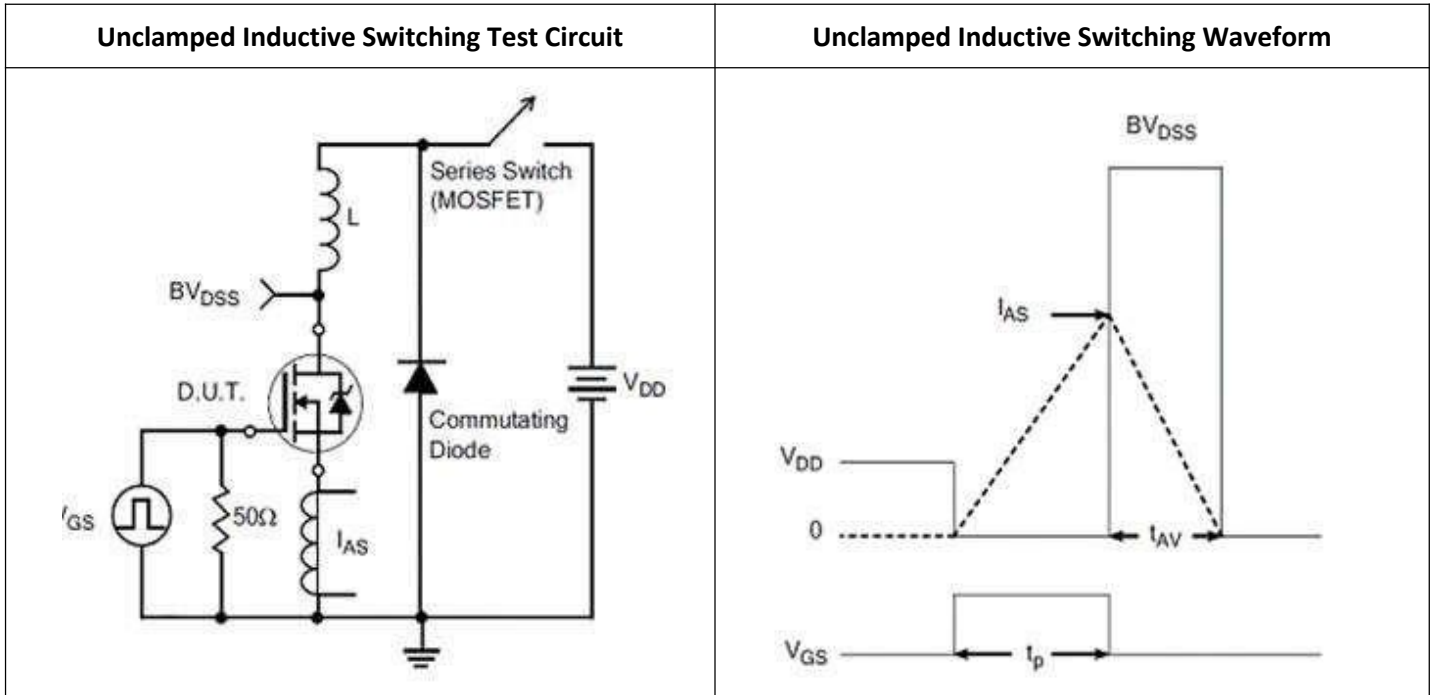


Figure 11 Typical Gate Charge vs Gate to Source Voltage

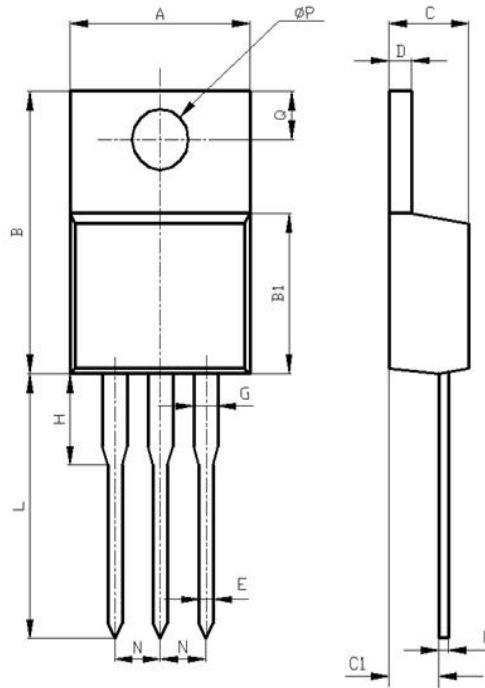


Test Circuit and Waveform

| Gate Charge Test Circuit | Gate Charge Waveforms |
|--|--|
|  <p>A circuit diagram for gate charge testing. It features a 1 mA current source connected to the gate of a D.U.T. (Device Under Test). The gate is also connected to a gate voltage measurement point V_{GS}. The drain is connected to a drain current measurement point I_D and a drain voltage measurement point V_{DS}. The circuit is powered by a V_{DD} supply.</p> |  <p>Waveform diagram showing V_{DS} and I_D versus V_{GS}. The V_{GS} waveform shows a threshold voltage $V_{GS(TH)}$, a Miller Region, and gate charge regions Q_{gs}, Q_{gd}, and Q_g.</p> |
| Resistive Switching Test Circuit | Resistive Switching Waveforms |
|  <p>A circuit diagram for resistive switching testing. It includes a gate resistor R_G and a load resistor R_L. The D.U.T. is connected between the gate and the load. The gate is driven by a pulse source, and the drain is connected to V_{DD}. Measurement points V_{GS} and V_{DS} are indicated.</p> |  <p>Waveform diagram showing V_{DS} and V_{GS} versus time. It illustrates the turn-on and turn-off transitions, with parameters $t_{d(on)}$, t_r, $t_{d(off)}$, and t_f. The V_{DS} waveform shows a 90% rise and a 10% fall.</p> |
| Diode Reverse Recovery Test Circuit | Diode Reverse Recovery Waveform |
|  <p>A circuit diagram for diode reverse recovery testing. It uses a 'Current Pump' circuit to drive the D.U.T. (diode) with a double pulse. The diode is connected to a load inductor L and a current measurement point I_D. The circuit is powered by V_{DD}. A di/dt adjuster is used to control the switching rate.</p> |  <p>Waveform diagram showing the diode current I_D versus time. It illustrates the reverse recovery process, with parameters $di/dt = 100A/\mu s$, Q_{rr}, and t_{rr}.</p> |



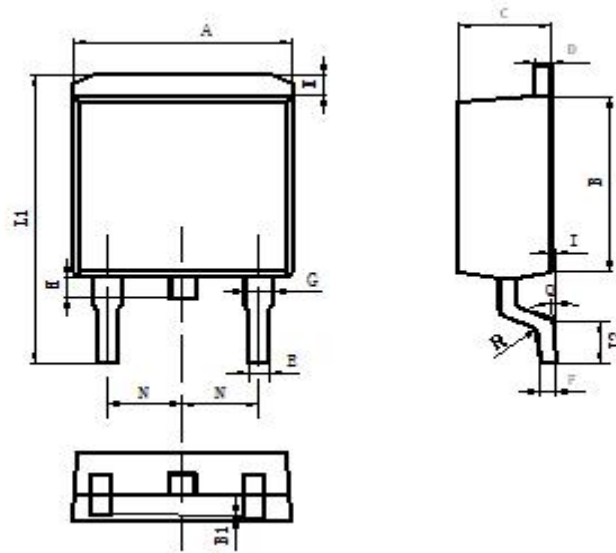
Package Description



| Symbol | Values(mm) | |
|----------|------------|-----|
| | MIN | MAX |
| A | 9.60 | 10. |
| B | 15.0 | 16. |
| B1 | 8.90 | 9.5 |
| C | 4.30 | 4.8 |
| C1 | 2.30 | 3.1 |
| D | 1.20 | 1.4 |
| E | 0.70 | 0.9 |
| F | 0.30 | 0.6 |
| G | 1.17 | 1.3 |
| H | 2.70 | 3.8 |
| L | 12.6 | 14. |
| N | 2.34 | 2.7 |
| Q | 2.40 | 3.0 |
| ϕP | 3.50 | 3.9 |

TO-220 Package

Package Information



| Symbol | Values (mm) | |
|--------|-------------|-------|
| | MIN | MAX |
| A | 9.80 | 10.40 |
| B | 8.90 | 9.50 |
| B1 | 0 | 0.10 |
| C | 4.40 | 4.80 |
| D | 1.16 | 1.37 |
| E | 0.70 | 0.95 |
| F | 0.30 | 0.60 |
| G | 1.07 | 1.47 |
| H | 1.30 | 1.80 |
| K | 0.95 | 1.37 |
| L1 | 14.50 | 16.50 |
| L2 | 1.60 | 2.30 |
| I | 0 | 0.2 |
| Q | 0° | 8° |
| R | 0.4 | 0.4 |
| N | 2.39 | 2.69 |

TO-263 package

NOTE:

1. Exceeding the maximum ratings of the device in performance may cause damage to the device, even the permanent failure, which may affect the dependability of the machine. Please do not exceed the absolute maximum ratings of the device when circuit designing.
2. When installing the heat sink, please pay attention to the torsional moment and the smoothness of the heat sink.
3. MOSFETs is the device which is sensitive to the static electricity, it is necessary to protect the device from being damaged by the static electricity when using it.
4. Shenzhen Minos reserves the right to make changes in this specification sheet and is subject to change without prior notice.

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