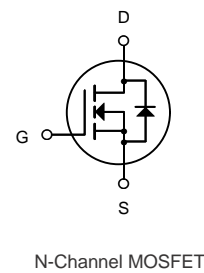
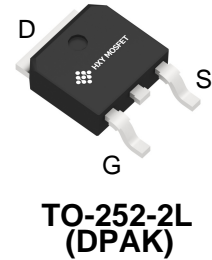




## Description

The FDD8453LZ-F085 uses advanced trench technology to provide excellent  $R_{DS(ON)}$ , low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.



## General Features

$V_{DS} = 40V$   $I_D = 80A$

$R_{DS(ON)} < 5.4m\Omega @ V_{GS}=10V$

## Application

Battery protection

Load switch

Uninterruptible power supply

## Ordering Information

Product ID	Pack	Brand	Qty(PCS)
FDD8453LZ-F085	TO-252-2L(DPAK)	HXY MOSFET	2500

## Absolute Maximum Ratings ( $T_C=25^\circ C$ unless otherwise noted)

Symbol	Parameter	Rating	Units
$V_{DS}$	Drain-Source Voltage	40	V
$V_{GS}$	Gate-Source Voltage	$\pm 20$	V
$I_D@T_C=25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	60	A
$I_D@T_C=100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	38	A
$I_{DM}$	Pulsed Drain Current	240	A
EAS	Single Pulse Avalanche Energy	100	mJ
$I_{AS}$	Avalanche Current	28	A
$P_D@T_C=25^\circ C$	Total Power Dissipation	114	W
$T_{STG}$	Storage Temperature Range	-55 to 150	$^\circ C$
$T_J$	Operating Junction Temperature Range	-55 to 150	$^\circ C$
$R_{\theta JA}$	Thermal Resistance Junction-Ambient	37	$^\circ C/W$



**Electrical Characteristics (T<sub>c</sub>=25°C unless otherwise noted)**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-Source Breakdown Voltage	I <sub>D</sub> = 250μA, V <sub>GS</sub> = 0V	40			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 40V, V <sub>GS</sub> = 0V			1.0	μA
I <sub>GSS</sub>	Gate-Body Leakage Current	V <sub>DS</sub> = 0V, V <sub>GS</sub> = ±20V			±100	nA
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA	1.3	1.9	2.5	V
R <sub>DS(on)</sub>	Static Drain-Source ON-Resistance <sup>(4)</sup>	V <sub>GS</sub> = 10V, I <sub>D</sub> = 30A		5.4	7.0	mΩ
		V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 20A		8.1	10.5	mΩ
C <sub>iss</sub>	Input Capacitance	V <sub>GS</sub> = 0V, V <sub>DS</sub> = 20V, f = 1MHz		2443		pF
C <sub>oss</sub>	Output Capacitance			167		pF
C <sub>rss</sub>	Reverse Transfer Capacitance			138		pF
Q <sub>g</sub>	Total Gate Charge	V <sub>GS</sub> = 0 to 10V V <sub>DS</sub> = 20V, I <sub>D</sub> = 20A		48		nC
Q <sub>gs</sub>	Gate Source Charge			10		nC
Q <sub>gd</sub>	Gate Drain("Miller") Charge			10		nC
t <sub>d(on)</sub>	Turn-On DelayTime	V <sub>GS</sub> = 10V, V <sub>DD</sub> = 20V I <sub>D</sub> = 20A, R <sub>GEN</sub> = 3Ω		10		ns
t <sub>r</sub>	Turn-On Rise Time			28		ns
t <sub>d(off)</sub>	Turn-Off DelayTime			40		ns
t <sub>f</sub>	Turn-Off Fall Time			7		ns
I <sub>S</sub>	Maximum Continuous Drain to Source Diode Forward Current				60	A
I <sub>SM</sub>	Maximum Pulsed Drain to Source Diode Forward Current				240	A
V <sub>SD</sub>	Drain to Source Diode Forward Voltage	V <sub>GS</sub> = 0V, I <sub>S</sub> = 30A			1.2	V
trr	Body Diode Reverse Recovery Time	I <sub>F</sub> = 20A, di/dt = 100A/us		11		ns
Qrr	Body Diode Reverse Recovery Charge			5		nC

- Notes: 1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature.  
2. E<sub>AS</sub> condition: Starting T<sub>J</sub>=25C, V<sub>DD</sub>=20V, V<sub>G</sub>=10V, R<sub>G</sub>=25ohm, L=0.5mH, I<sub>AS</sub>=20A  
3. R<sub>θJA</sub> is measured with the device mounted on a 1inch<sup>2</sup> pad of 2oz copper FR4 PCB  
4. Pulse Test: Pulse Width≤300μs, Duty Cycle≤0.5%.



### Typical Electrical and Thermal Characteristics (Curves)

Figure 1: Output Characteristics

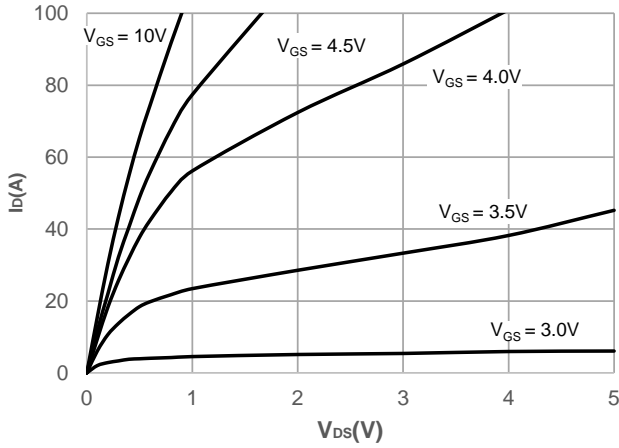


Figure 3: On-resistance vs. Drain Current

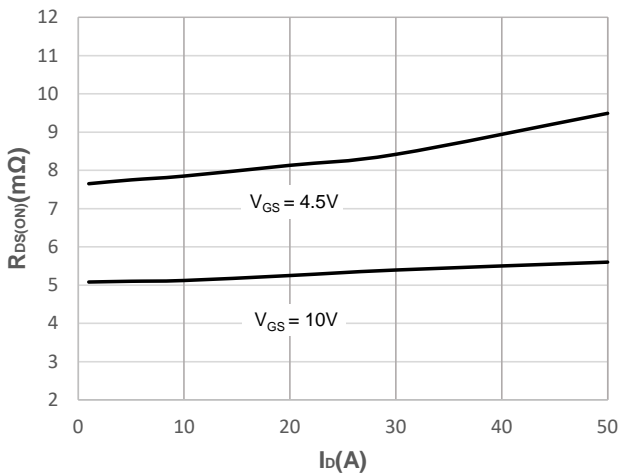


Figure 5: Gate Charge Characteristics

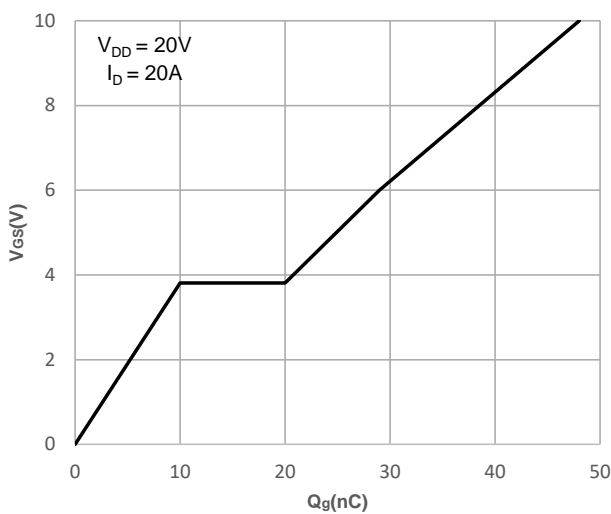


Figure 7: Normalized Breakdown voltage vs. Junction Temperature

Figure 2: Typical Transfer Characteristics

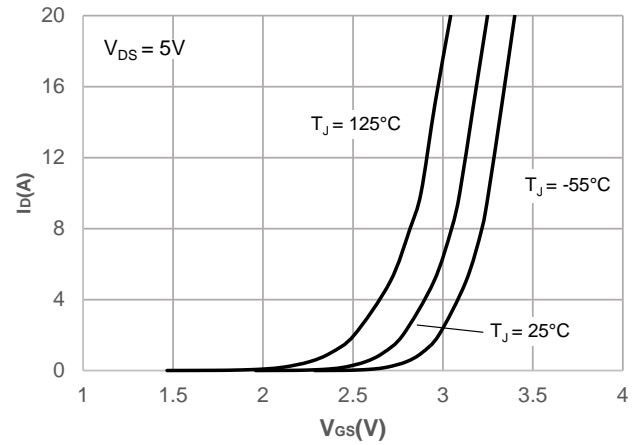


Figure 4: Body Diode Characteristics

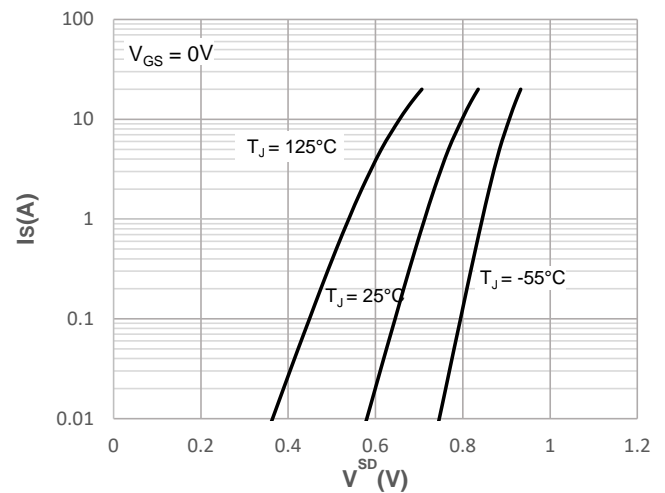


Figure 6: Capacitance Characteristics

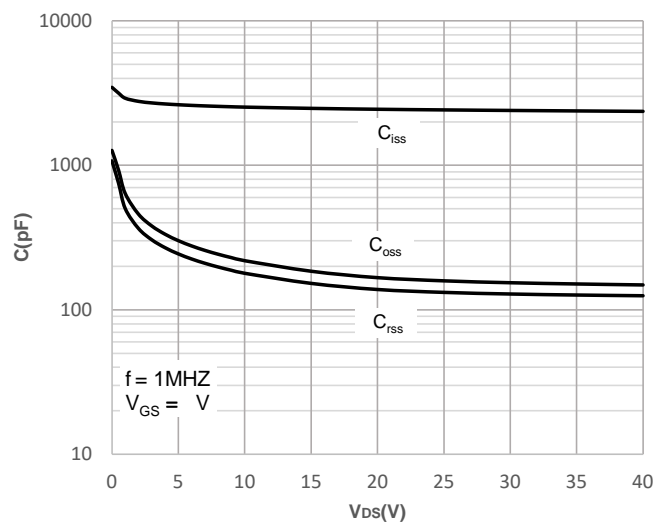


Figure 8: Normalized on Resistance vs. Junction Temperature

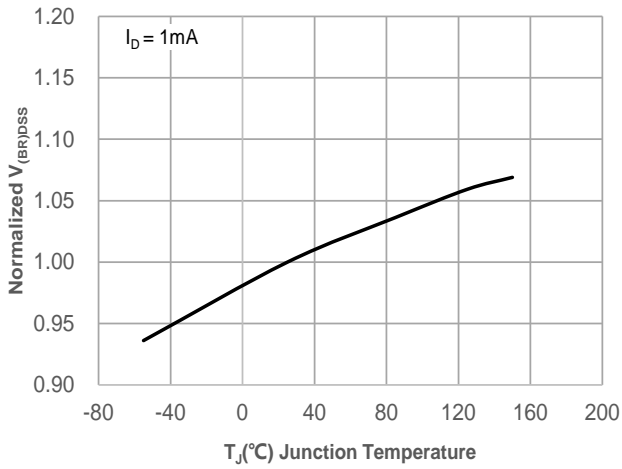


Figure 9: Maximum Safe Operating Area

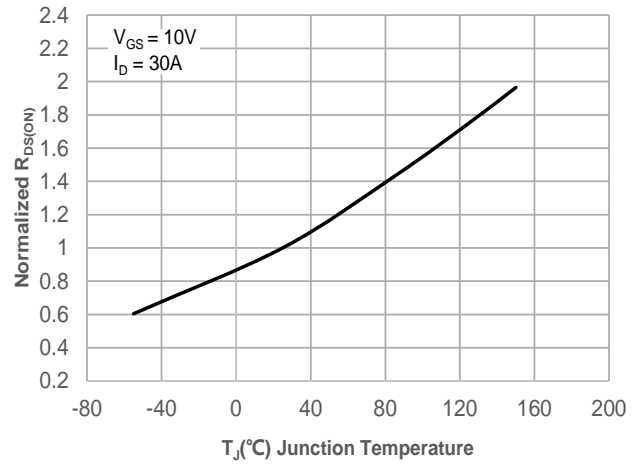


Figure 10: Maximum Continuous Drianc Current vs. Case Temperature

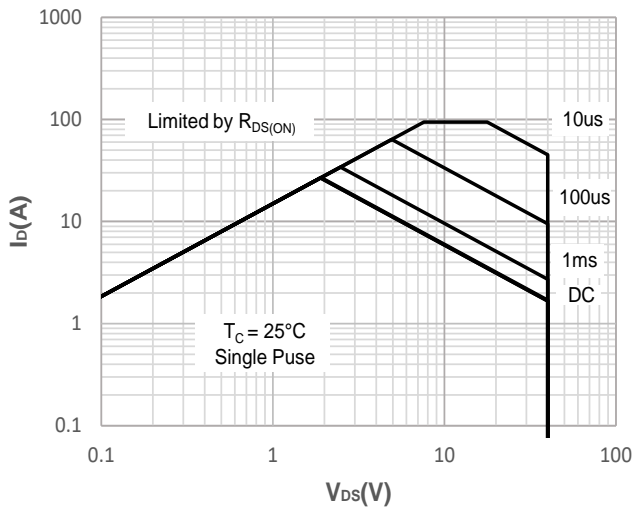


Figure 11: Normalized Maximum Transient Thermal Impedance

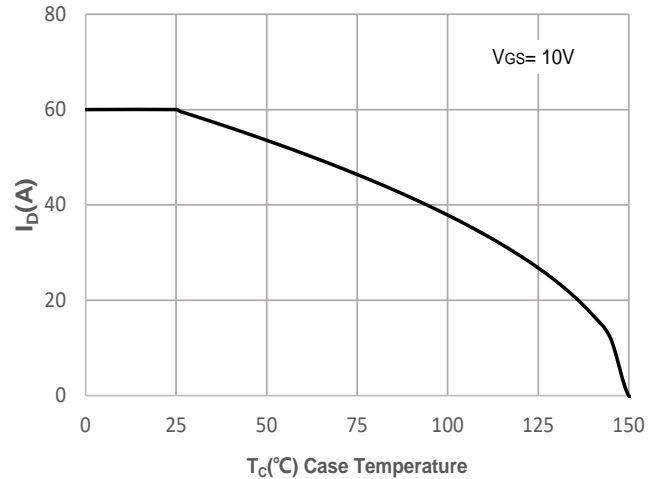
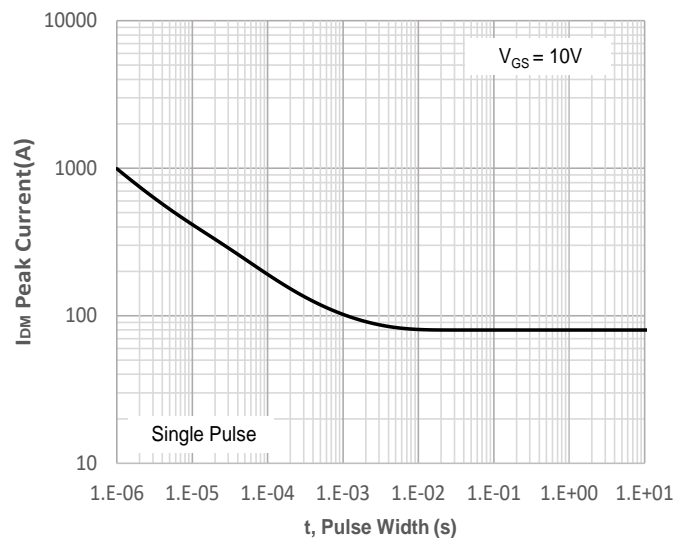
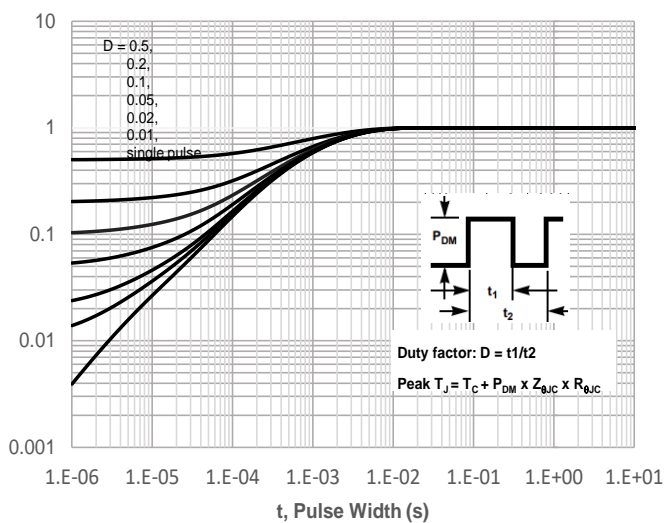


Figure 12: Peak Current Capacity





### Test Circuit

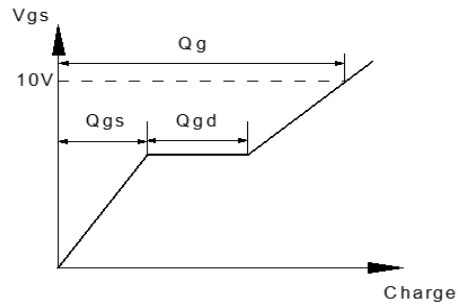
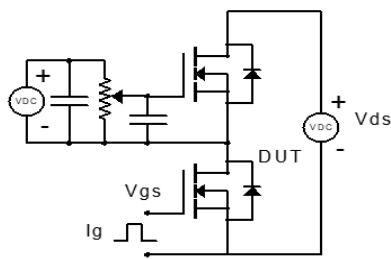


Figure 1: Gate Charge Test Circuit & Waveform

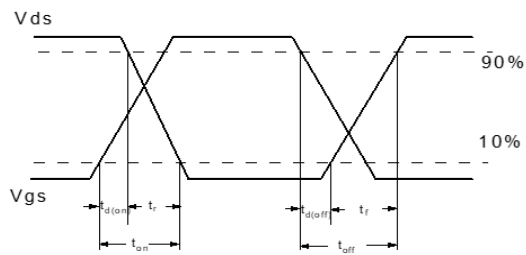
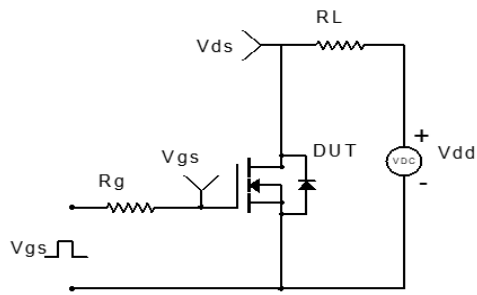


Figure 2: Resistive Switching Test Circuit & Waveform

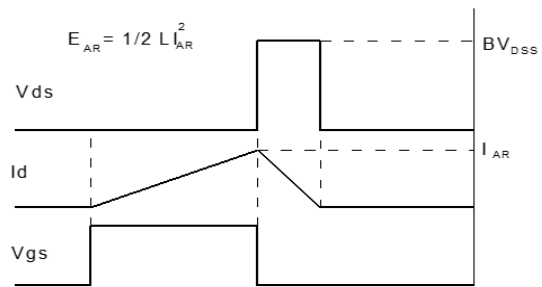
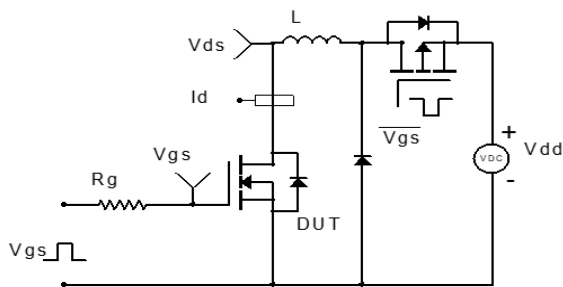


Figure 3: Unclamped Inductive Switching Test Circuit & Waveform

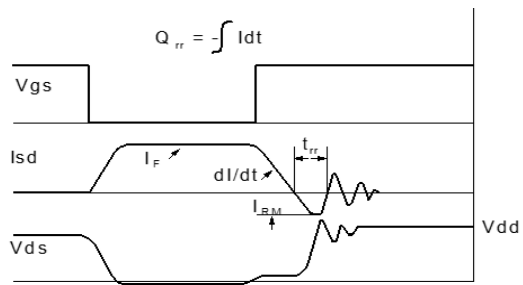
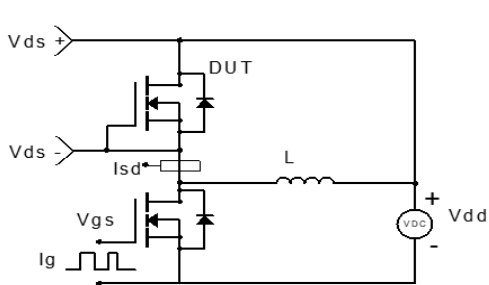
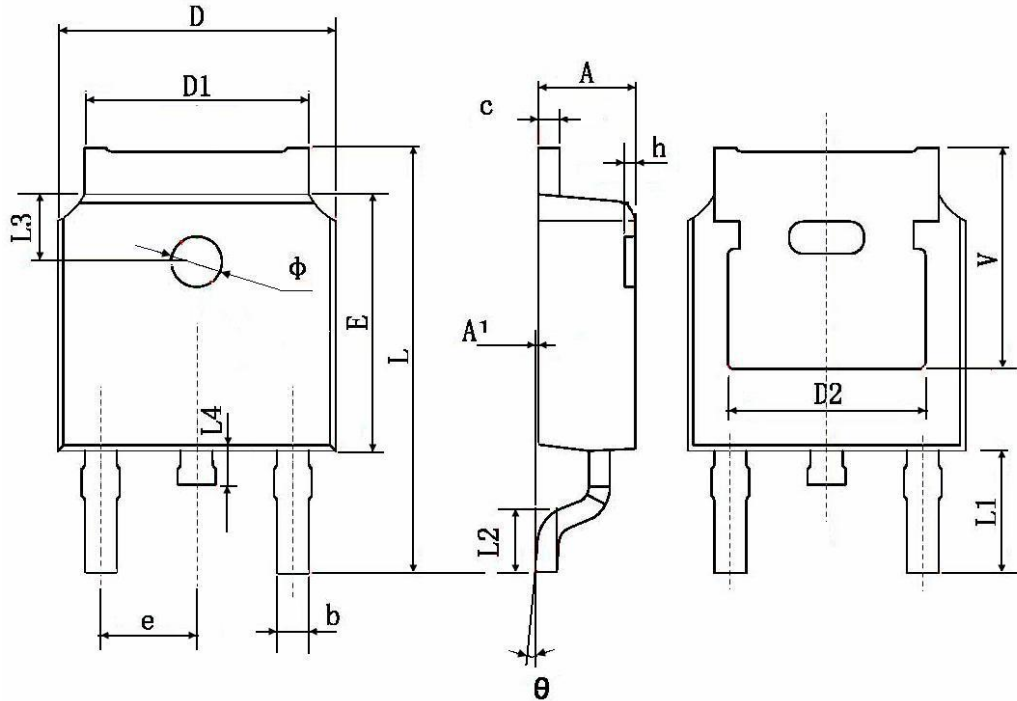


Figure 4: Diode Recovery Test Circuit & Waveform



### TO-252-2L(DPAK) Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	2.200	2.400	0.087	0.094
A1	0.000	0.127	0.000	0.005
b	0.660	0.860	0.026	0.034
c	0.460	0.580	0.018	0.023
D	6.500	6.700	0.256	0.264
D1	5.100	5.460	0.201	0.215
D2	0.483 TYP.		0.190 TYP.	
E	6.000	6.200	0.236	0.244
e	2.186	2.386	0.086	0.094
L	9.800	10.400	0.386	0.409
L1	2.900 TYP.		0.114 TYP.	
L2	1.400	1.700	0.055	0.067
L3	1.600 TYP.		0.063 TYP.	
L4	0.600	1.000	0.024	0.039
Φ	1.100	1.300	0.043	0.051
θ	0°	8°	0°	8°
h	0.000	0.300	0.000	0.012
V	5.350 TYP.		0.211 TYP.	



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