



Description

The IRF7104PBF uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

General Features

$V_{DS} = -20V, I_D = -4A$

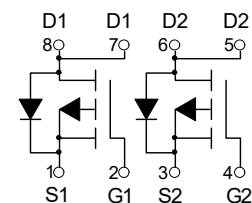
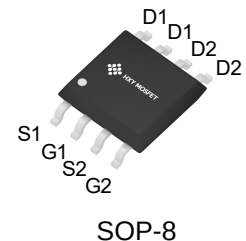
$R_{DS(ON)} < 95m\Omega @ V_{GS} = -4.5V$

$R_{DS(ON)} < 110m\Omega @ V_{GS} = -2.5V$

Application

PWM application

Load switch



Dual P-Channel MOSFET

Ordering Information

Product ID	Pack	Brand	Qty(PCS)
IRF7104PBF	SOP-8	HXY MOSFET	3000

Absolute Maximum Ratings ($T_A = 25^\circ C$ unless otherwise noted)

Symbol	Parameter	Limit	Unit
V_{DS}	Drain-Source Voltage	-20	V
V_{GS}	Gate-Source Voltage	± 12	V
I_D	Drain Current-Continuous	-4	A
I_{DM}	Drain Current-Pulsed (Note 1)	-20	A
P_D	Maximum Power Dissipation	2.0	W
T_J, T_{STG}	Operating Junction and Storage Temperature Range	-55 To 150	$^\circ C$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 2)	62.5	$^\circ C/W$



Electrical Characteristics ($T_J=25^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=-250\mu A$	-20	---	---	V
$\Delta BV_{DSS}/\Delta T_J$	BVDSS Temperature Coefficient	Reference to 25°C , $I_D=-1mA$	---	-0.02	---	V/ $^\circ\text{C}$
$R_{DS(ON)}$	Static Drain-Source On-Resistance ²	$V_{GS}=-4.5V, I_D=-5.8A$	---	85	95	$m\Omega$
		$V_{GS}=-2.5V, I_D=-3.5A$	---	95	110	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}, I_D=-250\mu A$	-0.6	-1.1	-1.7	V
$\Delta V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	4.32	---	mV/ $^\circ\text{C}$
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=-16V, V_{GS}=0V, T_J=25^\circ\text{C}$	---	---	-1	μA
		$V_{DS}=-16V, V_{GS}=0V, T_J=55^\circ\text{C}$	---	---	-5	
I_{GSS}	Gate-Source Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0V$	---	---	± 100	nA
g_{fs}	Forward Transconductance	$V_{DS}=-5V, I_D=-3A$	---	5.5	---	S
R_g	Gate Resistance	$V_{DS}=0V, V_{GS}=0V, f=1MHz$	---	24	48	Ω
Q_g	Total Gate Charge (-4.5V)	$V_{DS}=-16V, V_{GS}=-4.5V, I_D=-5.8A$	---	10.6	15	nC
Q_{gs}	Gate-Source Charge		---	1.0	---	
Q_{gd}	Gate-Drain Charge		---	2.0	---	
$T_{d(on)}$	Turn-On Delay Time	$V_{DD}=-15V, V_{GS}=-10V, R_G=6\Omega$ $I_D=-1A, R_G=10\Omega$	---	10	12	ns
T_r	Rise Time		---	4.9	6	
$T_{d(off)}$	Turn-Off Delay Time		---	22	42	
T_f	Fall Time		---	3	9	
C_{iss}	Input Capacitance	$V_{DS}=-15V, V_{GS}=0V, f=1MHz$	---	325	---	pF
C_{oss}	Output Capacitance		---	60	---	
C_{rss}	Reverse Transfer Capacitance		---	30	---	
I_S	Continuous Source Current ^{1,4}	$V_G=V_D=0V$, Force Current	---	---	-2.0	A
I_{SM}	Pulsed Source Current ^{2,4}		---	---	-20	A
V_{SD}	Diode Forward Voltage ²	$V_{GS}=0V, I_S=-1.7A, T_J=25^\circ\text{C}$	---	---	-1	V

Note :

1.The data tested by surface mounted on a 1 inch² FR-4 board with 20Z copper, $t<10\text{sec}$.

2.The data tested by pulsed , pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$

3.The power dissipation is limited by 150°C junction temperature

4.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.



Typical Characteristics

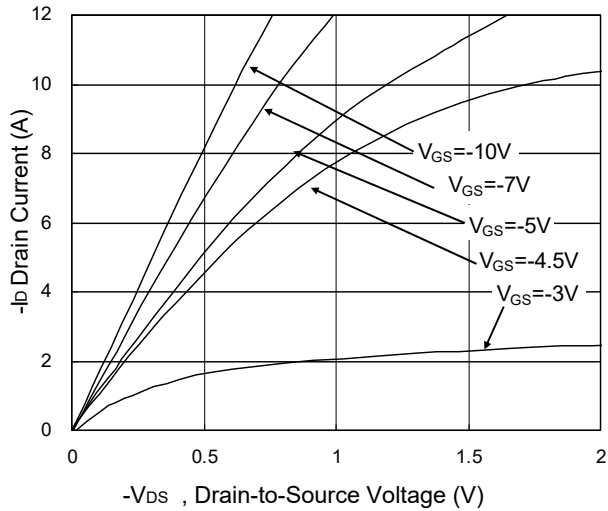


Fig.1 Typical Output Characteristics

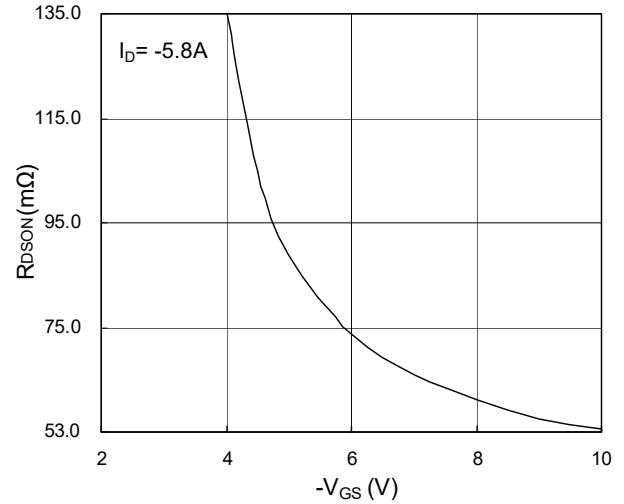


Fig.2 On-Resistance vs. G-S Voltage

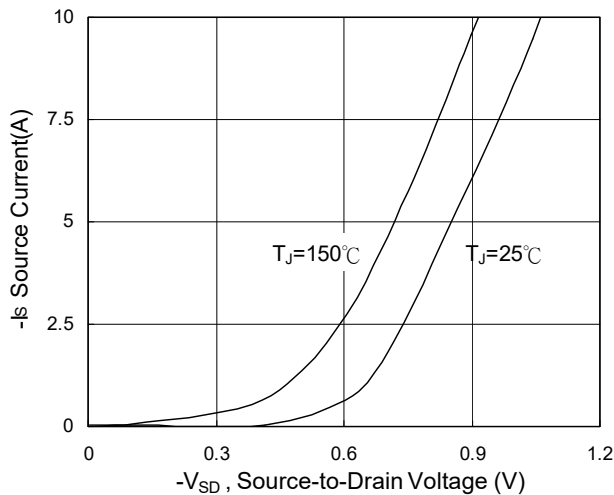


Fig.3 Forward Characteristics of Reverse

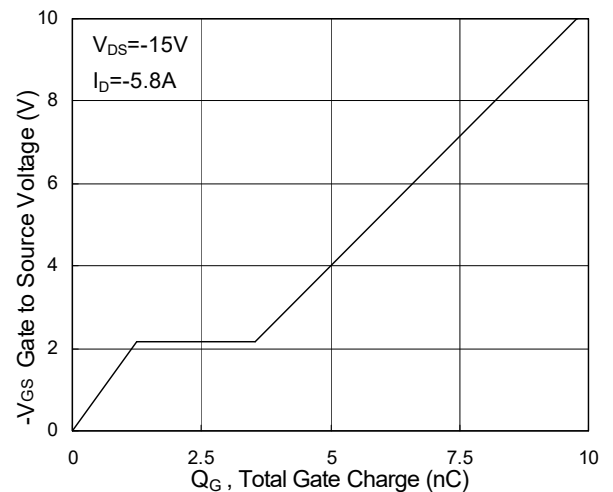


Fig.4 Gate-Charge Characteristics

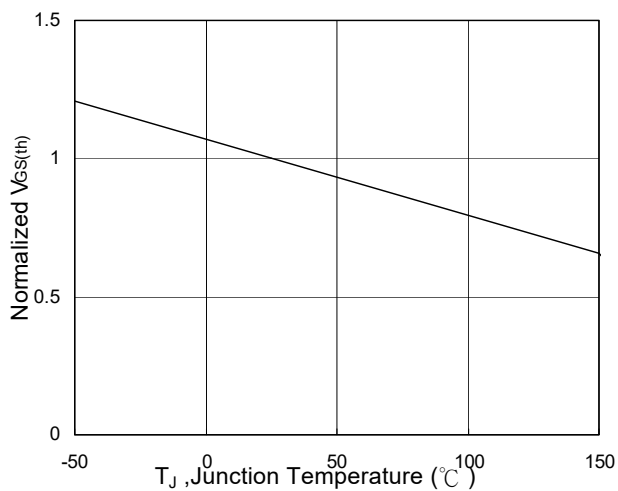


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

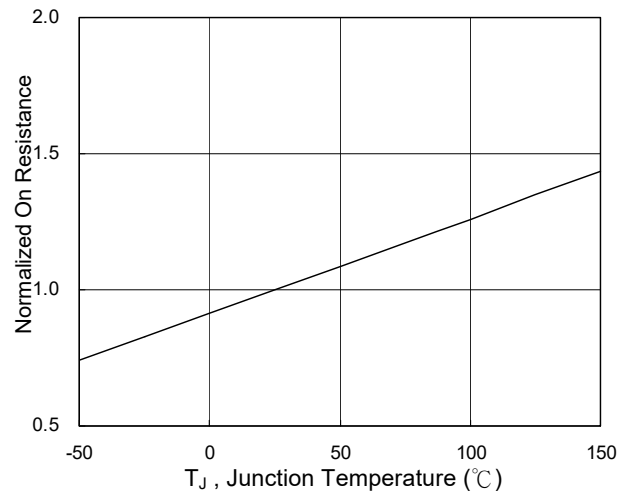


Fig.6 Normalized $R_{DS(on)}$ vs. T_J

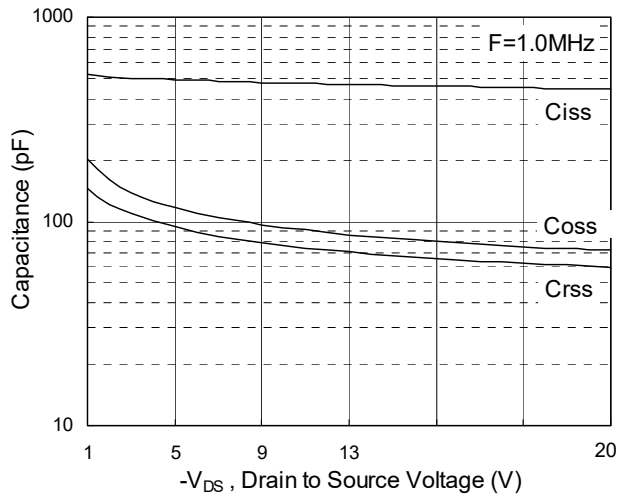


Fig.7 Capacitance

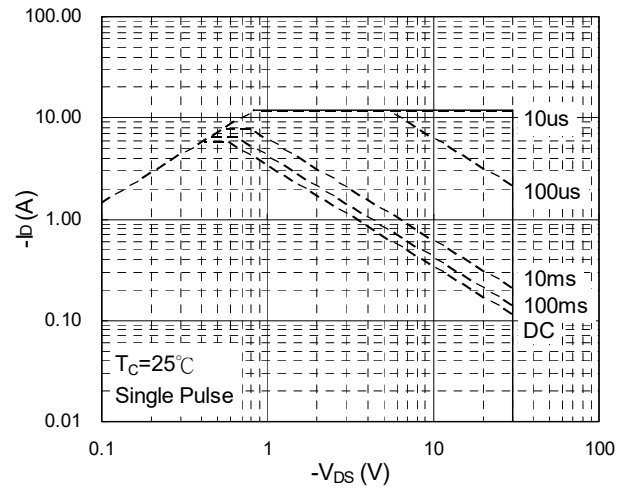


Fig.8 Safe Operating Area

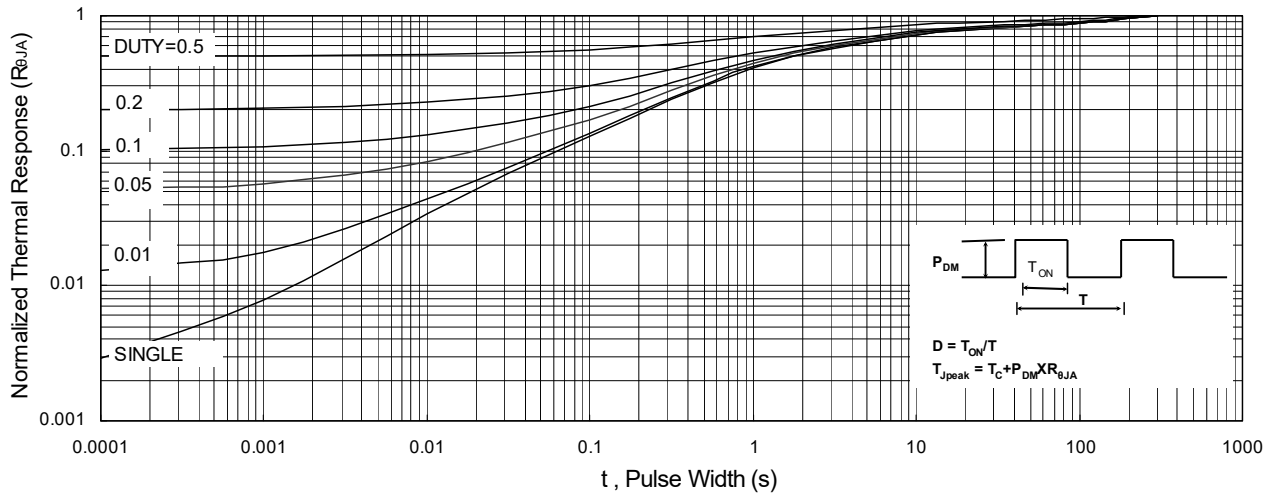


Fig.9 Normalized Maximum Transient Thermal Impedance

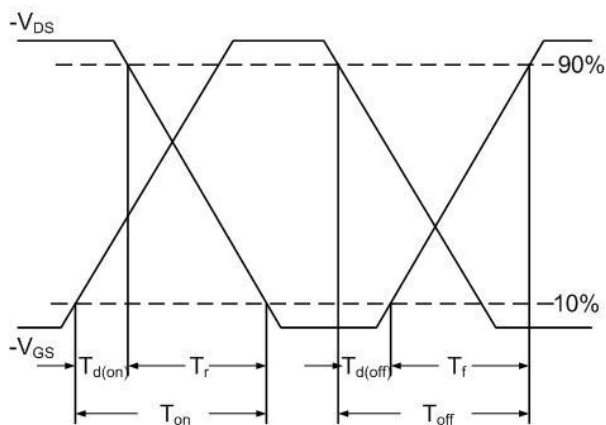


Fig.10 Switching Time Waveform

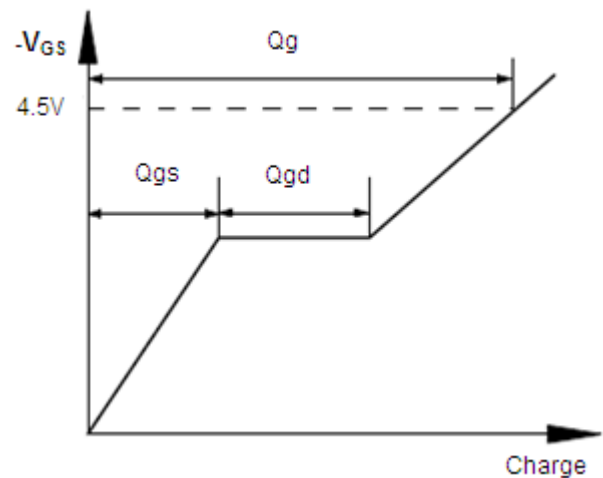
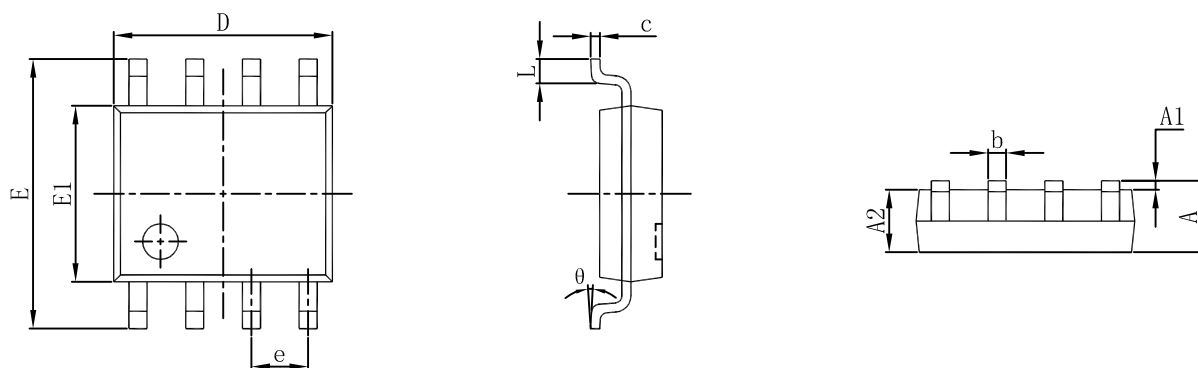


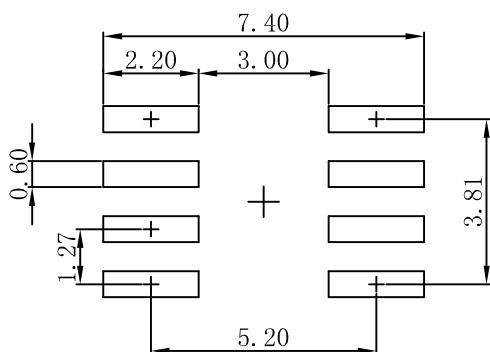
Fig.11 Gate Charge Waveform



SOP-8 Package Outline Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.800	5.000	0.189	0.197
e	1.270 (BSC)		0.050 (BSC)	
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°



Note:
1. Controlling dimension: in millimeters.
2. General tolerance: $\pm 0.05\text{mm}$.
3. The pad layout is for reference purposes only.



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