钍地半导体
Tudi Semiconductor

Product Specification

TUDI-AT24CM01

I²C-Compatible (2-wire) Serial EEPROM
1-Mbit (131,072 x 8)

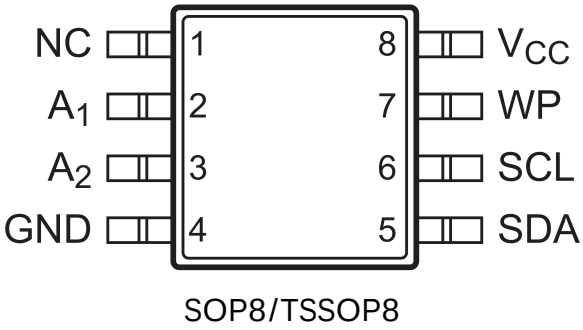
网址 www.sztdbdt.com

用芯智造·卓越品质

semiconductor device manufacturer

- Design
- research and development
- production
- and sales

Features



SOP8/TSSOP8

- Low Voltage and Standard Voltage Operation Available
-1.7V (V_{CC} = 1.7V to 5.5V)
-2.5V (V_{CC} = 2.5V to 5.5V)
- Internally Organized 131,072 x 8
- 2-wire Serial Interface
- Schmitt Triggers, Filtered Inputs for Noise Suppression
- Bidirectional Data Transfer Protocol
- 400kHz (1.7V) and 1MHz (5V, 2.5V) Compatibility
- Write Protect Pin for Hardware Data Protection
- 256-byte Page Write Mode
-Partial Page Writes Allowed
- Random and Sequential Read Modes
- Self-timed Write Cycle (5ms Max)
- High Reliability
-Endurance: 1,000,000 Write Cycles
-Data Retention: 40 Years
- Green Package Options (Pb/Halide-free/RoHS Compliant)
-8-lead SOIC, 8-lead TSSOP
- Die Sale Options: Wafer Form and Tape and Reel Available

Description

The AT24CM01 provides 1,048,576 bits of Serial Electrically Erasable and Programmable Read-Only Memory (EEPROM) organized as 131,072 words of 8 bits each. The device ’ scascadable feature allows up to four devices to share a common 2-wire bus. The device is optimized for use in many industrial and commercial applications where low power and low voltage operation are essential. The devices are available in space-saving 8-lead JEDEC SOIC, 8-lead TSSOP. In addition, the entire family is available in 1.7V (1.7V to 5.5V) and 2.5V (2.5V to 5.5V) versions.

Table1. Pin Configurations and Pinouts

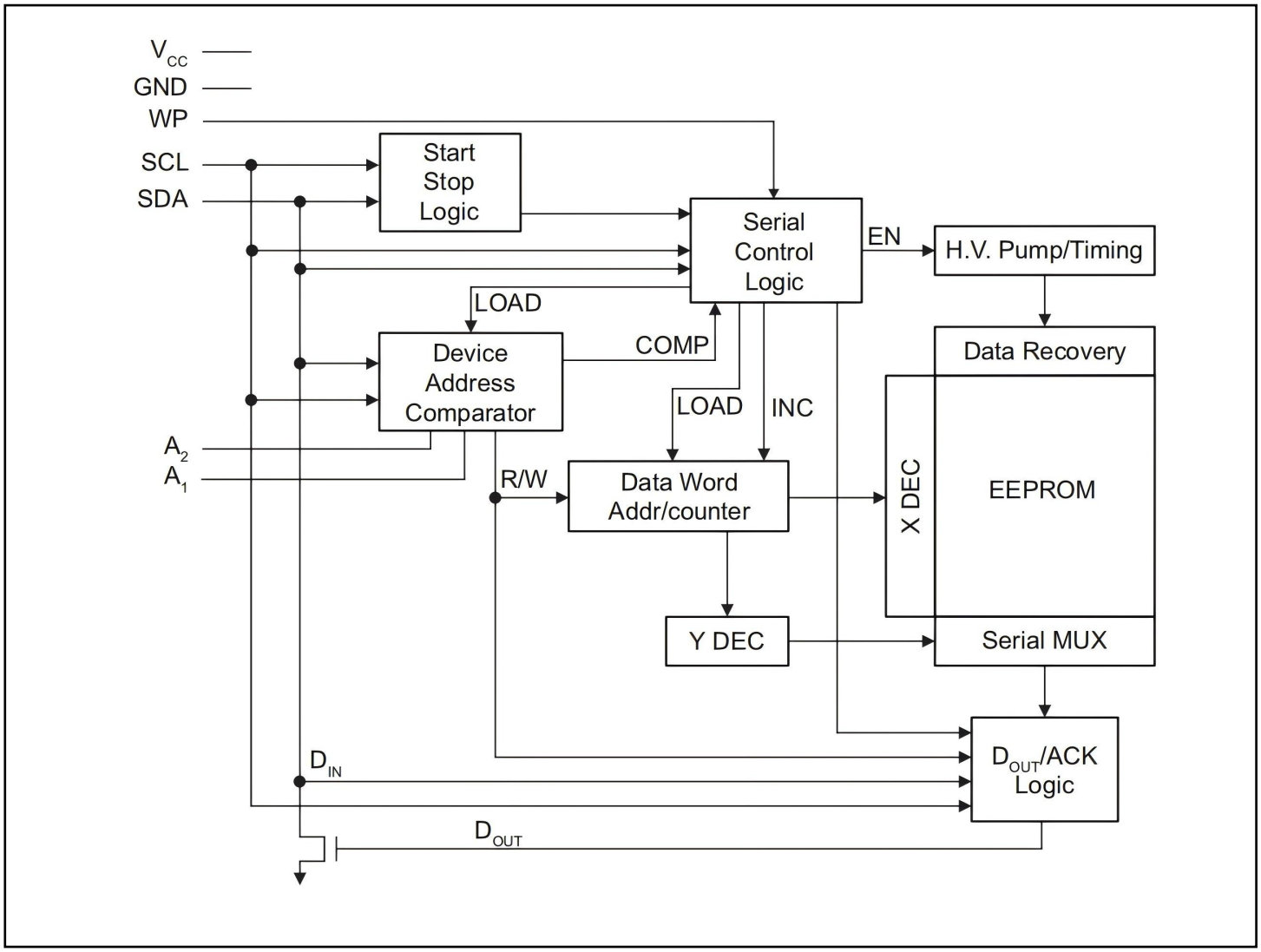
Pin Name	Function
NC	No Connect
A_1	Address Input
A_2	Address Input
GND	Ground
SDA	Serial Data
SCL	Serial Clock Input
WP	Write Protect
V_{CC}	Power Supply

Absolute Maximum Ratings

Operating Temperature . . . . . .-55ºC to +125ºC
Storage Temperature . . . . . .-65ºC to +150ºC
Voltage on any pin
with respect to ground . . . . . -1.0V to +7.0V
Maximum Operating Voltage 6.25V
DC Output Current 5.0mA

Notice: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in theoperational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Block Diagram



Pin Description

Serial Clock (SCL): The SCL input is used to positive edge clock data into each EEPROM device and negative edge clock data out of each device.

Serial Data (SDA): The SDA pin is bidirectional for serial data transfer. This pin is open drain driven and may be wire-ORed with any number of other open drain or open collector devices.

Device Addresses (A_2 and A_1): The A_2 and A_1 pins are device address inputs that can be hardwired or left not connected for hardware compatibility with other TUDI AT24Cxx devices. When the A_2 and A_1 pins are hardwired, as many as four 1-Mbit devices may be addressed on a single bussystem (See "Device Addressing" on page 9. for more details). |f the A_2 and A_1 pins are left floating, te A_2 and A_1 pin will be internally pulled down to GND if the capacitive coupling to the circuit board V_{CC} plane is <3pF. |f coupling is >3pF, TUDI recommends connecting the A_2 and A_1 pin to GND.

Write Protect (WP): The Write Protect input, when connected to GND, allows normal writeoperations . When WP is connected high to V_{cc}, all write operations to the memory are inhibited. |f the pin is lef t floating, the WP pin will be internally pulled down to GND if the capacitive coupling to the circuit board V_{cc} plane is <3pF. |f coupling is >3pF, TUDI recommends connecting the pin to GND. Switchi ng WP to V_{cc} prior to a write operation creates a software write protect function.

Table2. Write Protect

WP Pin Status	Part of the Array Protected
At V_{cc}	Full Array
At GND	Normal Read/rite Operations

Memory Organization

AT24CM01, 1-Mbit Serial EEPROM: The 1-Mbit is internally organized as 512 pages of 256 bytes each. Random word addressing requires a 17-bit data word address.

Table3.Pin Capacitance

Applicable over recommended operating range from T_A = 25ºC, f = 1.0MHz, V_{CC} = 5.5V.

Symbol	Test Condition	Max	Units	Conditions
$C_{I/O}$	Input/Output Capacitance(SDA)	8	pF	$V_{I/O}$=0V
C_{IN}	Input Capacitance(A_2,A_1,SCL)	6	pF	V_{IN}=0V

Note: 1. This parameter is characterized and is not 100% tested.

Table 4.DC Characteristics

Applicable over recommended operating range from: T_{AI} = -40ºC to +85ºC, V_{CC} = 1.7V to 5.5V (unless otherwise noted).

Symbol	Parameter	Test Condition		Min	Typ	Max	Units
V_{cc1}	Supply Voltage,1.7V Option			1.7		5.5	V
V_{cc2}	Supply Voltage,2.5V Option			2.5		5.5	V
I_{cc}	Supply Current	V_{cc}=5.0V	Read at 400kHz			2.0	mA
I_{cc}	Supply Current	V_{cc}=5.0V	Write at 400kHz			3.0	mA
I_{SB}	Standby Current	V_{cc}=1.7V	V_{IN}=V_{cc} or V_{ss}			1.0	μA
		V_{cc}=2.5V				2.0	μA
		V_{cc}=3.6V	V_{IN}=V_{cc} or V_{ss}			3.0	μA
		V_{cc}=5.5V				6.0	μA
I_{LI}	Input Leakage Current	V_{IN}=V_{cc}or V_{ss}			0.10	3.0	μA
I_{LO}	Output Leakage Current	V_{OUT}=V_{cc}or V_{ss}			0.05	3.0	μA
V_{IL}	Input Low Level(1)			-0.6		V_{cc}×0.3	V
V_{IH}	Input High Level(1)			V_{cc}×0.7		V_{cc}+0.5	V
V_{OL1}	Output Low Level	V_{cc}=1.7V	I_{OL}=0.15mA			0.2	V
V_{OL2}	Output Low Level	V_{cc}=3.0V	I_{OL}=2.1mA			0.4	V

Note: 1. V_{IL} min and V_{IH} max are reference only and are not tested.

Table 5.AC Characteristics

Applicable over recommended operating range from T_{AI} = -40ºC to +85ºC, V_{CC} = 1.7V to 5.5V (where applicable), CL = 100pF (unless otherwise noted). Test conditions are listed in Note 2.

Symbol	Parameter	1.7V		2.5V,5.0V		Units
		Min	Max	Min	Max	
f_{SCL}	Clock Frequency,SCL		400		1000	kHz
t_{LOW}	Clock Pulse Width Low	1300		400		ns
t_{HIGH}	Clock Pulse Width High	600		400		ns
t_I,	Noise Suppression Time(1)		100		50	ns
t_{AA}	Clock Low to Data Out Valid	50	900	50	550	ns
t_{BUF}	Time the bus must be free before anew transmission can start(1)	1300		500		ns
$t_{HD.STA}$	Start Condition Hold Time	600		250		ns
$t_{SU.STA}$	Start Condition Set-up Time	600		250		ns
$t_{HD.DAT}$	Data In Hold Time	0		0		ns
$t_{SU.DAT}$	Data In Set-up Time	100		100		ns
t_R	Inputs Rise Time(1)		300		300	ns
t_F	Inputs Fall Time(1)		300		100	ns
$t_{SU.STO}$	Stop Condition Set-up Time	600		250		ns
t_{DH}	Data Out Hold Time	50		50		ns
t_{WR}	Write Cycle Time		5		5	ms
Endurance(1)	25℃,Page Mode,3.3V	1,000,000				Write Cycles

Notes: 1. This parameter is ensured by characterization only.
2. AC measurement conditions:

- R_L (connects to V_{CC}): 1.3 k (2.5V, 5V), 10 k (1.7V)
- Input pulse voltages: 0.3 V_{CC} to 0.7 V_{CC}
- Input rise and fall times: ≤ 50ns
- Input and output timing reference voltages: 0.5 V_{CC}

Device Operation

Clock and Data Transitions: The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods. Data changes during SCL high periods will indicate a Start or Stop condition as defined below.

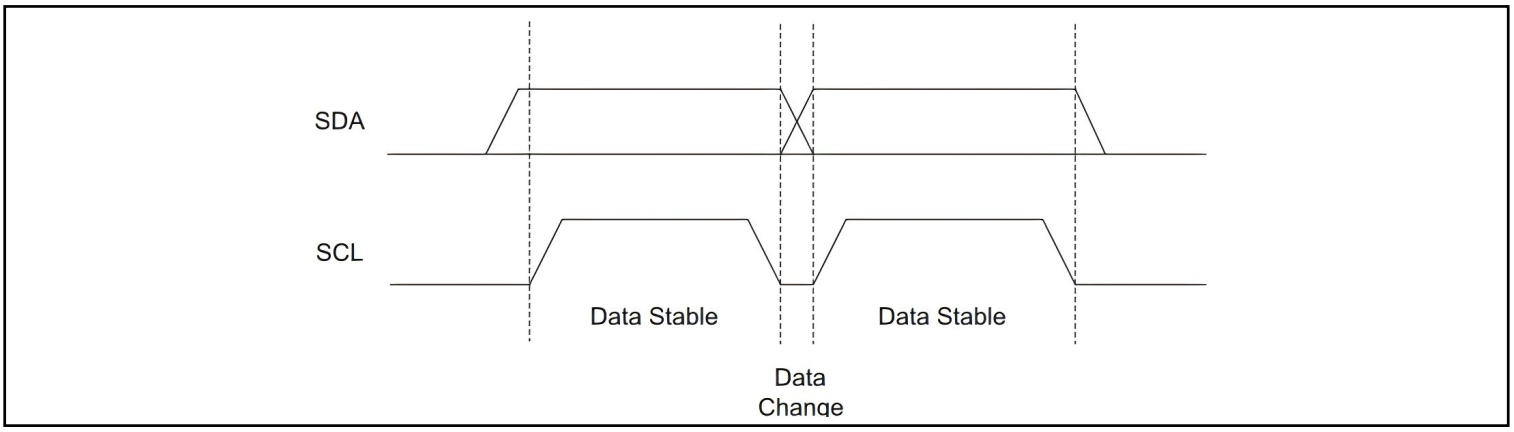


Figure 1. Data Validity

Start Condition: A high-to-low transition of SDA with SCL high is a Start condition which must precede any other command.
Stop Condition: A low-to-high transition of SDA with SCL high is a Stop condition. After a read sequence, the Stop condition will place the EEPROM in a standby power mode.

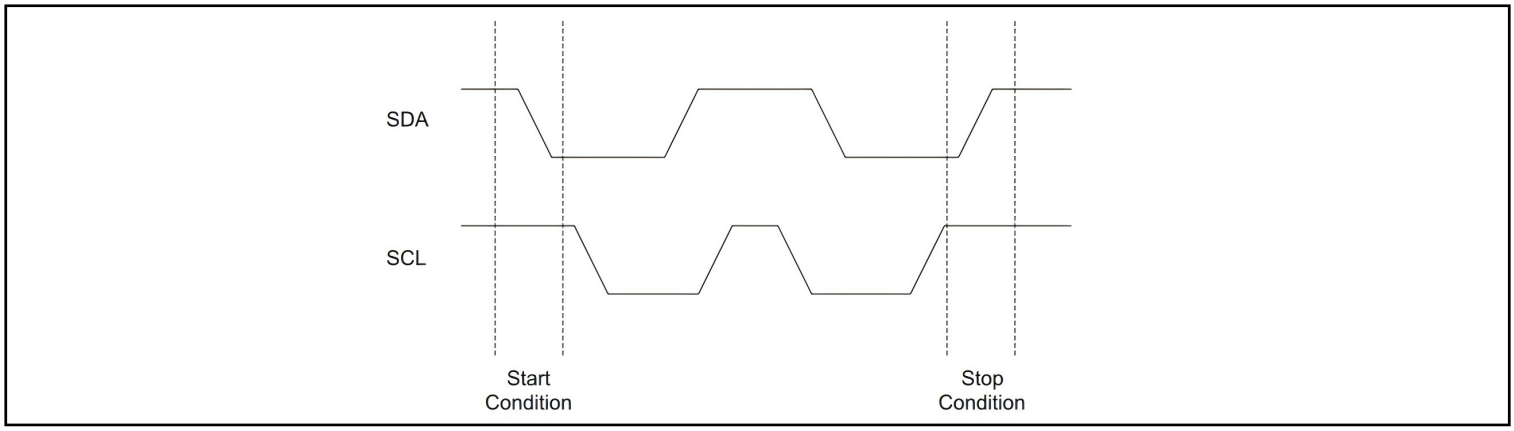


Figure 2. Start and Stop Definition

Acknowledge: All addresses and data words are serially transmitted to and from the EEPROM in eight bit words. The EEPROM sends a zero during the ninth clock cycle to acknowledge that it has received each word.

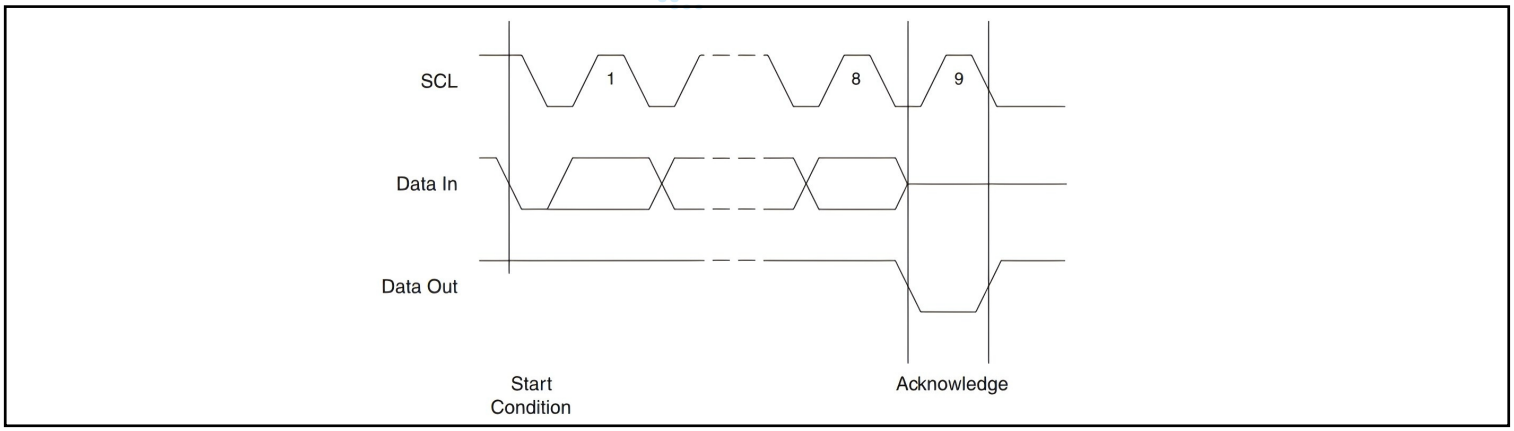


Figure 3. Output Acknowledge

Standby Mode:

The AT24CM01 features a low-power standby mode which is enabled:

● Upon power-up.

● After the receipt of the Stop condition and the completion of any internal operation.

Software Reset: After an interruption in protocol, power loss, or system reset, any 2-wire part can be protocol reset by following these steps:

1. Create a Start condition (if possible).
2. Clock nine cycles.
3. Create another Start condition followed by Stop condition as in Figure 4.

The device should be ready for the next communication after the above steps have been completed. In the event that the device is still non-responsive or remains active on the SDA bus, a power cycle must be used to reset the device.

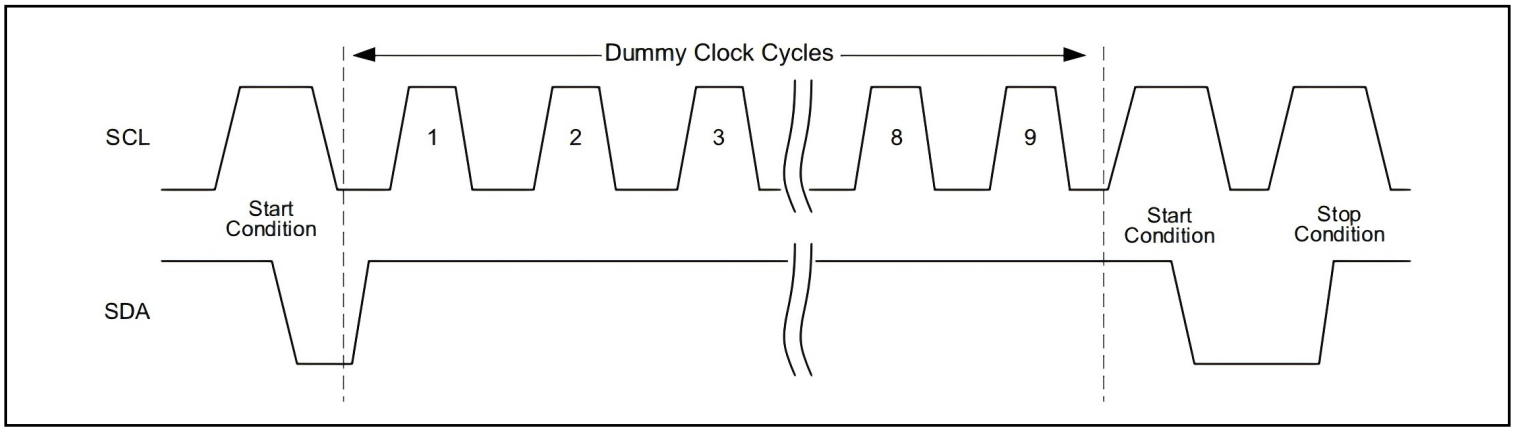
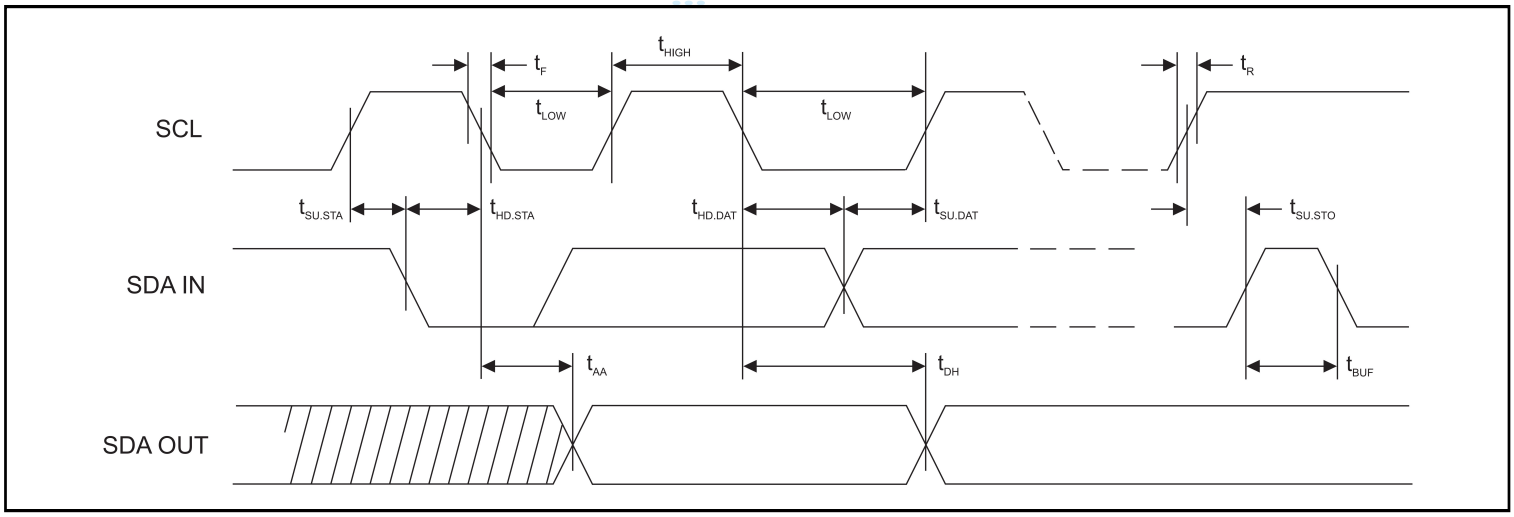
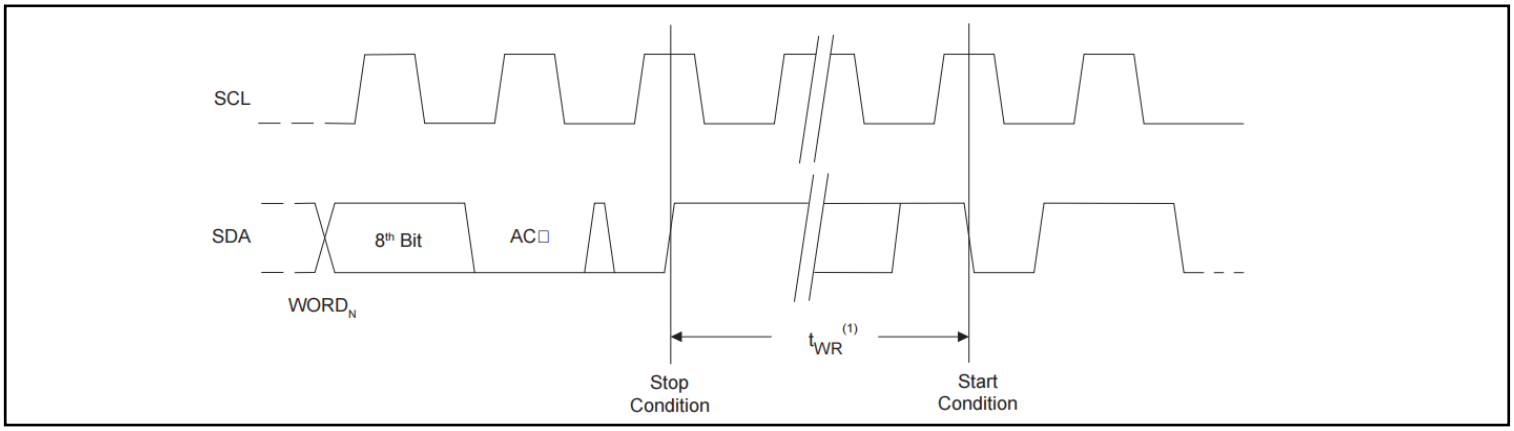


Figure 4. Software Reset



SCL: Serial Clock, SDA: Serial Data I/O

Figure 5. Bus Timing



SCL: Serial Clock, SDA: Serial Data I/O

Figure 6. Write Cycle Timing

Note: 1. The write cycle time t_{WR} is the time from a valid Stop condition of a write sequence to the end of the internal clear/write cycle.

Device Addressing

The 1-Mbit EEPROM requires an 8-bit device address word following a Start condition to enable the chip for a read or write operation (see Figure 7 below). The device address word consists of a mandatory ‘ 1010 ’ sequence for the first four most significant bits. This is common to all 2-wire EEPROM devices.

The 1-Mbit uses the two device address bits, A2 and A1, to allow up to four devices on the same bus. These A2 and A1 bits must compare to the corresponding hardwired input pins, A_2 and A_1. The A_2 and A_1 pins uses an internal proprietary circuit that biases it to a logic low condition if the pin is allowed to float.

The seventh bit (P_0) of the device address is a memory page address bit. This memory page address bit is the most significant bit of the data word address that follows. The eighth bit of the device address is the read/write operation select bit. A read operation is initiated if this bit is high and a write operation is initiated if this bit is low.

Upon a compare of the device address, the EEPROM will output a zero. If a valid compare is not made, the device will return to a standby state.

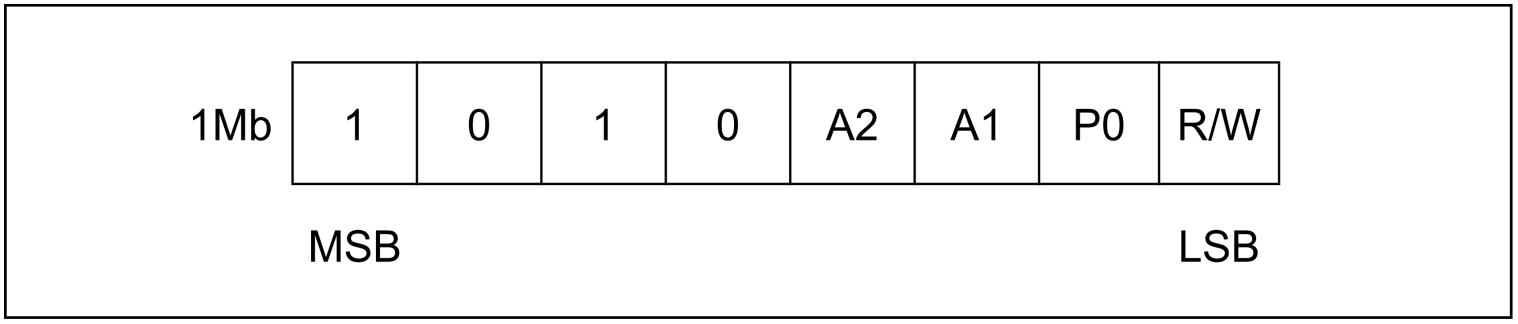


Figure 7 . Device Address

Write Operations

Byte Write: To select a data word in the 1-Mbit memory requires a 17-bit word address. The word address field consists of the P_0 bit in the device address byte, then the most significant word address followed by the least significant word address (Figure 8).

A write operation requires the P_0 bit and two 8-bit data word addresses following the device address word and acknowledgment. Upon receipt of this address, the EEPROM will againrespond with a zero and then the part is to receive the first 8-bit data word. Following receipt of the 8-bit data word, the EEPROM will output a zero. The addressing device, such as a microcontroller, then must terminate the write sequence with a Stop condition. At this time the EEPROM enters an internally timed write cycle, t_{WR}, to the nonvolatile memory. All inputs are disabled during this write cycle and the EEPROM will not respond until the write is complete (Figure 8).

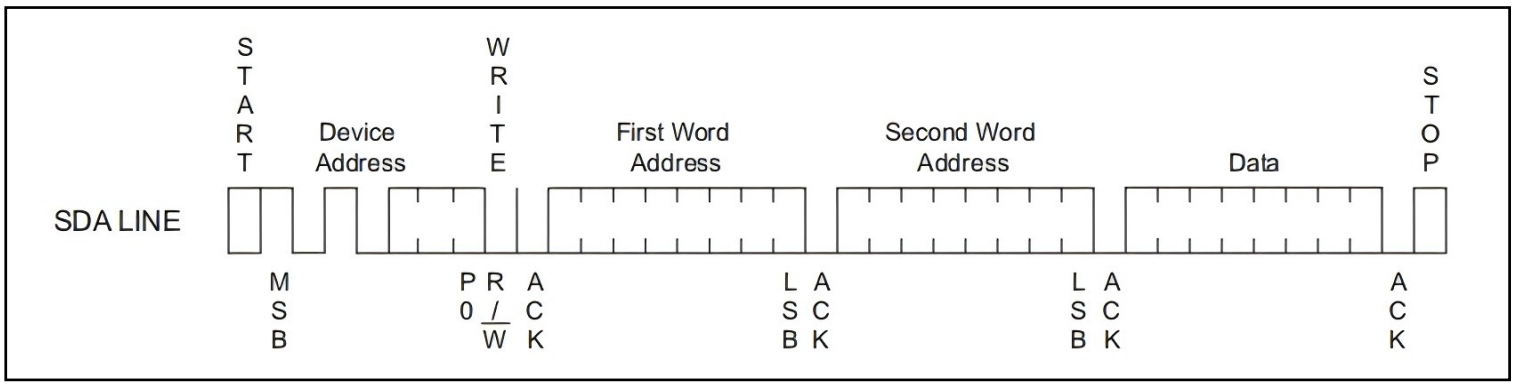


Figure 8. Byte Write

Page Write: The 1-Mbit EEPROM is capable of a 256-byte Page Write.

A Page Write is initiated the same way as a Byte Write, but the microcontroller does not send a Stop condition after the first data word is clocked in. Instead, after the EEPROM acknowledges receipt of the first data word, the microcontroller can transmit up to 255 more data words. The EEPROM will respond with an acknowledge after each data word is received. The microcontroller must terminate the page write sequence with a Stop condition (Figure 9) and the internally timed write cycle will begin.

The data word address lower 8 bits are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. When the internally generated word address, reaches the page boundary, the following byte is placed at the beginning of the same page. If more than 256 data words are transmitted to the EEPROM, the data word address will “ roll over ” and previous data will be overwritten. The address “ rollover ” during write is from the last byte of the current page to the first byte of the same page.

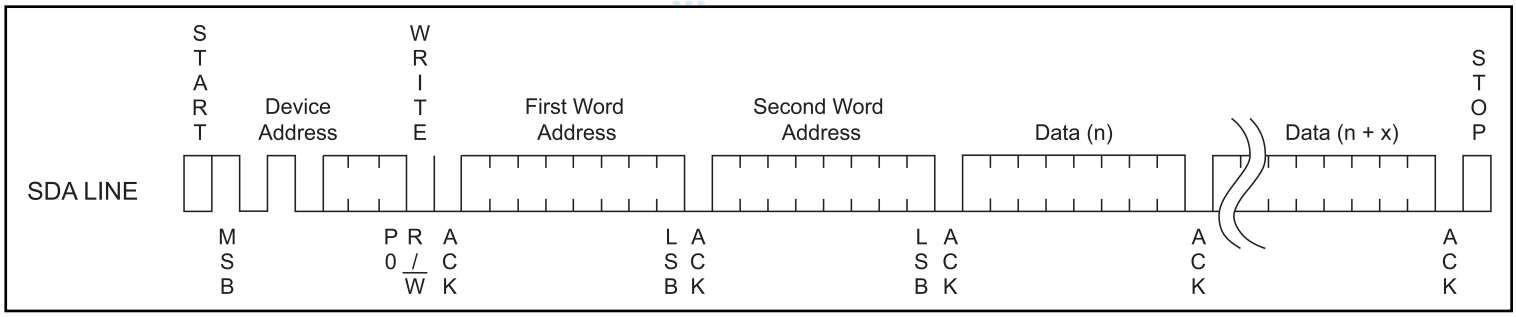


Figure 9. Page Write

Acknowledge Polling: Once the internally timed write cycle has started and the EEPROM inputs are disabled, Acknowledge Polling can be initiated. This involves sending a Start condition followed by the device address word. The read/write bit is representative of the operation desired. Only if the internal write cycle has completed will the EEPROM respond with a zero, allowing a new read or write sequence to be initiated.

Data Security: The AT24CM01 has a hardware data protection scheme that allows the user to write protect the entire memory when the WP pin is at V_{CC}.

Read Operations

Read operations are initiated the same way as write operations with the exception that the read/ write select bit in the device address word is set to one. There are three read operations: Current Address Read, Random Address Read, and Sequential Read.

Current Address Read: The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the V_{CC} to the part is maintained. The address "rollover" during read is from the last byte of the last page, to the first byte of the first page of the memory.
Once the device address with the read/write select bit set to one is input and acknowledged by the EEPROM, the current address data word is serially clocked out on the SDA line. The microcontroller does not respond with a zero but does generate a following Stop condition.

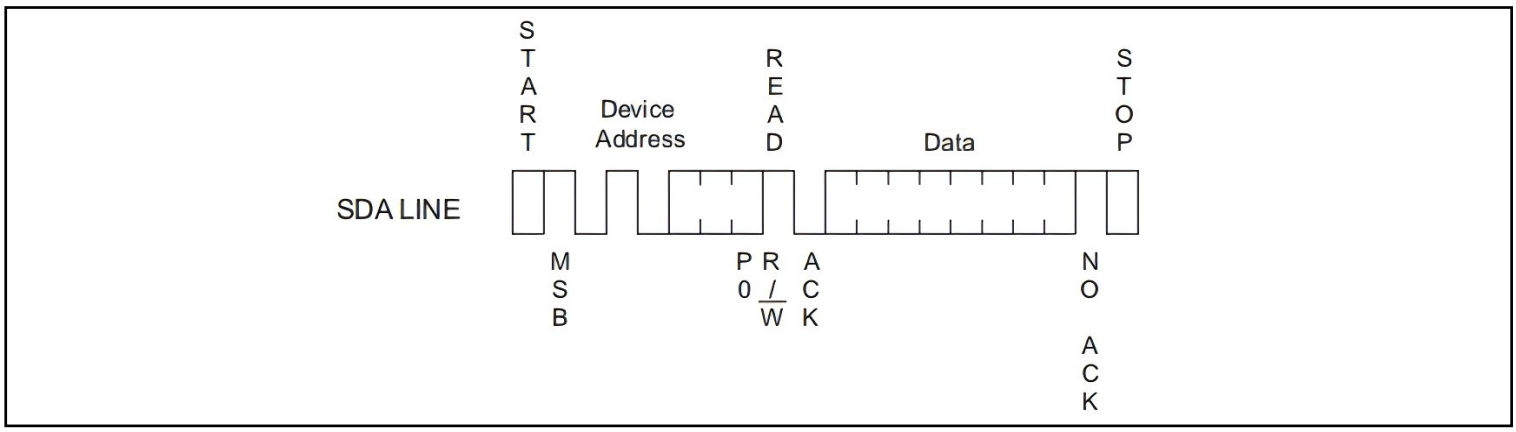


Figure 10. Current Address Read

Random Read: A Random Read requires an initial byte write sequence to load in the data word address. This is known as a “ dummy write ” operation. Once the device address word and data word address are clocked in and acknowledged by the EEPROM, the microcontroller mustgenerate another Start condition. The microcontroller now initiates a current address read by sending a device address with the read/write select bit high. The EEPROM acknowledges the device address and serially clocks out the data word on the SDA line. The microcontroller does not respond with a zero but does generate a following Stop condition.

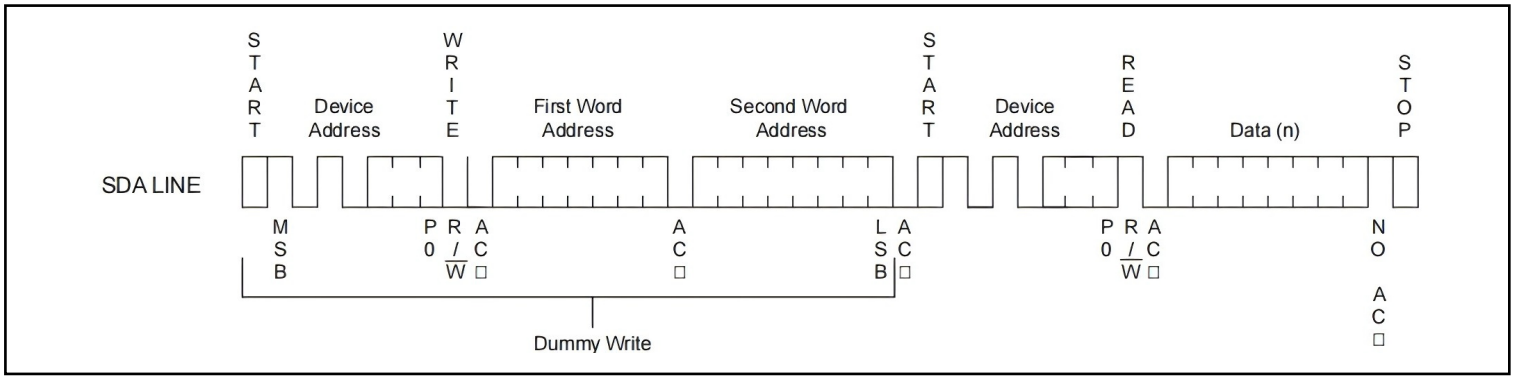


Figure11. Random Read

Sequential Read: Sequential Reads are initiated by either a Current Address Read or a Random Read. After the microcontroller receives a data word, it responds with an acknowledge. As long as the EEPROM receives an acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will “ roll over ” and the sequential read will continue. The Sequential Readoperation is ter minated when the microcontroller does not respond with a zero, but does generate a following Stop condition.

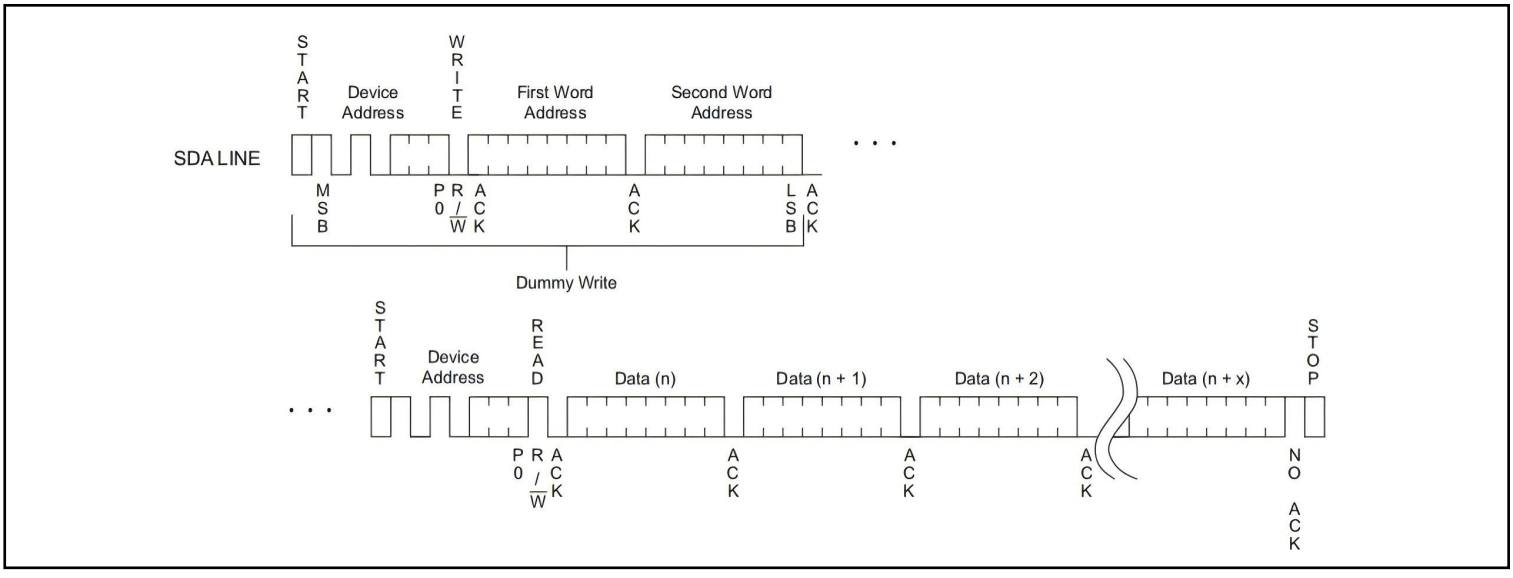


Figure12. Sequential Read

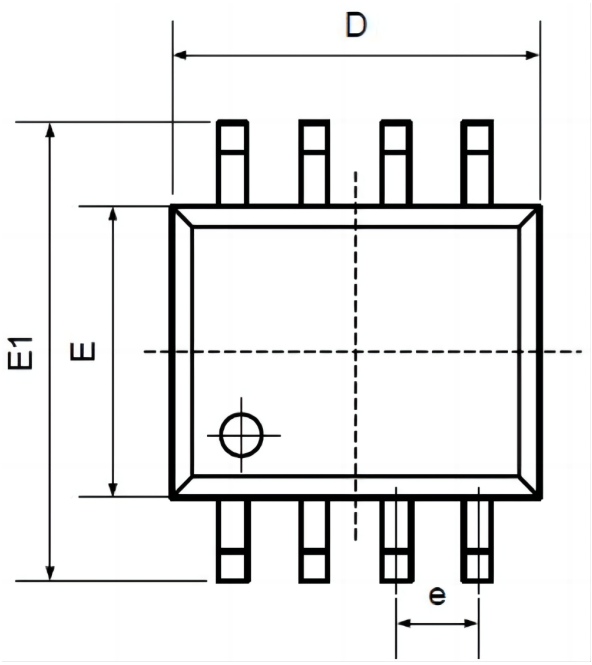
Order information

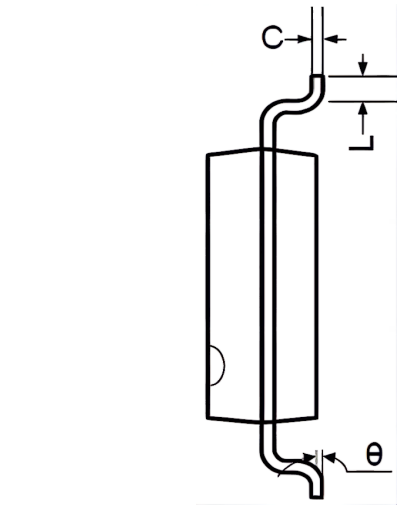
Order Number	Package	Package Quantity	Marking On The park	Temperature
AT24CM01-SSHM-T-TUDI	SOP8	Tape,Reel,4000	24CM01	-40°C to 85°C
			2GM	
AT24CM01-SSHD-T-TUDI	SOP8	Tape,Reel,4000	24CM01D	
			2GD	
AT24CM01-XHM-T-TUDI	TSSOP8	Tape,Reel,4000	2GM	

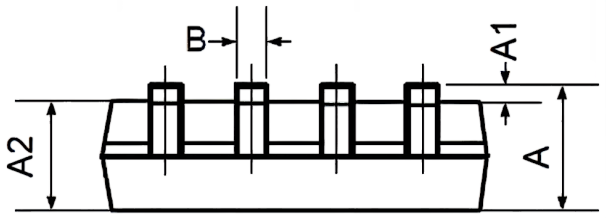
Revision history

	Date	Revision	Page
V1.0	2023/6	New	1-18
V1.1	2024/10	Update model and PDF template	1-18

Package SOP8

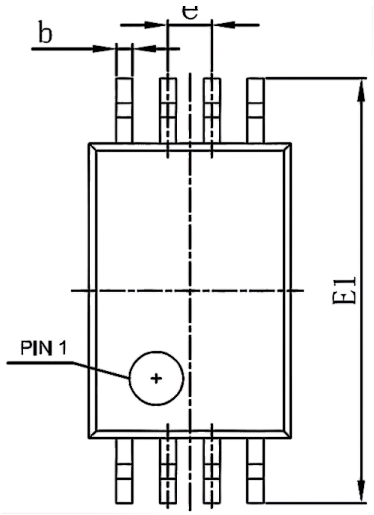


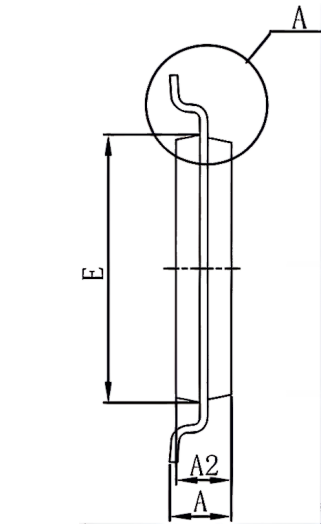


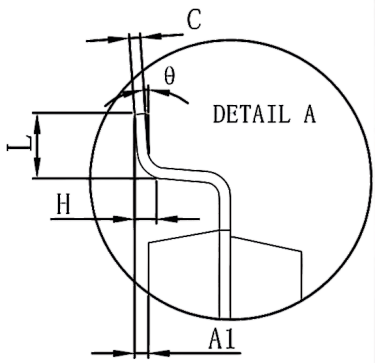


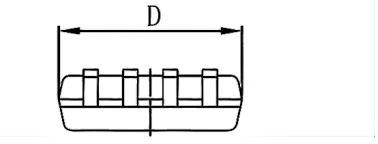
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
B	0.330	0.510	0.013	0.020
C	0.190	0.250	0.007	0.010
D	4.780	5.000	0.188	0.197
E	3.800	4.000	0.150	0.157
E1	5.800	6.300	0.228	0.248
e	1.270TYP		0.050TYP	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Package TSSOP8









Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
D	2.900	3.100	0.114	0.122
E	4.300	4.500	0.169	0.177
b	0.190	0.300	0.007	0.012
C	0.090	0.200	0.004	0.008
E1	6.250	6.550	0.246	0.258
A		1.200		0.047
A2	0.800	1.000	0.031	0.039
A1	0.050	0.150	0.002	0.006
e	0.65(BSC)		0.026(BSC)	
L	0.500	0.700	0.020	0.028
H	0.25(TYP)		0.01(TYP)	
θ	1°		1°	

Important statement:

●TUDI Semiconductor reserves the right to modify the product manual without prior notice! Before placing an order, customers need to confirm whether the obtained information is the latest version and verify the completeness of the relevant information.

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