1.General Description

The 74HC166 and 74HCT166 are 8-bit serial or parallel-in/serial-out shift registers. The device features a serial data input (DS), eight parallel data inputs (D0 to D7) and a serial output (Q7). When the parallel enable input ($\overline{PE}$) is LOW, the data from D0 to D7 is loaded into the shift register on the next LOW-to-HIGH transition of the clock input (CP). When $\overline{PE}$ is HIGH, data enters the register serially at DS with each LOW-to-HIGH transition of CP. When the clock enable input ($\overline{CE}$) is LOW data is shifted on the LOW-to-HIGH transitions of CP. A HIGH on $\overline{CE}$ disables the CP input. Inputs include clamp diodes which enable the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.

2.Features and Benefits

- Wide supply voltage range from 2.8 V to 6.0 V
- High noise immunity
- CMOS low power dissipation
- Synchronous parallel-to-serial applications
- Synchronous serial input for easy expansion
- Latch-up performance exceeds 250 mA
- Complies with JEDEC standard:
  - JESD8C(2.8 V to 3.6 V)
  - JESD7A(2.8 V to 6.0 V)
- Input levels:
  - For 74HC166: CMOS level
  - For 74HCT166: TTL level
- ESD protection:
  - HBM ANSI/ESDA/JEDEC JS-001 Class 2 exceeds 3500 V
  - CDM ANSI/ESDA/JEDEC JS-002 Class C3 exceeds 2000 V
- Multiple package options
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

3.Ordering Information

Table 1. Ordering information

Type number	Package		
	Name	Description	Quantity
74HC166D	SOP-16L	plastic small outline package; 16 leads; body width 3.9 mm	2500
74HCT166D			
74HC166PW	TSSOP-16L	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	2500
74HCT166PW			

4.Function Diagram

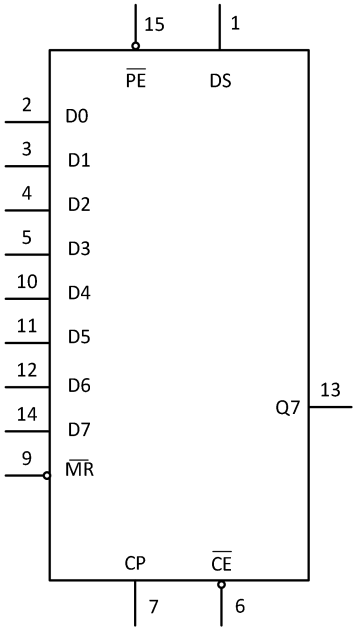


Fig. 1. Logic symbol

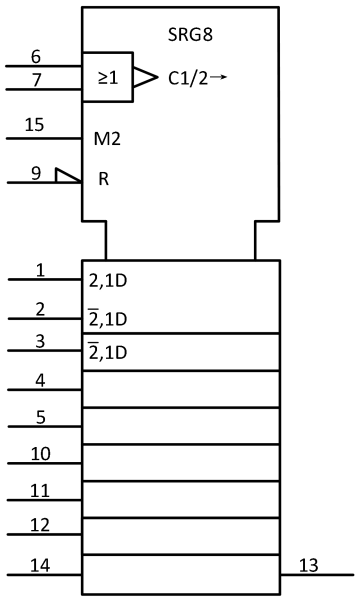


Fig. 2. IEC logic symbol

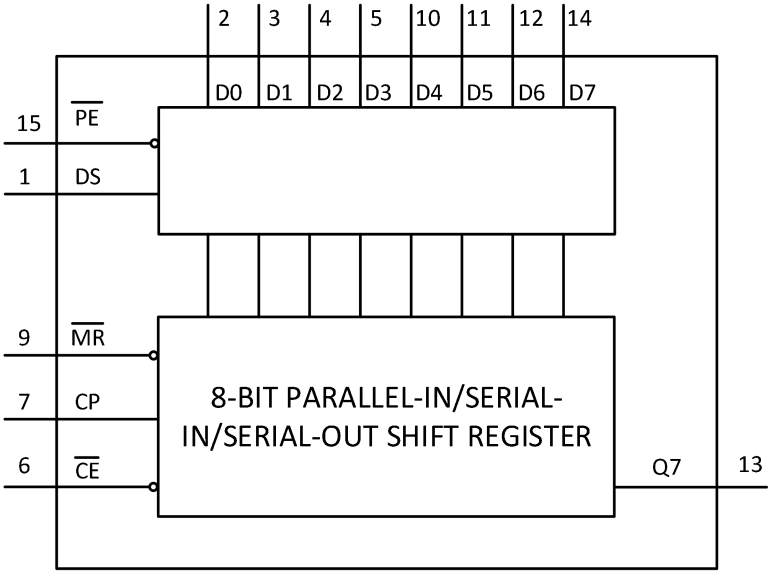


Fig. 3. Functional diagram

5.Pinning Information

5.1. Pinning

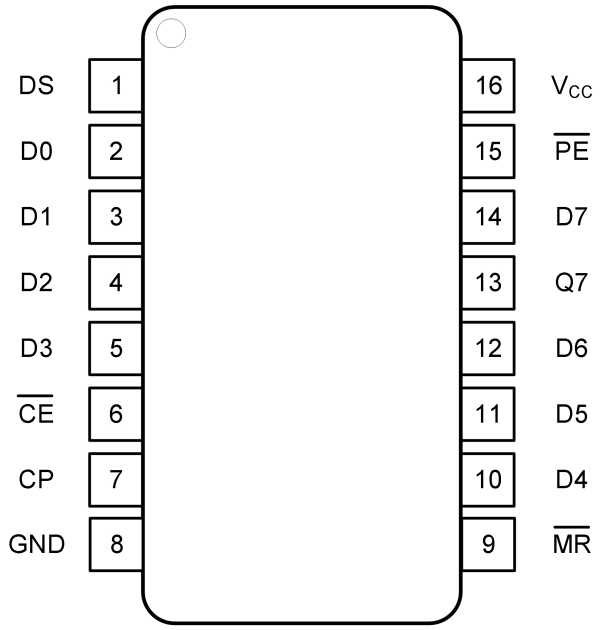


Fig. 4. Top view pin configuration SOP and TSSOP

5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
DS	1	serial data input
D0 to D7	2, 3, 4, 5, 10, 11, 12, 14	parallel data inputs
$\overline{CE}$	6	clock enable input (active LOW)
CP	7	clock input (LOW-to-HIGH edge-triggered)
GND	8	ground (0 V)
$\overline{MR}$	9	asynchronous master reset (active LOW)
Q7	13	serial output from the last stage
$\overline{PE}$	15	parallel enable input (active LOW)
V_{CC}	16	supply voltage

6.Functional Description

Table 3. Function table

H = HIGH voltage level;
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition;
L = LOW voltage level;
l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition;
q = state of the referenced input one set-up time prior to the LOW-to-HIGH clock transition;
X = don't care
↑ = LOW-to-HIGH transition.

Operating modes	Inputs					Qn registers		Outputs
	$\overline{PE}$	$\overline{CE}$	CP	DS	D0 to D7	Q0	Q1 to Q6	Q7
parallel load	l	l	↑	X	l	L	L to L	L
	l	l	↑	X	h	H	H to H	H
serial shift	h	l	↑	l	X	L	q0 to q5	q6
	h	l	↑	h	X	H	q0 to q5	q6
Hold"do nothing"	X	H	X	X	X	q0	q1 to q6	q7

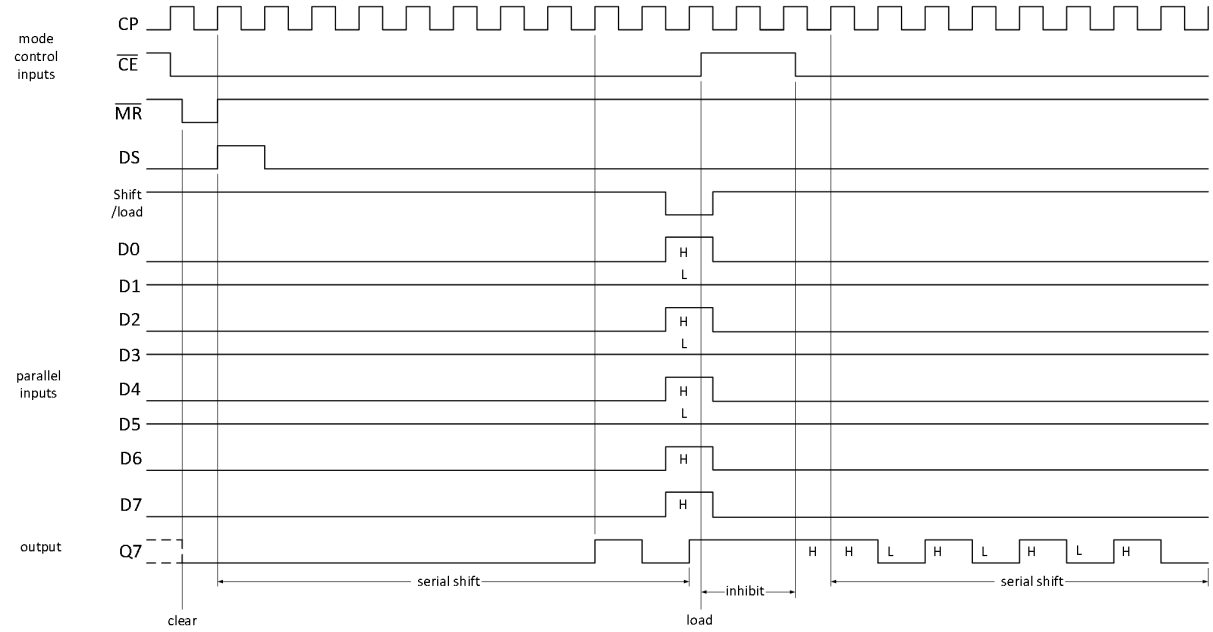


Fig. 5. Typical clear, shift, load, inhibit, and shift sequences

7. Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Table 4. Absolute Maximum Ratings

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	7.0	V
I_{IK}	input clamping current	$V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V [1]		±20	mA
I_{OK}	output clamping current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V [1]		±20	mA
I_O	output current	-0.5 V $< V_O < V_{CC} + 0.5$ V		±25	mA
I_{CC}	supply current			50	mA
I_{GND}	ground current		-50		mA
P_{tot}	total power dissipation	T_{amb} = -40 °C to + 125 °C		500	mW
T_{stg}	storage temperature		-65	150	°C

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

8. Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. EnergyMath does not recommend exceeding them or designing to Absolute Maximum Ratings.

Table 5. Recommended Operating Conditions

Symbol	Parameter	Conditions	74HC166			74HCT166			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	supply voltage		2.8	5.0	6.0	4.5	5.0	5.5	V
V_I	input voltage		0		V_{CC}	0		V_{CC}	V
V_O	output voltage		0		V_{CC}	0		V_{CC}	V
T_{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	V_{CC} = 3.0 V			371				ns/V
		V_{CC} = 4.5 V		1.67	139		1.67	139	ns/V
		V_{CC} = 6.0 V			83				ns/V

9.Static Characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
74HC166								
V_{IH}	HIGH-level input voltage	V_{CC} = 3.0 V	2.0	1.8		2.0		V
		V_{CC} = 4.5 V	3.15	2.4		3.15		V
		V_{CC} = 6.0 V	4.2	3.5		4.2		V
V_{IL}	LOW-level input voltage	V_{CC} = 3.0 V		1.3	0.6		0.6	V
		V_{CC} = 4.5 V		2.1	1.35		1.35	V
		V_{CC} = 6.0 V		2.8	1.8		1.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}						
		I_O = -20µA; V_{CC} = 3.0 V	2.9	3.0		2.9		V
		I_O = -20µA; V_{CC} = 4.5 V	4.4	4.5		4.4		V
		I_O = -20µA; V_{CC} = 6.0 V	5.9	6.0		5.9		V
		I_O = -4.0 mA; V_{CC} = 4.5 V	3.84	4.4		3.7		V
		I_O = -5.2 mA; V_{CC} = 6.0 V	5.34	5.9		5.2		V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}						
		I_O = 20µA; V_{CC} = 3.0 V		0	0.1		0.1	V
		I_O = 20µA; V_{CC} = 4.5 V		0	0.1		0.1	V
		I_O = 20µA; V_{CC} = 6.0 V		0	0.1		0.1	V
		I_O = 4.0 mA; V_{CC} = 4.5 V		0.04	0.33		0.4	V
		I_O = 5.2 mA; V_{CC} = 6.0 V		0.05	0.33		0.4	V
I_I	input leakage current	V_I = V_{CC} or GND ; V_{CC} = 6.0 V		0.1	±1		±1	µA
I_{CC}	supply current	V_I = V_{CC} or GND ; I_O = 0A ; V_{CC} = 6.0 V		11	20		40	µA
C_I	input capacitance	Pin PL,DS		4.3				pF
		Pin CP, CE		7.0				pF
		Pin D0 to D7		8.6				pF

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	
74HCT166								
V_{IH}	HIGH-level input voltage	V_{CC} = 4.5 V to 5.5 V	2.0			2.0		V
V_{IL}	LOW-level input voltage	V_{CC} = 4.5 V to 5.5 V			0.8		0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL};						
		I_O = -20 µA; V_{CC} = 4.5 V	4.4			4.4		V
		I_O = -4.0 mA; V_{CC} = 4.5 V	3.84			3.7		V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL};						
		I_O = 20 µA; V_{CC} = 4.5 V			0.1		0.1	V
		I_O = 5.2 mA; V_{CC} = 4.5 V			0.33		0.4	V
I_I	input leakage current	V_I = V_{CC} or GND ; V_{CC} = 5.5 V			±1		±1	µA
I_{CC}	supply current	V_I = V_{CC} or GND; I_O = 0 A; V_{CC} = 5.5 V			20		40	µA
ΔI_{CC}	additional supply current	per pin ; V_I = V_{CC} - 2.1 V; I_O = 0 A; other inputs at V_{CC} or GND; V_{CC} = 4.5 V to 5.5 V			400		490	µA
C_I	input capacitance			4.0				pF

[1]All typical values are measured at T_{amb} = 25°C.

10. Dynamic Characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 9.

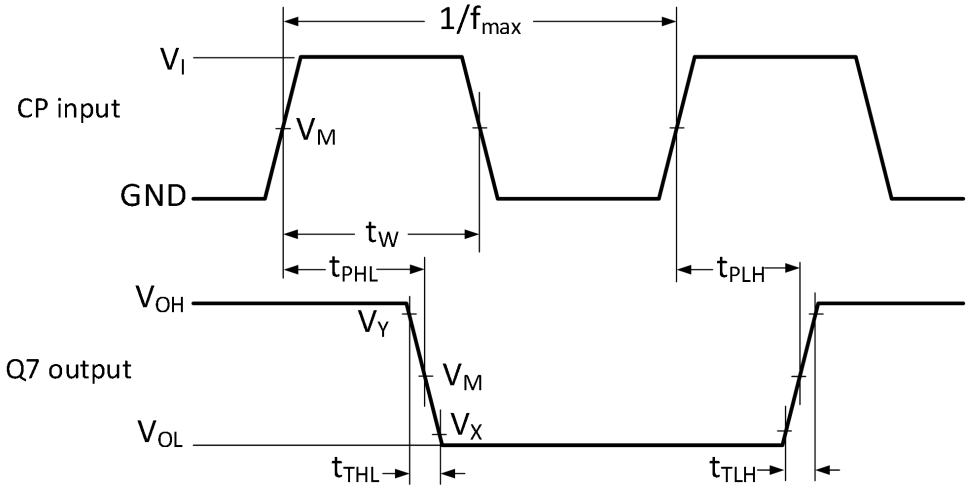
Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
74HC166								
t_{pd}	propagation delay	CP to Q7; see Fig. 6 [2]						
		V_{CC} = 3.0 V		18.4	27		30	ns
		V_{CC} = 4.5 V		12.5	17		20	ns
		V_{CC} = 6.0 V		10.4	13		15	ns
		$\overline{MR}$ to Q7; see Fig. 7						
		V_{CC} = 3.0 V		17.9	27		30	ns
		V_{CC} = 4.5 V		11.8	17		20	ns
		V_{CC} = 6.0 V		9.7	13		15	ns
t_t	transition time	output; see Fig. 6 [3]						
		V_{CC} = 3.0 V		3.1	8		10	ns
		V_{CC} = 4.5 V		2.2	7		9	ns
		V_{CC} = 6.0 V		1.9	7		9	ns
t_W	pulse width	CP HIGH or LOW;see Fig. 6						
		V_{CC} = 3.0 V	25			31		ns
		V_{CC} = 4.5 V	20			24		ns
		V_{CC} = 6.0 V	17			20		ns
		$\overline{MR}$ input LOW; see Fig. 7						
		V_{CC} = 3.0 V	20			25		ns
		V_{CC} = 4.5 V	15			18		ns
		V_{CC} = 6.0 V	13			15		ns
t_{rec}	recovery time	$\overline{MR}$ to CP; see Fig. 7						
		V_{CC} = 3.0 V	20			23		ns
		V_{CC} = 4.5 V	15			18		ns
		V_{CC} = 6.0 V	13			15		ns

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
t_{SU}	set up time	Dn, $\overline{CE}$ to CP; see Fig. 8						
		V_{CC} = 3.0 V	25			30		ns
		V_{CC} = 4.5 V	20			24		ns
		V_{CC} = 6.0 V	17			20		ns
		$\overline{PE}$ to CP;see Fig. 8						
		V_{CC} = 3.0 V	25			30		ns
		V_{CC} = 4.5 V	20			24		ns
		V_{CC} = 6.0 V	17			20		ns
t_h	hold time	Dn, $\overline{CE}$ to CP; see Fig. 8						
		V_{CC} = 3.0 V	5			5		ns
		V_{CC} = 4.5 V	5			5		ns
		V_{CC} = 6.0 V	5			5		ns
		$\overline{PE}$ to CP; see Fig. 8						
		V_{CC} = 3.0 V	5			5		ns
		V_{CC} = 4.5 V	5			5		ns
		V_{CC} = 6.0 V	5			5		ns
f_{max}	maximum frequency	for CP; see Fig. 6						
		V_{CC} = 3.0 V	20			16		MHz
		V_{CC} = 4.5 V	24			20		MHz
		V_{CC} = 6.0 V	28			24		MHz
C_{PD}	power dissipation capacitance	per package ; V_I = GND to V_{CC} ; [4]		26				pF
74HCT166								
t_{pd}	propagation delay	CP to Q7; see Fig. 6 [2]						
		V_{CC} = 4.5 V		12.5	17		20	ns
		$\overline{MR}$ to Q7; see Fig. 7						
		V_{CC} = 4.5 V		11.8	17		20	ns
t_t	transition time	output; see Fig. 6 [3]						
		V_{CC} = 4.5 V		2.2	7		9	ns

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
t_W	pulse width	CP HIGH or LOW;see Fig. 6						
		V_{CC} = 4.5 V	20			24		ns
		$\overline{MR}$ input LOW; see Fig. 7						
		V_{CC} = 4.5 V	15			18		ns
t_{rec}	recovery time	$\overline{MR}$ to CP; see Fig. 7						
		V_{CC} = 4.5 V	15			18		ns
t_{SU}	set up time	Dn, $\overline{CE}$ to CP; see Fig. 8						
		V_{CC} = 4.5 V	20			24		ns
		$\overline{PE}$ to CP;see Fig. 8						
		V_{CC} = 4.5 V	20			24		ns
t_h	hold time	Dn, $\overline{CE}$ to CP; see Fig. 8						
		V_{CC} = 4.5 V	5			5		ns
		$\overline{PE}$ to CP; see Fig. 8						
		V_{CC} = 4.5 V	5			5		ns
f_{max}	maximum frequency	for CP; see Fig. 6						
		V_{CC} = 4.5 V	24			20		MHz
C_{PD}	power dissipation capacitance	per package ; V_I = GND to V_{CC} - 1.5 ; [4]		26				pF

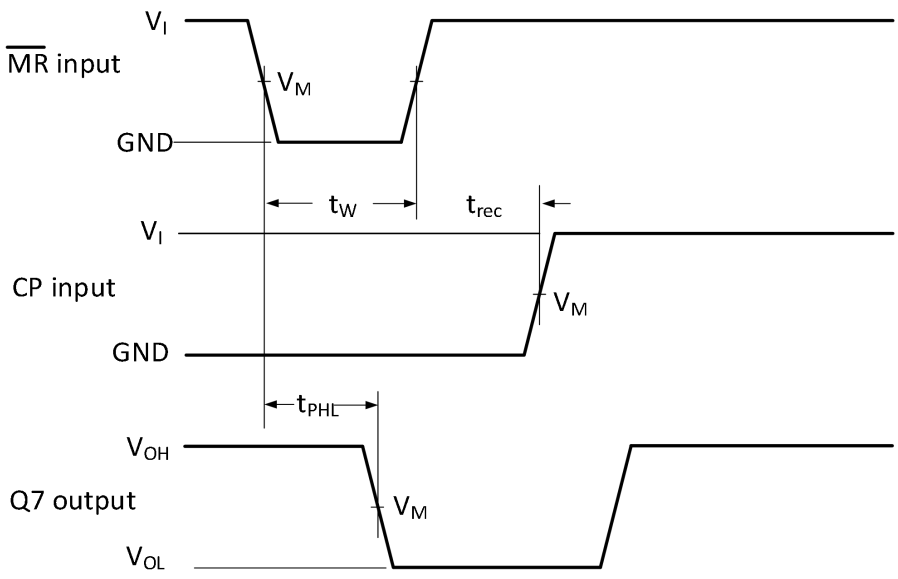
[1] Typical values are measured at T_{amb} = 25 °C.
[2] t_{pd} is the same as t_{PLH} and t_{PHL}.
[3] t_t is the same as t_{THL} and t_{THL}.
[4] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

11. Waveforms and test circuit



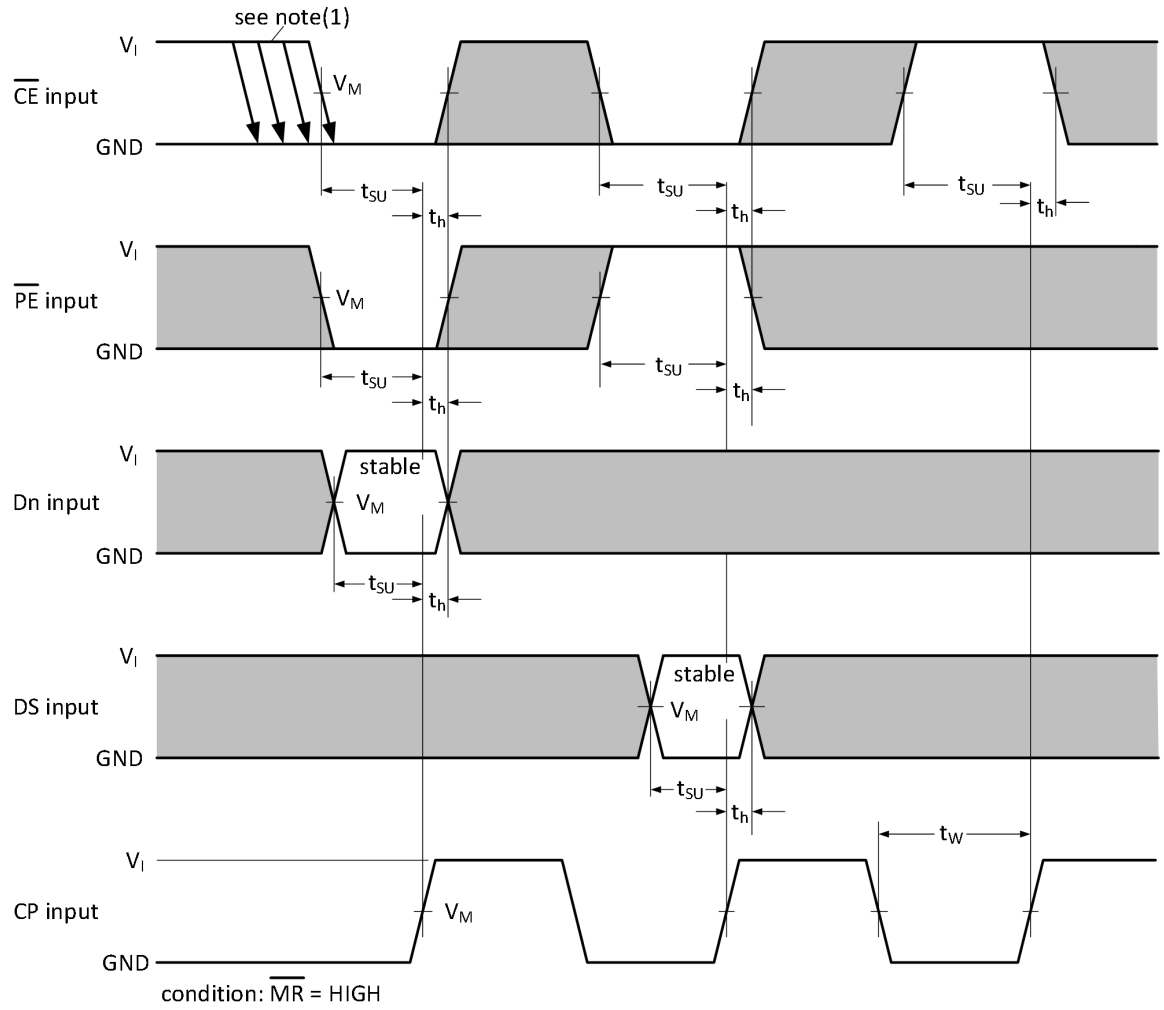
Measurement points are given in Table 8.
V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 6. Clock (CP) to output (Q7) propagation delays, pulse width, output transition times and maximum frequency



Measurement points are given in Table 8.
V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 7. Master reset (MR) pulse width, MR to output (Q7) propagation delay and MR to clock (CP) recovery time



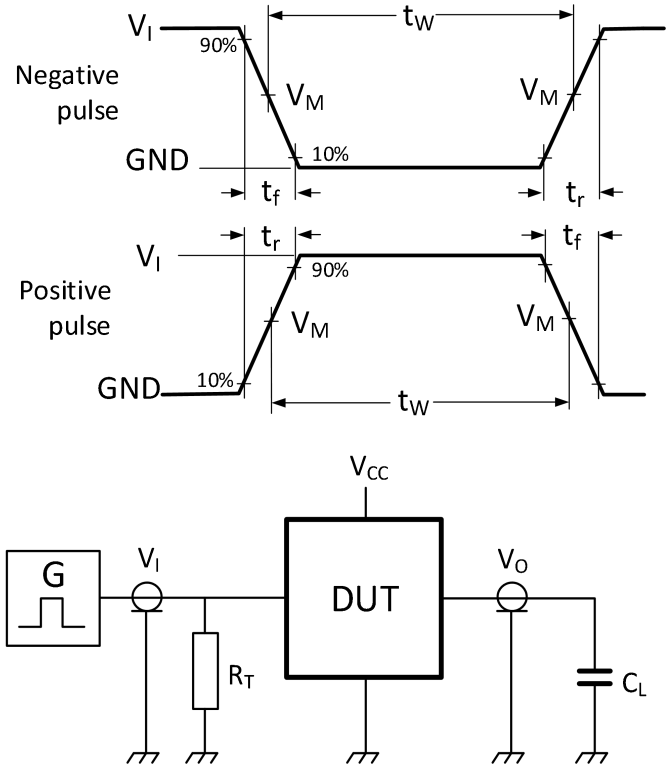
The shaded areas indicate when the input is permitted to change for predictable output performance Measurement points are given in Table 8 .

(1) $\overline{CE}$ may change only from HIGH-to-LOW while CP is LOW.

Fig. 8. Set-up and hold times

Table 8. Measurement points

Type	Input		Output
	V_I	V_M	V_M
74HC166	V_{CC}	$0.5V_{CC}$	$0.5V_{CC}$
74HCT166	3 V	1.3 V	1.3 V



Test data is given in Table 9.
Definitions for test circuit:
C_L = Load capacitance including jig and probe capacitance.
R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

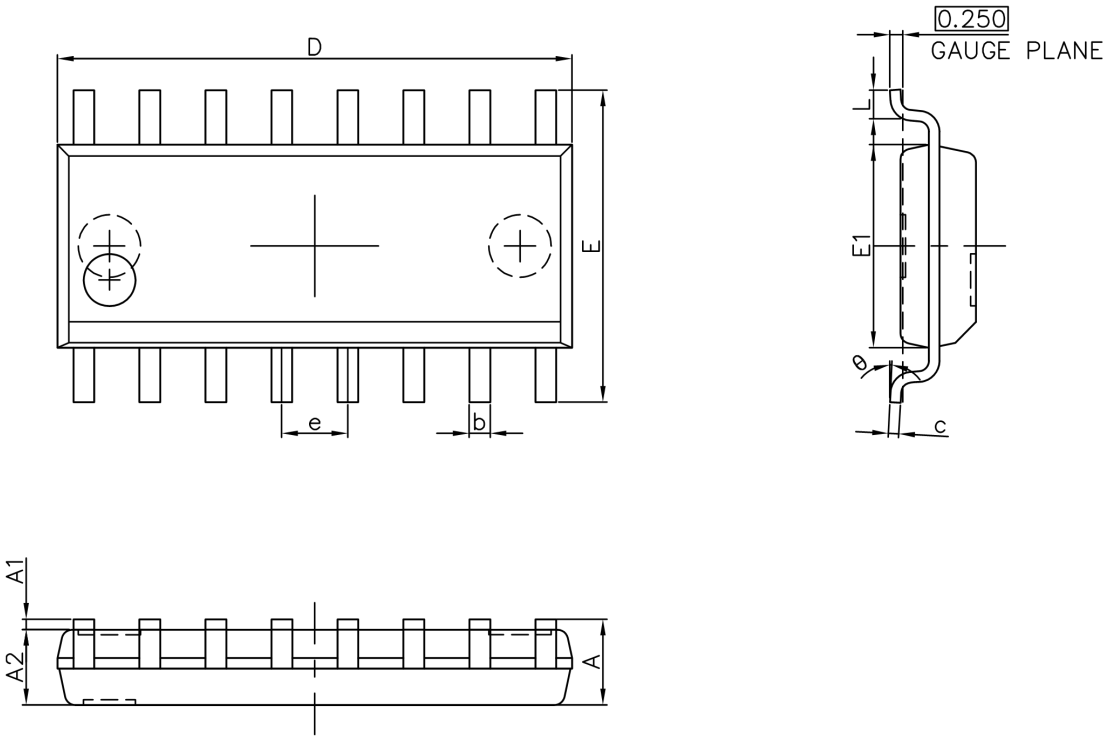
Fig. 9. Test circuit for measuring switching times

Table 9. Test data

Type	Input		Load	Test
	V_I	$t_r = t_f$	C_L	
74HC166	V_{CC}	2.5 ns	50 pF	t_{PHL}, t_{PLH}
74HCT166	3 V	2.5 ns	50 pF	t_{PHL}, t_{PLH}

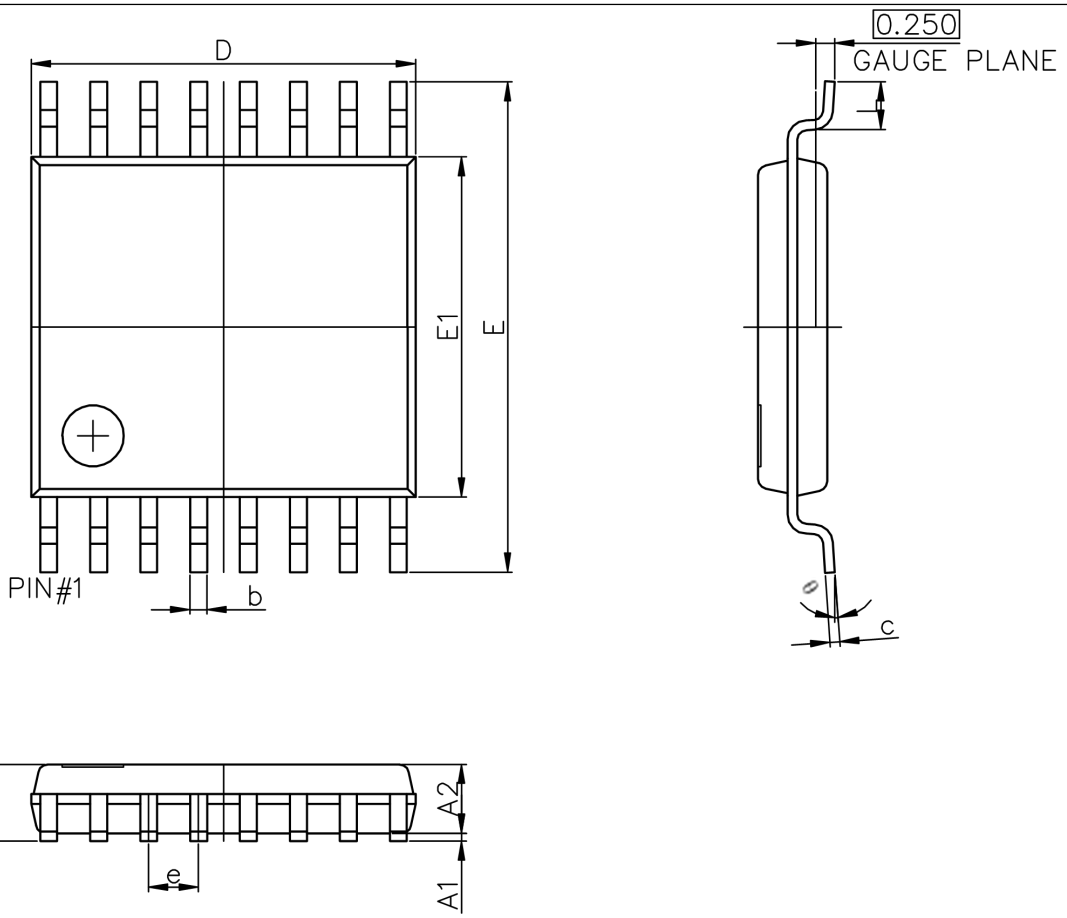
12. Package Outline

SOP-16L



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	——	1.750	——	0.069
A1	0.150	0.250	0.006	0.010
A2	1.400	1.500	0.055	0.059
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	9.800	10.000	0.386	0.394
e	1.270(BSC)		0.050(BSC)	
E	5.900	6.100	0.232	0.240
E1	3.800	4.000	0.150	0.157
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

TSSOP-16L



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	——	1.200	——	0.047
A1	0.020	0.100	0.001	0.004
A2	0.800	1.000	0.031	0.039
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
D	4.900	5.100	0.193	0.201
e	0.650(BSC)		0.026(BSC)	
E	6.250	6.550	0.252(BSC)	
E1	4.300	4.500	0.169	0.177
L	0.500	0.700	0.020	0.028
θ	1°	7°	1°	7°

13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
CDM	Charged Device Model
TTL	Transistor-Transistor Logic

14. Revision History

Table 11. Revision history

Document ID	Release Date	Data sheet status	Change notice	Supersedes
74HC_HCT166 Rev. 1.0	Feb 20, 2025	Product datasheet		