

Description

The US5D8543 is a low skew, high performance 2-to-4 clock fanout buffer. Utilizing Low Voltage Differential Signaling (LVDS) the US5D8543 provides a low power, low noise, solution for distributing clock signals. The US5D8543 has two selectable clock inputs. The CLK, nCLK pair can accept most standard differential input levels. The PCLK, nPCLK pair can accept LVPECL input levels. Guaranteed output and part-to-part skew characteristics make the US5D8543 ideal for those applications demanding well defined performance and repeatability.

The US5D8543 clock buffer distributes two clock inputs to 4 pairs of differential LVDS clock outputs with minimum skew for clock distribution. It has a maximum clock frequency up to 2-GHz.

The device is designed for a signal fanout of high-frequency, low phase-noise clock and data signal.

Features

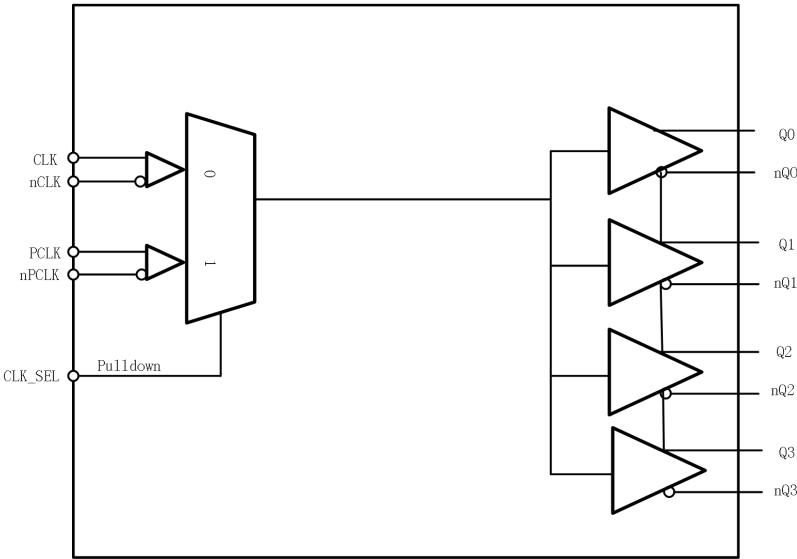
- 2:4 Differential Buffer
- Selectable differential CLK, nCLK or LVPECL clock inputs
- CLK, nCLK pair can accept the following differential input levels: LVDS, LVPECL, HCSL, LVCMOS
- PCLK, nPCLK pair can accept the following differential input levels: LVPECL
- Four LVDS outputs
- Maximum Output Frequency
LVDS - 2-GHz
- Propagation Delay: 0.5 ns(typical)
- Output skew: 50 ps (Maximum)
- Part-to-part skew: 500ps (Maximum)
- Additive RMS phase jitter 3.3V@ 156.25MHz:
58 fs RMS (12kHz - 20MHz)
- 3.3V or 2.5V operating supply
- Industrial Temperature Range:-40°C to 85°C
- Available in TSSOP-20 package

Applications

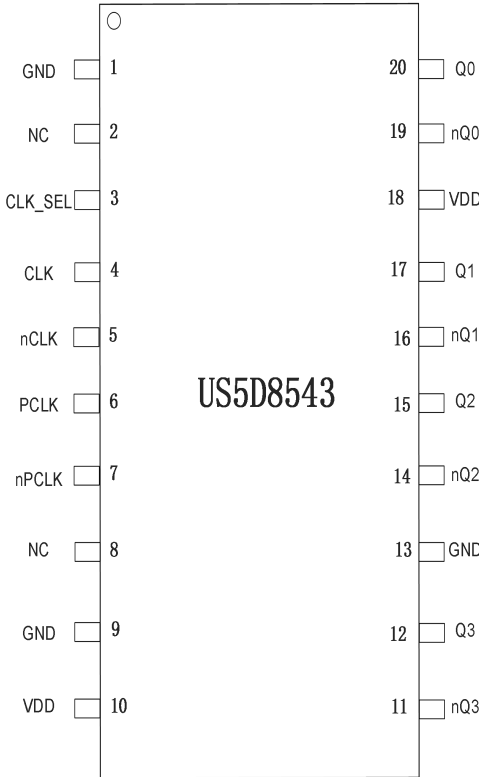
- Clock Distribution
- Wireless Base Stations
- Network Routers



Block Diagram



Pin Assignment for TSSOP-20 Package



Pin Description and Pin Characteristic Tables

Table 1: Pin Descriptions

Number	Name	Type	Description
1	GND	Power	Ground.
9	GND	Power	Ground.
13	GND	Power	Ground.
2	NC	---	Not connect.
3	CLK_SEL	Input	Clock select input. When HIGH selects differential PCLK nPCLK inputs. When LOW selects differential CLK nCLK inputs.
4	CLK	Input	Non-inverting differential clock input.
5	nCLK	Input	Inverting differential clock input.
6	PCLK	Input	Non-inverting differential LVPECL clock input.
7	nPCLK	Input	Inverting differential LVPECL clock input.
8	NC	---	Not connect.
10	VDD	Power	Power supply pin.
18	VDD	Power	Power supply pin.
11	Q3	Output	Differential output pair number 3.
12	nQ3	Output	Differential output pair number 3.
14	Q2	Output	Differential output pair number 2.
15	nQ2	Output	Differential output pair number 2.
16	Q1	Output	Differential output pair number 1.
17	nQ1	Output	Differential output pair number 1.
19	Q0	Output	Differential output pair number 0.
20	nQ0	Output	Differential output pair number 0.

Table 2: CLOCK INPUTS FUNCTION TABLE

INPUTS		OUTPUTS		Input to Output Mode	Polarity
CLK,PCLK	nCLK,nPCLK	Q0,Q1,Q2,Q3	nQ0,nQ1,nQ2,nQ3		
0	1	Low	High	Differential to Differential	Non Inverting
1	0	High	Low	Differential to Differential	Non Inverting
0	Biased; note1	Low	High	Single ended to Differential	Non Inverting
1	Biased; note1	High	Low	Single ended to Differential	Non Inverting
Biased; note1	0	High	Low	Single ended to Differential	Inverting
Biased; note1	1	Low	High	Single ended to Differential	Inverting

NOTE1: Single ended use requires that one of the differential inputs be biased. The voltage at the biased input sets the switch point for the single ended input. For LVCMOS and LVTTL levels the recommended input bias network is a resistor to VDD, a resistor of equal value to ground and a 0.1μF capacitor from the input to ground. The resulting switch point is approximately $VCC/2 \pm 300mV$.

Absolute Maximum Ratings

Exposure to absolute maximum rating conditions for extended periods may affect product reliability. Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of the product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied.

Item	Rating
V_{DD}	4.6V
V_{IN}	-0.5V to $V_{DD} + 0.5V$
T_J :Junction Temperature	125°C
T_{STG} :Storage Temperature	-65°C to 150°C

ESD Ratings

		Max	Unit
V(ESD) Electrostatic discharge	Human-body model (HBM), ANSI/ESDA/JEDEC JS-001-2017	±2500	V
	Machine model (MM), JEDEC Std. JESD22-A115-C	±250	
	Charged-device model (CDM), ANSI/ESDA/JEDEC JS-002-2018	±750	

Latch up

		Max	Unit
Latch up	I-test, JEDEC STD JESD78E	±200	mA
	V-test, JEDEC STD JESD78E	4.6	V

Recommended Operating Conditions

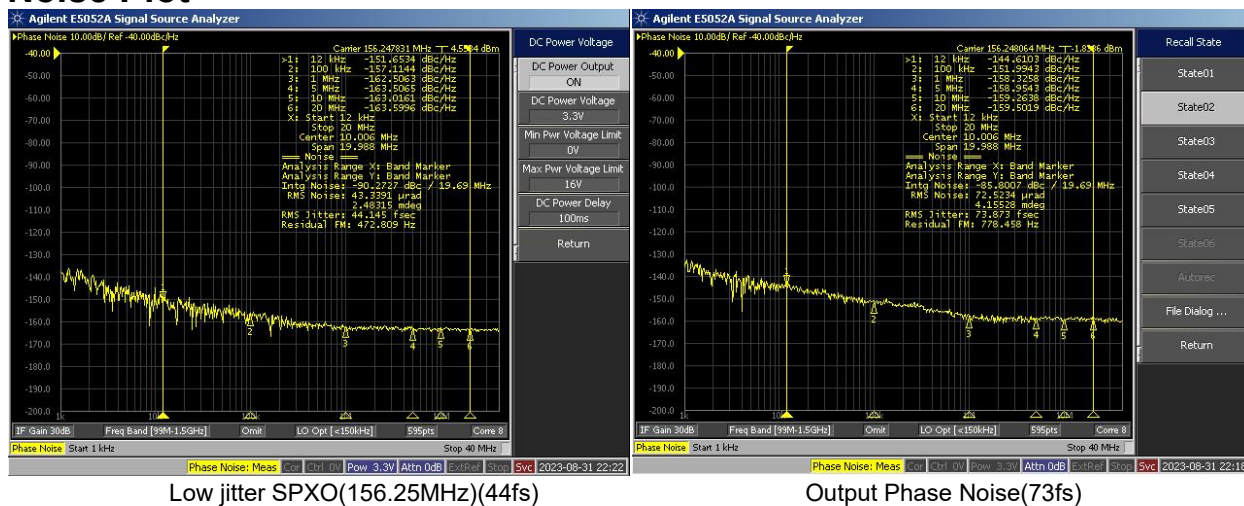
Symbol	Parameter	Min	Typ	Max	Unit
T_A	Ambient air temperature	-40		85	°C
T_J	Junction temperature			125	°C
V_{DD}	Power supply for Core and input Buffer blocks	3.3-5%	3.3	3.3+5%	V
		2.5-5%	2.5	2.5+5%	V

Electrical Characteristics

VDD = 3.135 V to 3.465 V and TA = -40°C to 85°C (unless otherwise noted).

Parameter		Test Conditions	Min	Typ	Max	Unit
LVC MOS DC Characteristics						
V _{IH}	Input high voltage		2			V
V _{IL}	Input low voltage				0.8	V
I _{IH}	Input high current	CLK_SEL, VDD=V _{IN} =3.465V			150	μA
I _{IL}	Input low current	CLK_SEL, VDD=3.465V, V _{IN} =0V	-5			μA
Differential DC Characteristics						
I _{IH}	Input high current	CLK, VDD=V _{IN} =3.465V			150	μA
		nCLK, VDD=V _{IN} =3.465V			5	μA
I _{IL}	Input low current	CLK, VDD=3.465V, V _{IN} =0V	-5			μA
		nCLK, VDD=3.465V, V _{IN} =0V	-150			μA
V _{pp}	Peak-to-Peak Voltage;		0.15		1.3	V
V _{CMR}	Common Mode Input Voltage;		0.5		VDD-0.85	V
LVPECL DC Characteristics						
I _{IH}	Input high current	PCLK, VDD=V _{IN} =3.465V			150	μA
		nPCLK, VDD=V _{IN} =3.465V			5	μA
I _{IL}	Input low current	PCLK, VDD=3.465V, V _{IN} =0V	-5			μA
		nPCLK, VDD=3.465V, V _{IN} =0V	-150			μA
V _{pp}	Peak-to-Peak Voltage		0.3		1	V
V _{CMR}	Common Mode Input Voltage		1.5		VDD	V
LVDS DC Characteristics						
V _{OD}	Differential Output Voltage		250	350	450	mV
Δ V _{OD}	V _{OD} Magnitude Change		-50		50	mV
V _{OS}	Differential output common-mode voltage		1.125	1.25	1.375	V
Δ V _{OS}	V _{OS} Magnitude Change			5	25	mV
AC Characteristics						
F _{IN}	Input frequency		0.1		2000	MHz
I _{DD}	operating current	VDD=3.3V, F _{IN} =156.25MHz		73		mA
t _{pLH}	Propagation Delay			0.5	1.5	ns
T _{sk(0)}	Output skew			20	50	ps
T _{sk(pp)}	Part-to-part skew				500	ps
t _R	Output rise time	RL=100Ω, 20% to 80%		120	500	ps
t _F	Output fall time	RL=100Ω, 20% to 80%		120	500	ps
t _{RJIT}	Phase jitter	@156.25MHz (12KHz-20MHz), VDD=3.3V		58	100	fs
odc	Output Duty Cycle		45	50	55	%

Phase Noise Plot



The additive phase jitter for this device was measured using the Low jitter SPXO(156.25MHz) as an input source with and Agilent E5052A phase noise analyzer. (VDD=3.3V)

Timing Diagrams

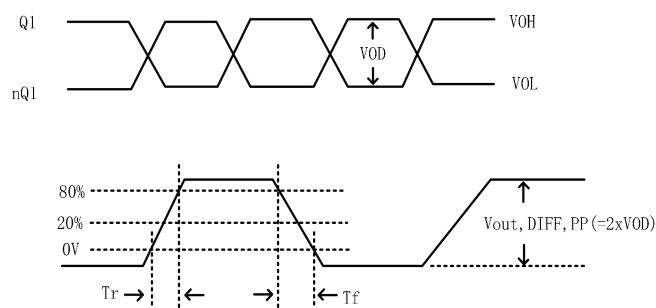
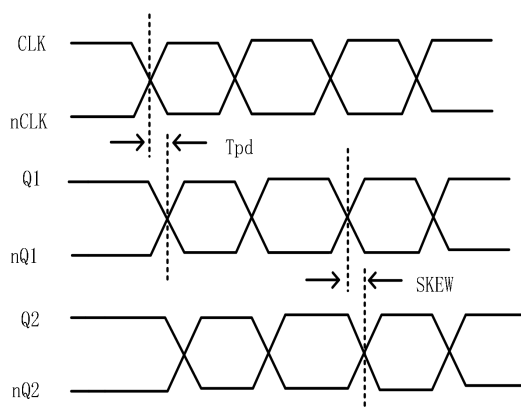


Figure 1.output voltage and rise/fall time



(1) Output skew is calculated as the greater of the following: As the difference between the fastest and the slowest tPLHn (n = 0, 1, 2....7), or as the difference between the fastest and the slowest tPHLn (n = 0, 1, 2....7).

(2) Part-to-part skew is calculated as the greater of the following: As the difference between the fastest and the slowest tPLHn (n = 0, 1, 2....7) across multiple devices, or the difference between the fastest and the slowest tPHLn (n = 0, 1, 2....7) across multiple devices

Figure 2.output and skew

Applications Information

For the single-ended input LVCMOS signal, R_s and R_0 in the driver form a $50\ \Omega$ impedance match, and the direct-isolated capacitor C_3 avoids the influence of the common-mode level between the input and output, and then drives the receiver through the voltage divider and the common-mode level to $V_{DD}/2$.

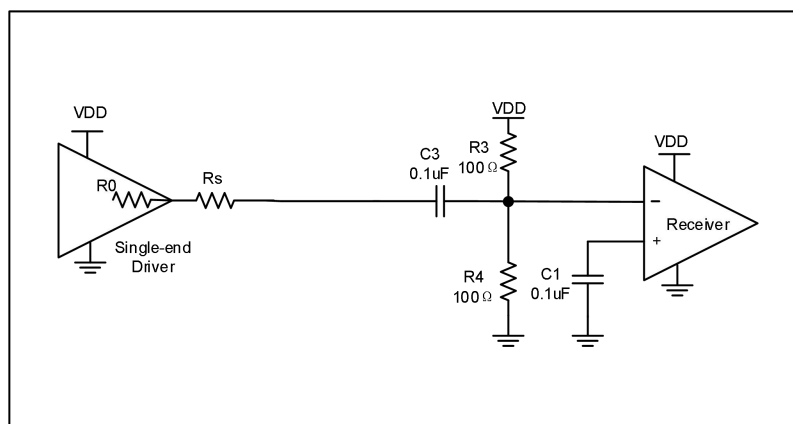
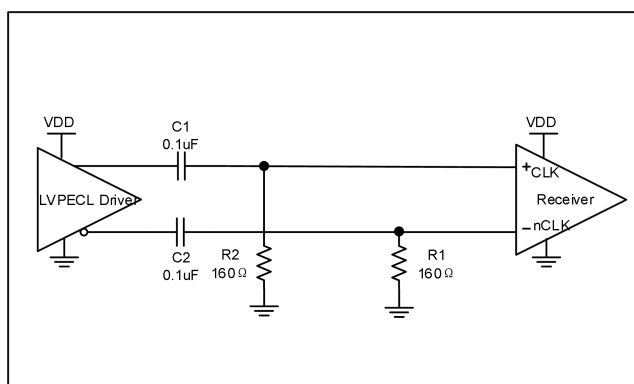


Figure3.Single-termination method of differential input

Input connection circuit

The CLK /nCLK accepts LVDS, LVPECL, HCSL and other differential signals. Both differential signals must meet the V_{PP} and V_{CMR} input requirements. Figure4 to Figure7 show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements.



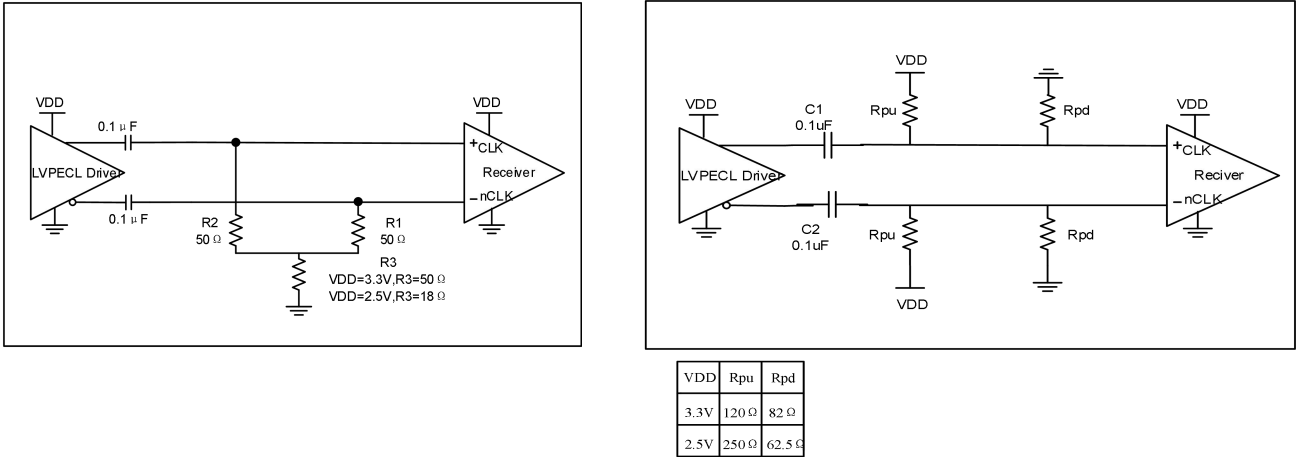


Figure4.LVPECL Driver(AC)

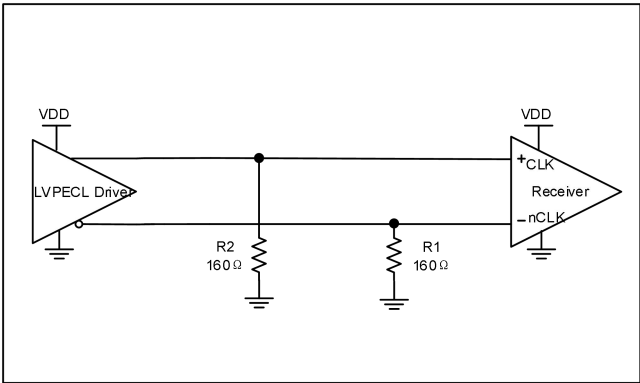
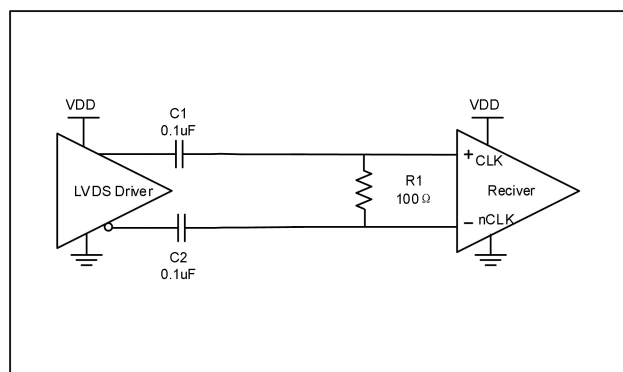
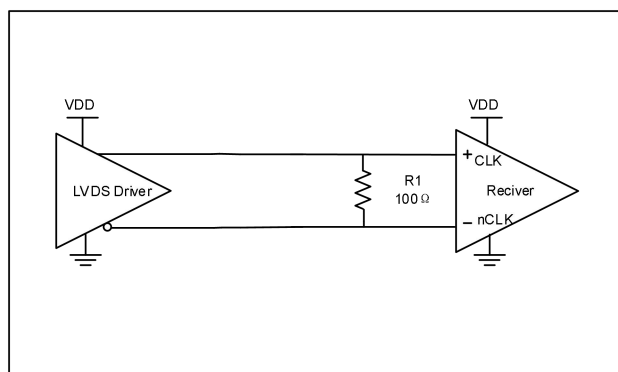


Figure5.LVPECL Driver(DC)

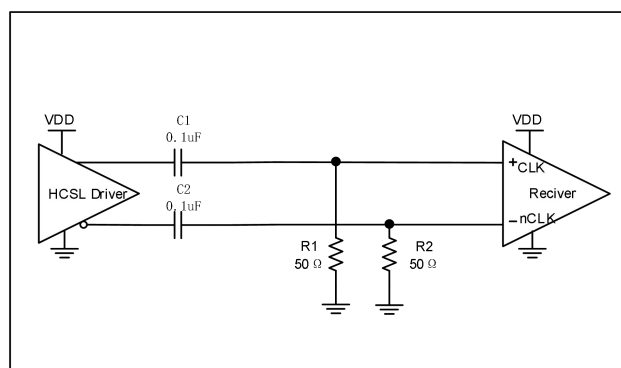


a)AC coupling

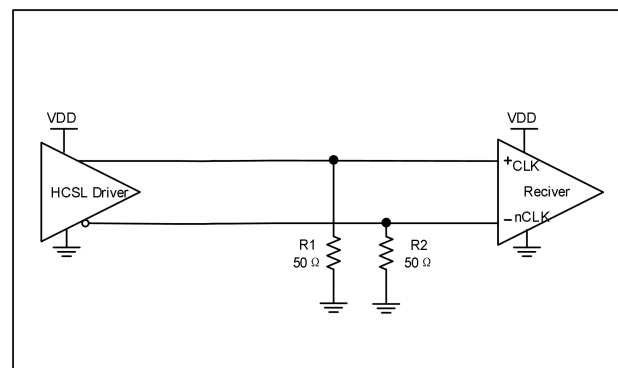


b)DC coupling

Figure6.LVDS Driver



a)AC coupling



b)DC coupling

Figure7.HCSL Driver

Output connection circuit

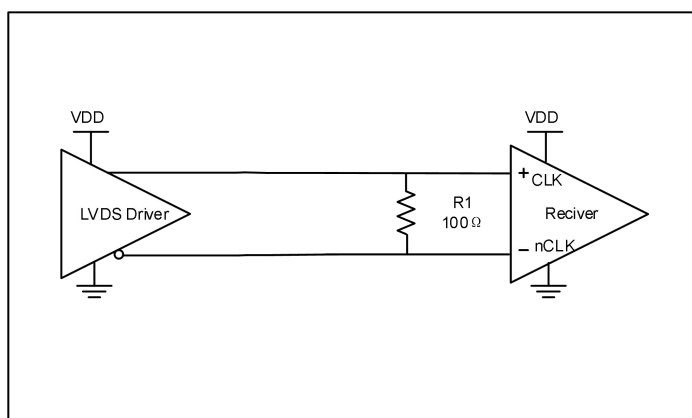
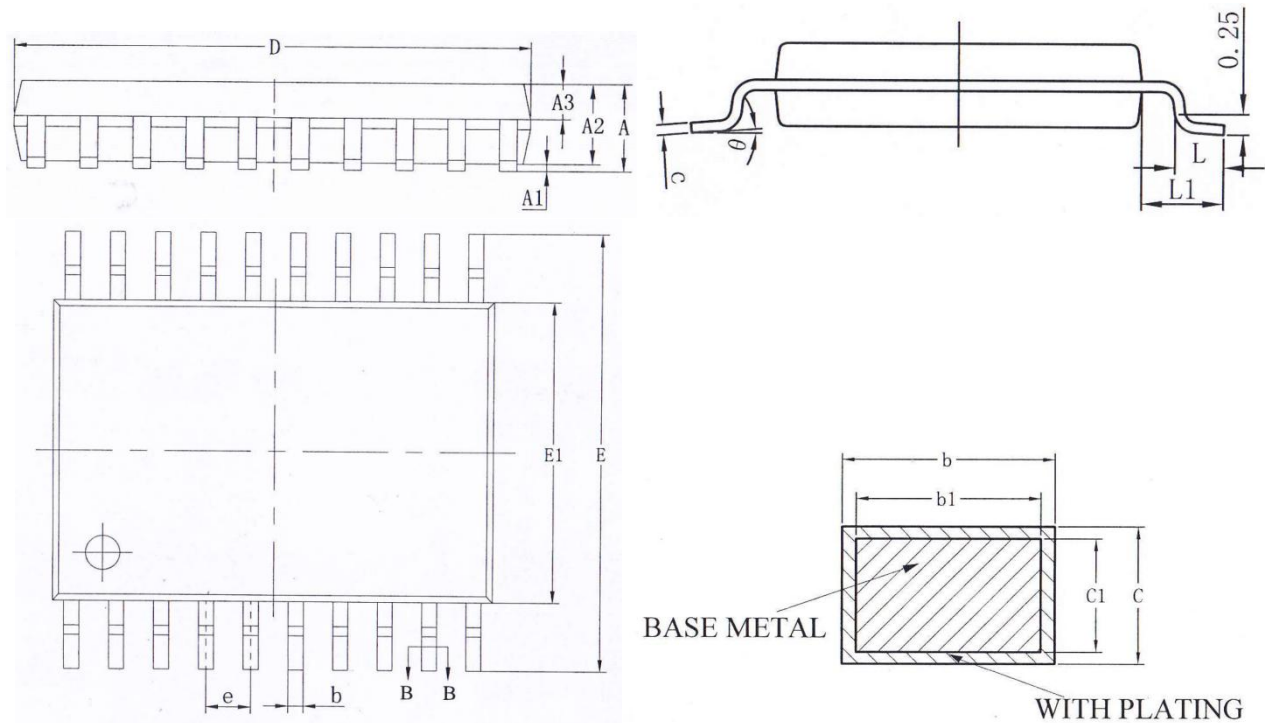


Figure8.LVDS Driver

PACKAGE DIMENSIONS(TSSOP-20)



SYMBOL	Millimeter		
	Min	Nom	Max
A	—	—	1.20
A1	0.05	—	0.15
A2	0.90	1.00	1.05
A3	0.39	0.44	0.49
b	0.20	—	0.28
b1	0.19	0.22	0.25
c	0.13	—	0.17
c1	0.12	0.13	0.14
D	6.40	6.50	6.60
E1	4.30	4.40	4.50
E	6.20	6.40	6.60
e	0.65BSC		
L	0.45	—	0.75
L1	1.00REF		
θ	0	—	8°

Reflow profile

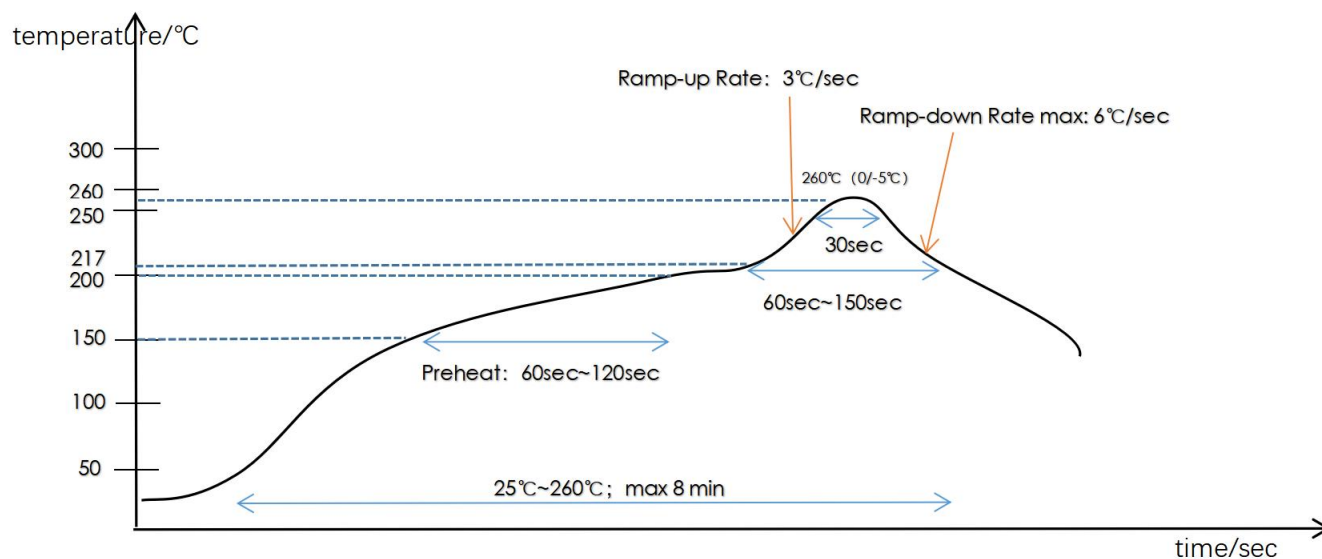


Figure9: Recommended Temperature(PB-Free)

Reflow Condition	Convection or IR/Convection
Average ramp-up rate(217°C to Peak)	3°C/second max
Preheat temperature 175(±25)°C	60~120 seconds
Temperature maintained above 217°C	60~150 seconds
Time within 5°C of actual peak temperature	30 seconds
Peak temperature range	260 +0/-5°C
Ramp-down rate	6°C/second max
Time 25°C to peak temperature	8 minutes max
Maximum number of reflow cycles	≤3

Revision History

Date	Description of Change	Revision
2023.06.19	First Draft.	1.0
2023.12.05	Modify the LVCMOS input connection	1.5