Low Offset Voltage, Low Noise, 7 MHz High Precision JFET Op Amps

Features

- Low Offset Voltage: 75 μV max
- Low Offset Voltage Drift: 0.5 μV/°C typical
  2 μV/°C max
- Low Input Bias Current: 25 pA
- Low Noise: $10\,\text{nV}/\sqrt{\text{Hz}}$ @ 1 kHz
  0.1 Hz to 10 Hz 1.75 $\mu V_{P\text{-}P}$
- Bandwidth: 7 MHz
- Slew Rate: 35 V/μS
- Fast settling time: 560 ns to 0.01%
- Supply Current: 2 mA per amplifier
- Supply Voltage: ± 4.5 V to ± 15 V or 9 V to 30 V
- Specified Temperature Range: - 40 °C to +125 °C

Applications

- Multipole filters
- Precision current measurement
- Photodiode amplifiers
- Instrumentation
- Sensors Interface
- Audio

General Description

ZJA3512 family are dual- and quad- precision JFET amplifiers that feature low offset voltage, low input bias current, low input voltage noise and low input current noise. ZJA3512's offset voltage is guaranteed to be within 75 μV, which is an order of magnitude better than traditional JFET op amps.

The combination of low offset, low noise, and very low input bias current makes these amplifiers especially suitable for high impedance sensor amplification and precise current measurement using shunts. The combination of DC precision, low noise, and fast settling time results in superior accuracy in medical instruments, electronic measurement, and automated test equipment. ZJA3512 family maintain their fast-settling performance even with substantial capacitive loads. Moreover, they do not suffer from output phase reversal when input voltages exceed the maximum common-mode voltage range.

Fast slew rate and excellent stability with capacitive load make ZJA3512 a perfect fit for high performance filters. Low input bias currents, low offset, and low noise result in a wide dynamic range of photodiode amplifier circuits. Low noise and distortion, high output current, and excellent speed make ZJA3512 a great choice for audio applications.

ZJA3512-2 is available in 8-lead narrow SOIC and 8-lead MSOP packages. ZJA3512-4 is available in 14-lead SOIC package. All of them are specified over the -40°C to +125°C extended industrial temperature range.

Typical Application

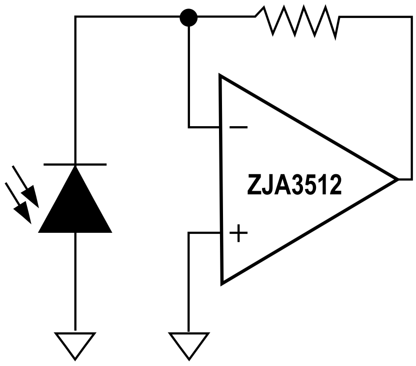

Figure 1. Photodiode amplifier

Typical Characteristics

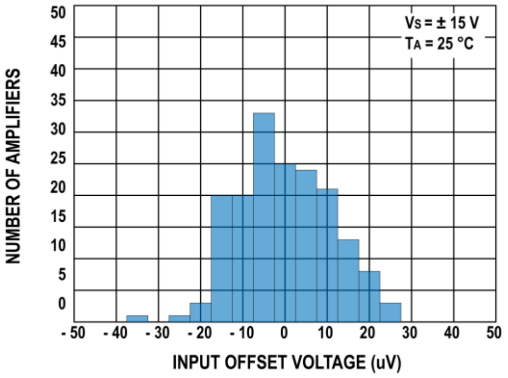

Figure 2. Offset voltage histogram

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Version (Preliminary Datasheet) [1]

Revision History

October 2023——Preliminary Datasheet

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Pin Configurations and Function

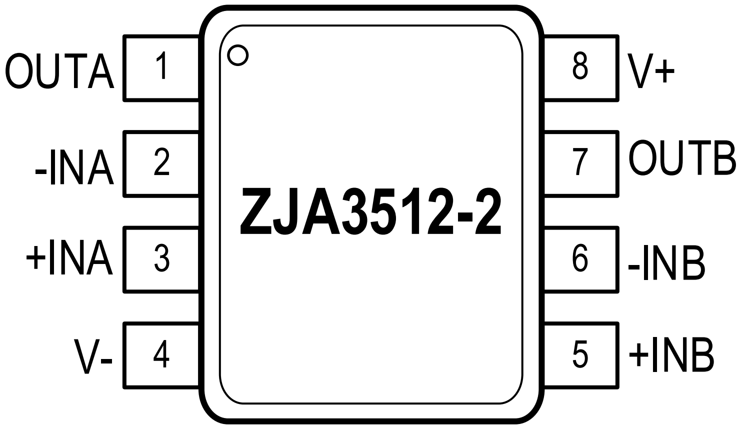

Figure 3. ZJA3512-2 Pin Configuration (8-lead SOIC and MSOP)

Mnemonic	Pin No.	I/O[1]	Description
OUTA	1	AO	Channel A output
-INA	2	AI	Channel A inverting input
+INA	3	AI	Channel A Non-inverting input
V-	4	P	Negative power supply
+INB	5	AI	Channel B Non-inverting input
-INB	6	AI	Channel B inverting input
OUTB	7	AO	Channel B output
V+	8	P	Positive power supply

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[1] AI：Analog Input；P：Power；AO：Analog Output.

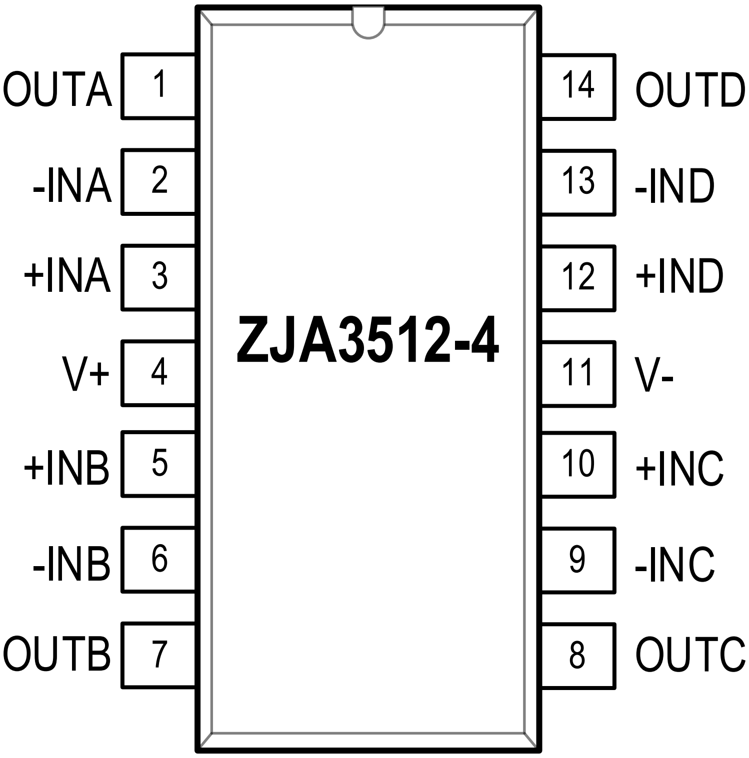

Figure 4. ZJA3512-4 Pin Configuration (14-lead SOIC)

Mnemonic	Pin No.	I/O[1]	Description
OUTA	1	AO	Channel A output
-INA	2	AI	Channel A inverting input
+INA	3	AI	Channel A non-inverting input
V+	4	P-	Positive power supply
+INB	5	AI	Channel B non-inverting input
-INB	6	AI	Channel B inverting input
OUTB	7	AO	Channel B output
OUTC	8	AO	Channel C output
-INC	9	AI	Channel C inverting input
+INC	10	AI	Channel C non-inverting input
V-	11	P	Negative power supply
+IND	12	AI	Channel D non-inverting input
-IND	13	AI	Channel D inverting input
OUTD	14	AO	Channel D output

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[1] AI：Analog Input；P：Power；AO：Analog Output.

Absolute Maximum Ratings [1]

Parameter	Rating
Supply Voltage	± 18V
Input Voltage	± Vs
Output Short-Circuit Duration to GND	TBD
Operating Temperature Range	- 40 °C to 125 °C
Storage Temperature Range	- 65 °C to 150 °C
Junction Temperature Range	- 65 °C to 150 °C
Lead Temperature, Soldering (10 sec)	300 °C
ESD Rating (ESD) [2]	
Human Body Model (HBM) [3]	2 kV
Charge Device Model (CDM) [4]	1.5 kV

Thermal Resistance [5]

Package Type	θ_{JA}	θ_{JC}	Unit
8-lead SOIC	158	43	°C/W
8-lead MSOP	190	44	°C/W
14-lead SOIC	120	36	°C/W

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[1] These ratings apply at 25°C, unless otherwise noted.
Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

[2] Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

[3] ANSI/ESDA/JEDEC JS-001 Compliant

[4] ANSI/ESDA/JEDEC JS-002 Complaint

[5] θ_{JA} addresses the conditions for soldering devices onto circuit boards to achieve surface mount packaging.

Specifications

The ● denotes the specification which apply over the full operating temperature range, otherwise specifications are at V_S = ±15 V, V_{CM} = 0 V, T_A = 25 °C, unless otherwise noted.

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
INPUT CHARACTERISTICS							
Offset Voltage	V_{OS}	B Grade			30	75	µV
			●			200	µV
		A Grade			200	500	µV
			●			1	mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	B Grade			0.5	2	µV/°C
		A Grade			4	8	µV/°C
Input Bias Current	I_B				25	80	pA
		- 40 °C < T_A< + 85 °C				0.7	nA
		- 40 °C < T_A< + 125 °C	●			10	nA
Input Offset Current	I_{OS}				5		pA
		- 40 °C < T_A< + 85 °C					nA
		- 40 °C < T_A< + 125 °C	●				nA
Input Capacitance		Differential					pF
		Common-Mode					pF
Input Voltage Range	IVR			-13.5		+ 13	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = - 12.5 V to + 12.5 V		86	108		dB
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ, V_O=± 13.5 V, V_{CM} = 0 V		90	100		dB
OUTPUT CHARACTERISTICS							
Output Voltage High	V_{OH}	R_L = 10 kΩ			14.9		V
		R_L = 2 kΩ			14.7		V
Output Voltage Low	V_{OL}	R_L = 10 kΩ			- 14.9		V
		R_L = 2 kΩ			- 14.8		V
Output Current	I_{OUT}		●	40	65		mA
Power Supply							
Supply Current per Amplifier	I_S	V_O = 0 V			2	2.1	mA
			●				mA
Power Supply Rejection Ratio	PSRR	Vs = ± 4.5 V to ± 18 V		86	105		dB

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ		35		V/μs
Gain Bandwidth Product	GBP			7		MHz
Settling Time	t_S	To 0.1%, G = +1, 0 V to 10 V Step		0.39		μs
		To 0.01%, G = +1, 0 V to 10 V Step		0.56		μs
THD + Noise	THD+N	1 kHz, G = +1, R_L = 2 kΩ		0.0003		%
Phase Margin	Φ_M			63		Degree
NOISE PERFORMANCE						
Voltage Noise Density	e_n	f = 10 Hz		52.7		$\text{nV}/\sqrt{\text{Hz}}$
		f = 100 Hz		20		$\text{nV}/\sqrt{\text{Hz}}$
		f = 1 kHz		10		$\text{nV}/\sqrt{\text{Hz}}$
		f = 10 kHz		9.7		$\text{nV}/\sqrt{\text{Hz}}$
Peak-to-Peak Voltage Noise	$e_{nP\text{-}P}$	0.1 Hz to 10 Hz Bandwidth		1.75		$\mu V_{P\text{-}P}$

Typical Performance Characteristics

Unless otherwise stated, $T_A = 25$ °C, $V_S = \pm15$ V, $R_L = 2$ kΩ.

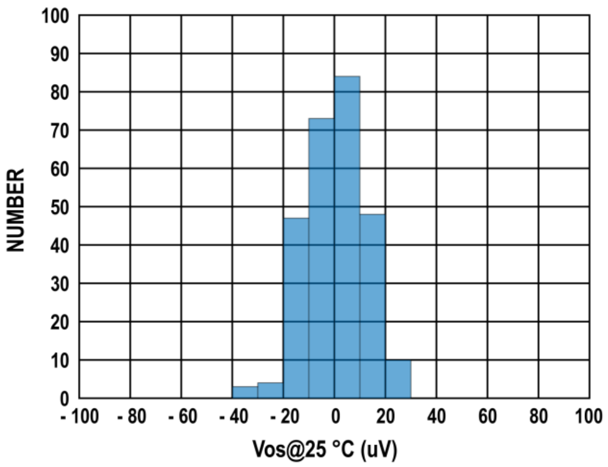


Figure 5. Input offset voltage histogram (B grade)

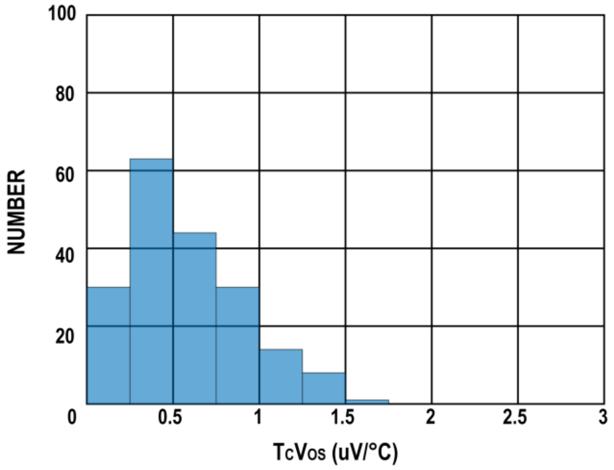


Figure 6. Temperature drift histogram (B grade)

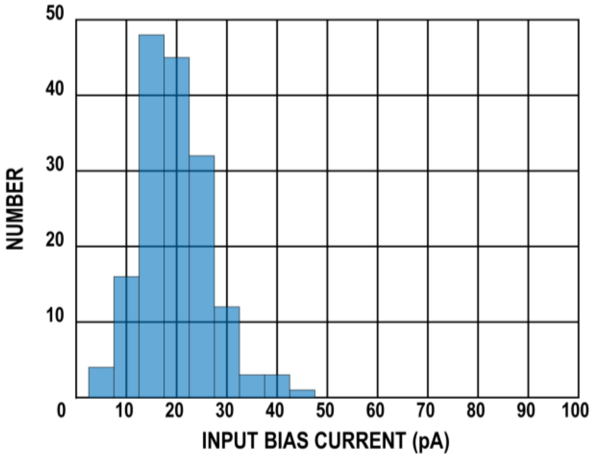


Figure 7. Input Bias Current @ 25 ° C

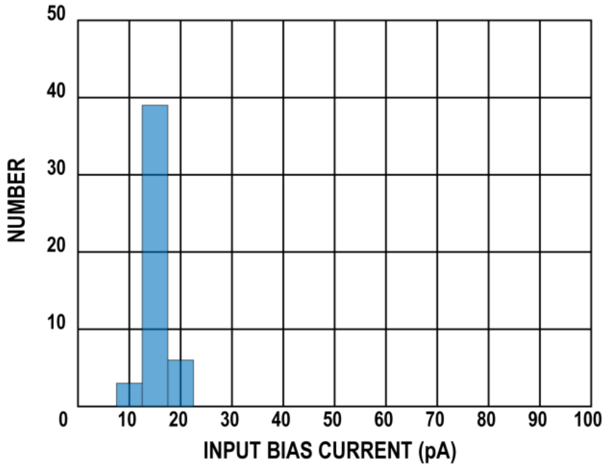


Figure 8. Input Bias Current @- 40 ° C

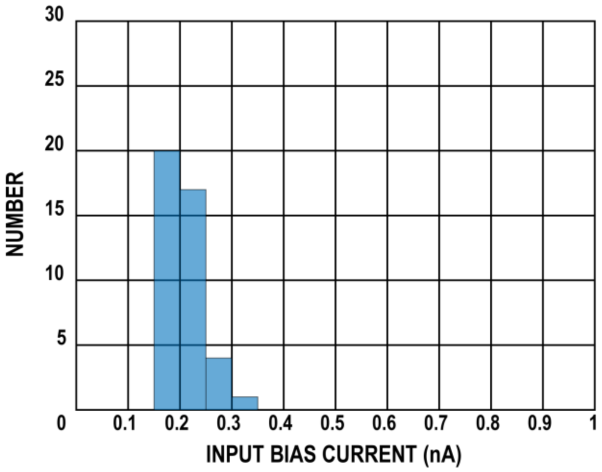


Figure 9. Input Bias Current @85 ° C

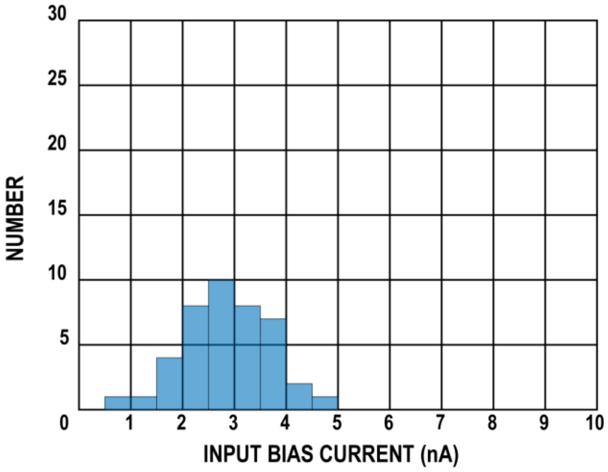


Figure 10. Input Bias Current @ 125 ° C

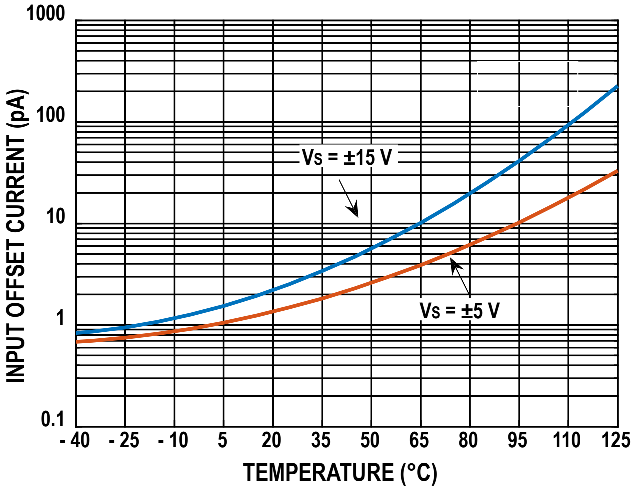


Figure 11. Input Offset Current vs. Temperature

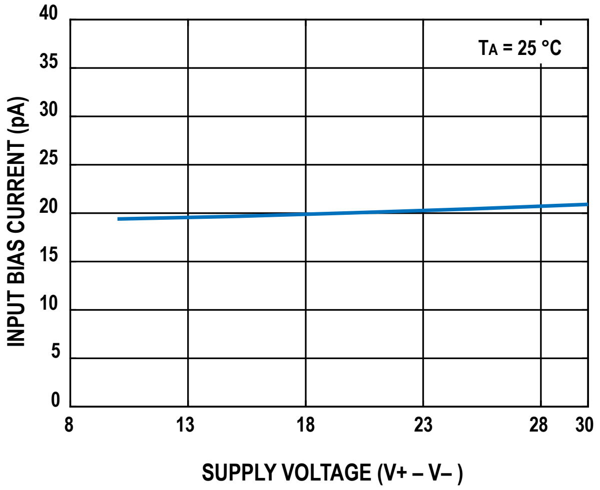


Figure 12. Input Bias Current vs. Supply Voltage

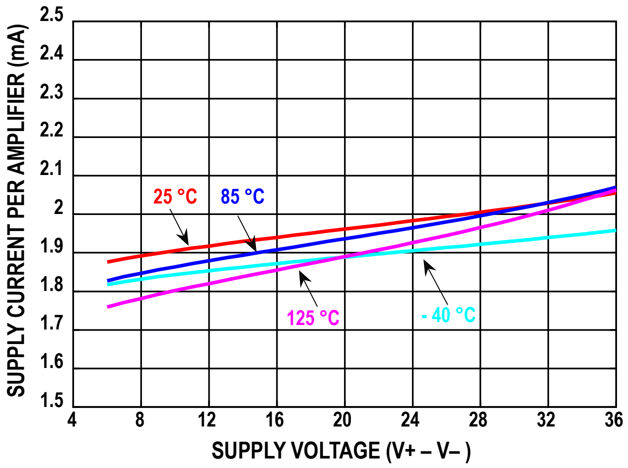


Figure 13. Supply Current vs. Supply Voltage per Amplifier

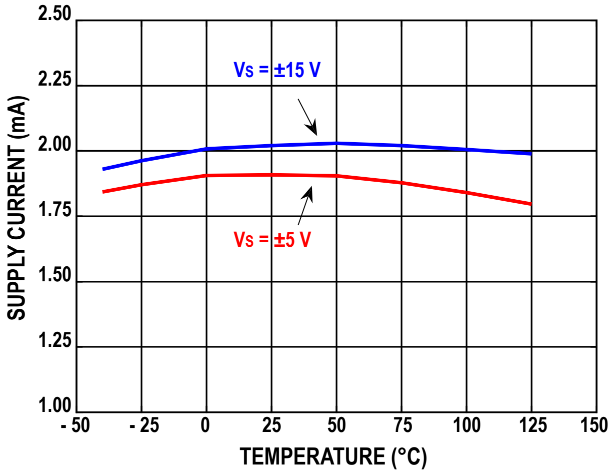


Figure 14. Supply Current vs. Temperature per Amplifier

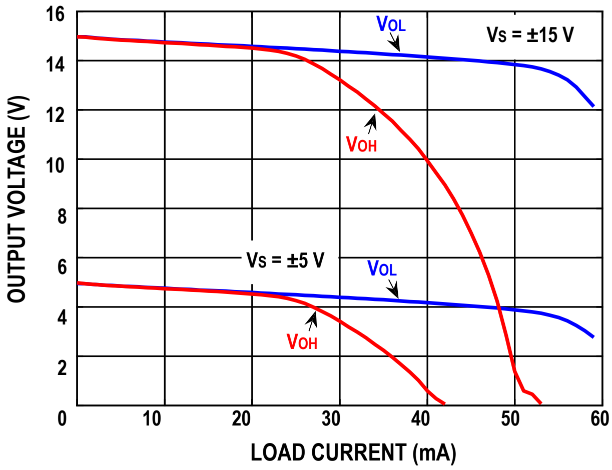


Figure 15. Output Voltage vs. Load Current

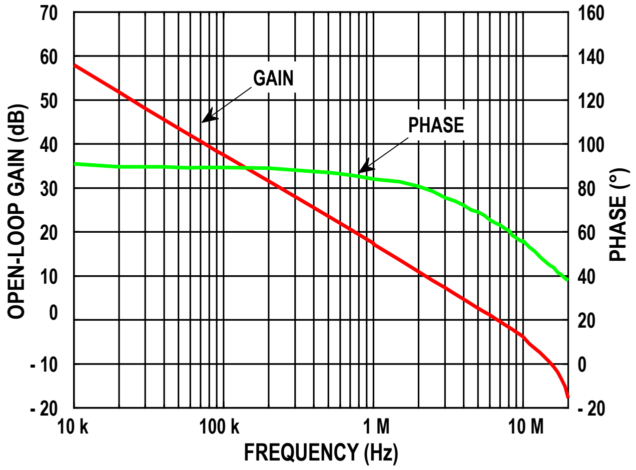


Figure 16. Open-Loop Gain vs. Frequency

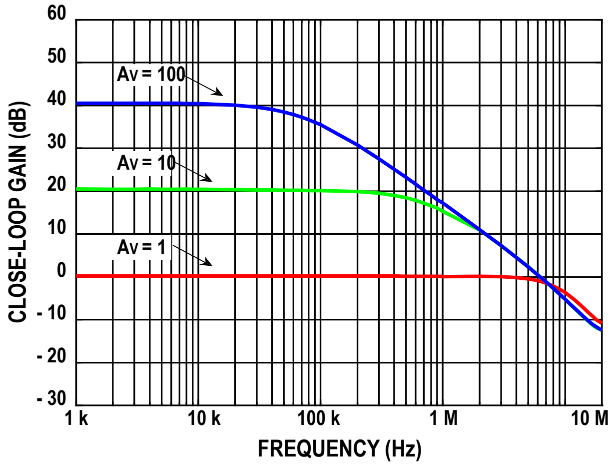


Figure 17. Close-Loop Gain vs. Frequency

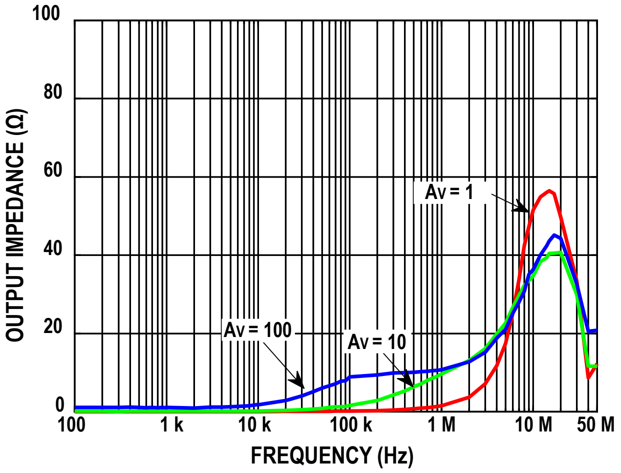


Figure 18. Output Impedance vs. Frequency

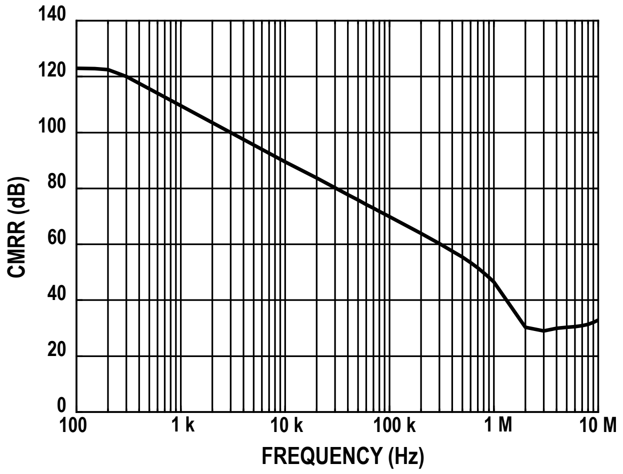


Figure 19. CMRR vs. Frequency

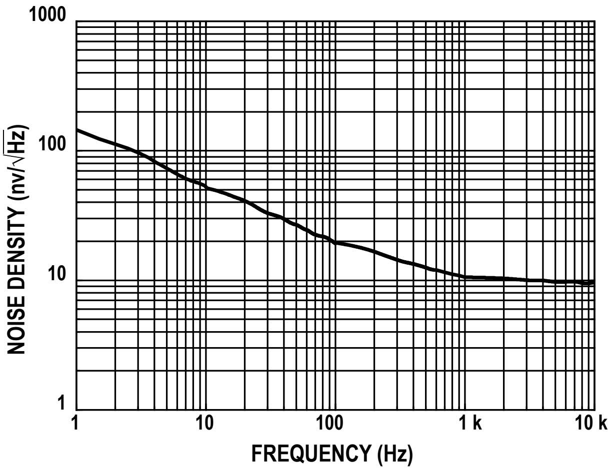


Figure 20. Voltage Noise Density vs. Frequency

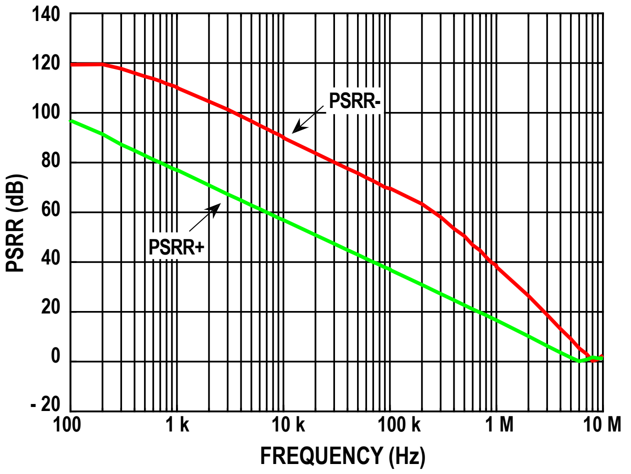


Figure 21. PSRR vs. Frequency

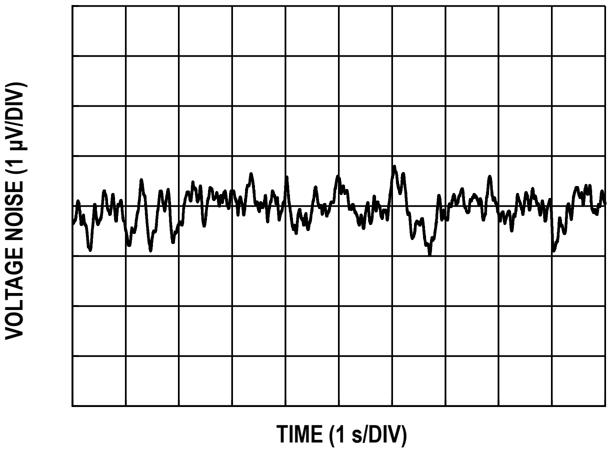


Figure 22. 0.1 Hz to 10 Hz Input Voltage Noise

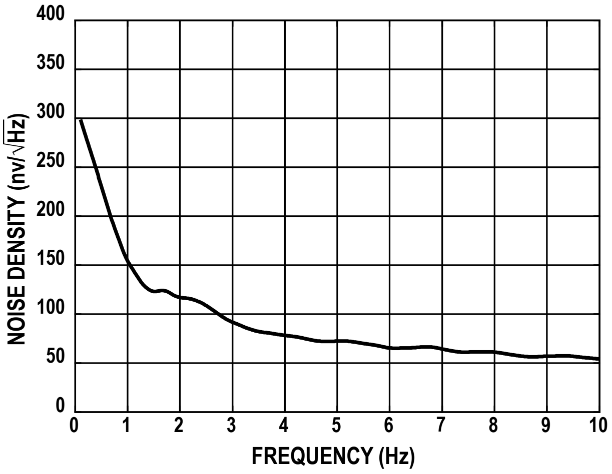


Figure 23. Voltage Noise Density vs. Frequency

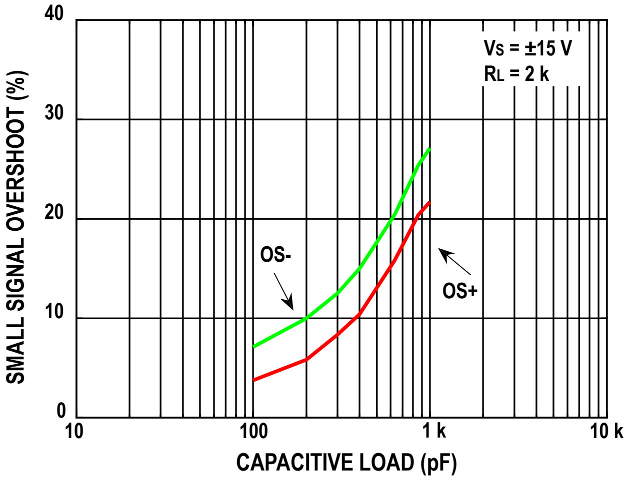


Figure 24. Small Signal Overshoot vs. Load Capacitance

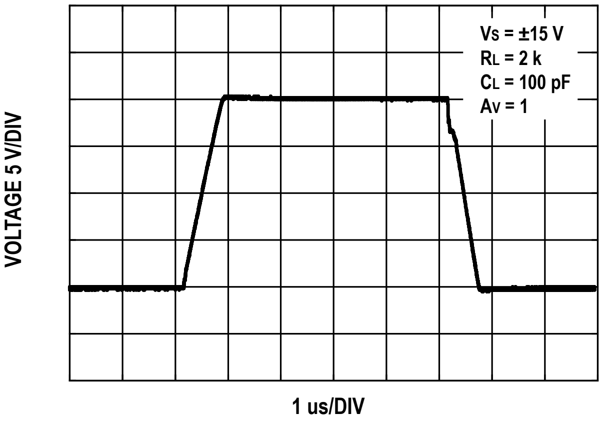


Figure 25. Large Signal Transient Response

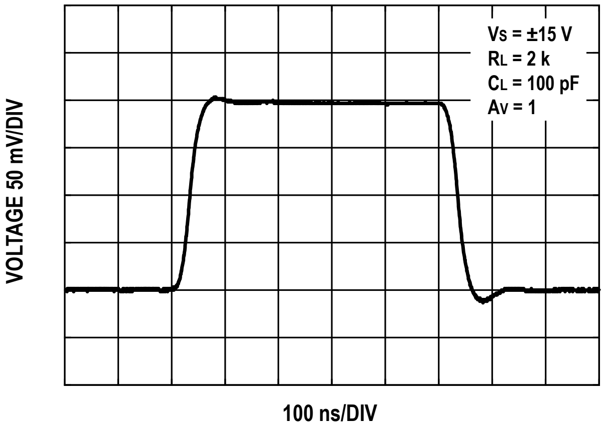


Figure 26. Small Signal Transient Response

General Application Information

Output Phase Reversal

Phase reversal is a change of polarity in the transfer function of the amplifier. This can occur when the voltage applied at the input of an amplifier exceeds the maximum common-mode voltage. Phase reversal can cause permanent damage to the device and may result in system lockups. The ZJA3512-2 and ZJA3512-4 do not exhibit phase reversal when input voltages are beyond the supplies.

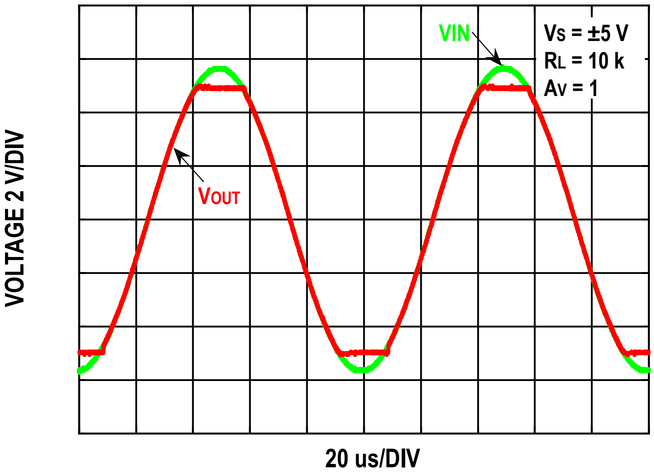


Figure 27. No phase reversal

THD + Noise

ZJA3512 features low total harmonic distortion (THD) and excellent gain linearity, making these amplifiers a great choice for precision circuits with high closed-loop gain and for audio application circuits. Figure 28 demonstrates that when configured with positive unity gain (the worst case) and driving a 100 kΩ load, the total distortion and noise of ZJA3512 is approximately 0.0003 %.

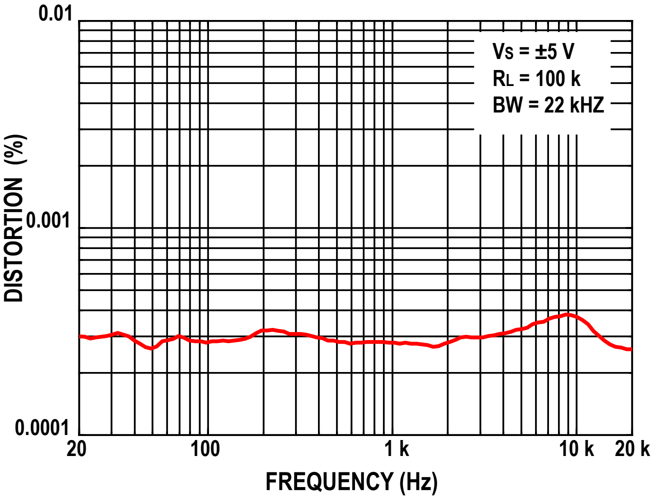


Figure 28. THD+N vs. Frequency

Total Noise Including Source Resistors

The low input current noise and input bias current of the ZJA3512 make it the ideal amplifier for circuits with substantial input source resistance. Input offset voltage increases by less than 15nV per 500 Ω of source resistance at room temperature. The total noise density of the circuit is

$$e_{nTOTAL} = \sqrt{e_n^2 + (i_n R_s)^2 + 4kTR_s}$$

Where:

e_n is the input voltage noise density of the parts.
i_n is the input current noise density of the parts.
R_S is the source resistance at the noninverting terminal.
K is Boltzman's constant (1.38×10^{-23} J/K).
T is the ambient temperature in Kelvin (T = 273 + °C).

For $R_S < 3.9$ kΩ, e_n dominates and $e_{nTOTAL} \approx e_n$.

The current noise of the ZJA3512 is so low that its contribution does not become a significant term unless R_S is greater than 165 MΩ, an impractical value for most applications.

The total equivalent rms noise over a specific bandwidth is expressed as:

$$e_{nTOTAL} = e_{nTOTAL}\sqrt{BW}$$

Where BW is the bandwidth in Hertz.

Note that the above analysis is valid for frequencies larger than 300 Hz and assumes flat noise above 10 kHz. For lower frequencies, flicker noise (1/f) must be considered.

Settling Time

Settling time is the time required for the amplifier output to reach a stable state and remain within a percentage of its step value. The pulse has been applied to the input terminal. Thanks to its impressive slew rate of 35 V/us, ZJA3512 settles to within 0.01 % in less than 560 ns, for a 10 V step in positive unity gain. This makes it an excellent choice as a buffer at the output of DACs whose settling time is typically less than 1 μs.

In addition to fast settling time and fast slew rate, the low offset voltage drift and input offset current of ZJA3512 allows full accuracy of a 16-bit converter over the entire operating temperature range.

Overload Recovery Time

Overload recovery, also known as overspeed recovery, refers to the time it takes the output of an amplifier to recover from a saturated condition to its linear region. This recovery time is particularly long, which is crucial for the application of amplifiers that must promptly response to small signal in the presence of excessive large transient. Figure 29 shows the positive overload recovery of ZJA3512. The output recovers from saturation within approximately 440 ns.

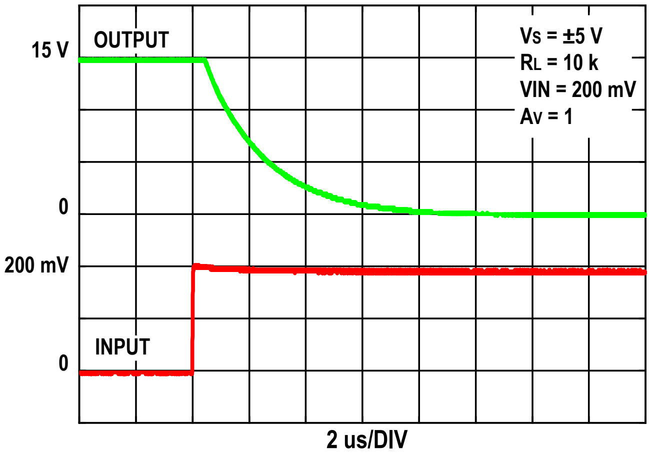


Figure 29. Positive Overload Recovery

The negative overdrive recovery time is also approximately 440 ns as shown in Figure 30. In addition to the fast recovery time, ZJA3512 show excellent positive and negative recovery time symmetry. This is an important feature of transient signal rectification, as the output signal is kept equally undistorted throughout any given period.

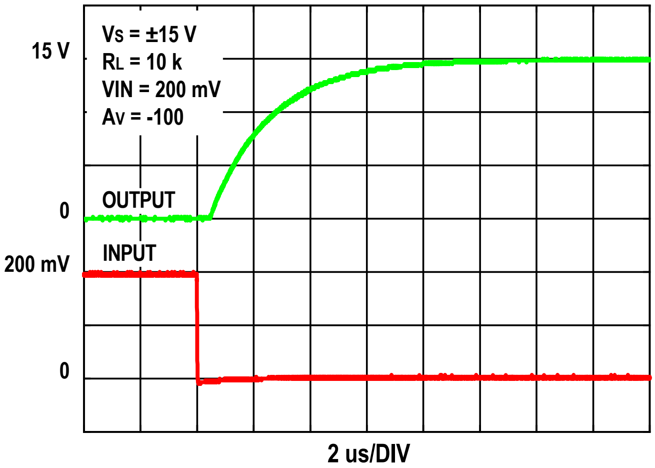


Figure 30. Negative Overload Recovery

Capacitive Load Drive

ZJA3512 is unconditionally stable under all gains in both inverted and non-inverting configurations. It is capable of driving up to 1000 pF capacitive load, without oscillation under positive unity gain configuration (worst case configuration). However, as with most amplifiers, driving larger capacitive loads in a unity gain configuration may cause excessive overshoot and/or ringing, or even oscillation. A simple snubber network reduces the amount of overshoot and ringing significantly. The advantage of this configuration is that the output swing of the amplifier will not decrease, as R_S is located outside the feedback loop.

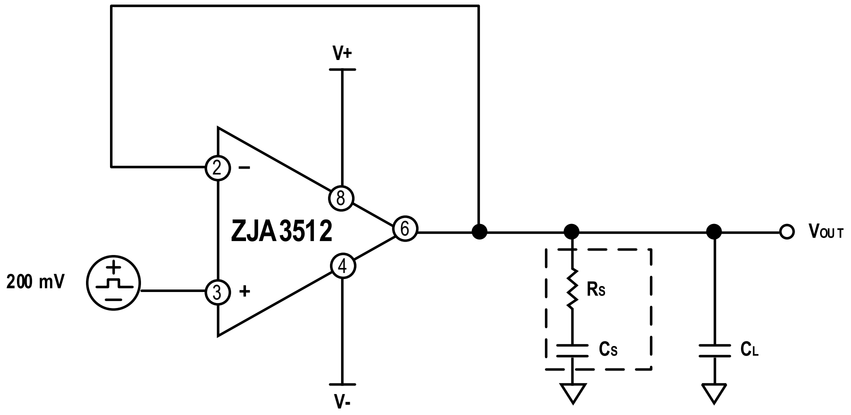


Figure 31. Snubber Network Configuration

Figure 32 shows a scope plot of the output of ZJA3512 in response to a 400 mV pulse. The circuit is configured as unity gain (worst case), with a load capacitance of 500 pF, and no ringing is observed at the output. As a comparison, one popular JFET amplifier from competitor demonstrates excessive ringing under the same condition, as shown in Figure 33. This confirms the outstanding stability margin of ZJA3512.

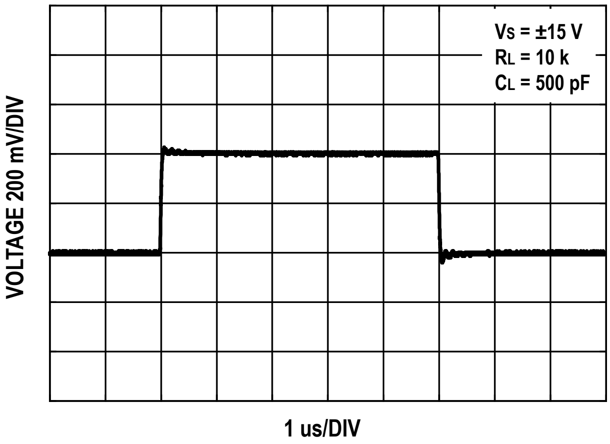


Figure 32. ZJA3512 Directly Driving Large Capacitive Load

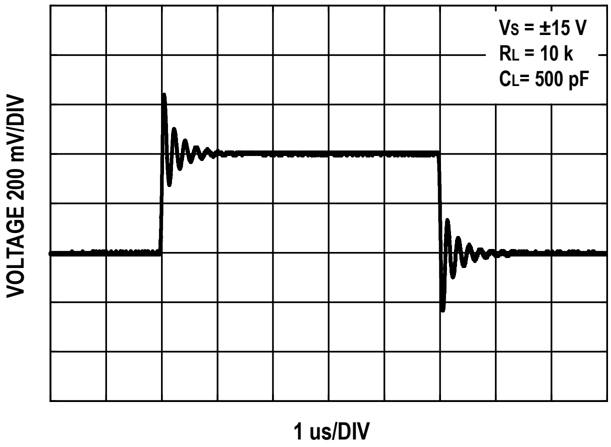


Figure 33. Competitor JFET Amplifier Driving Capacitive Load

However, further increase of capacitive load eventually undermines stability and leads to ringing as shown in Figure 34 for Cload of 1 nF. By adding a simple snubber network, it is able to eliminate the ringing as displayed in Figure 35.

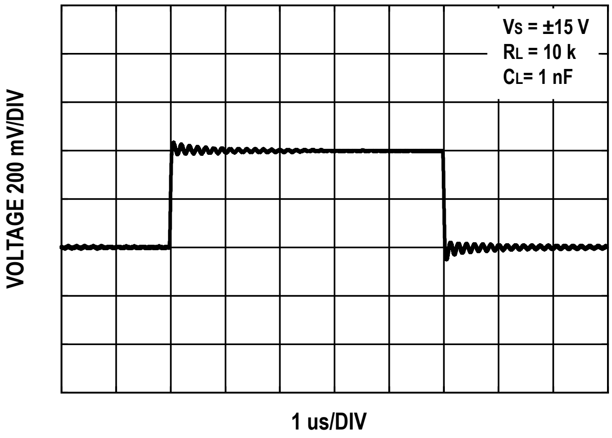


Figure 34. Direct Capacitive Load Drive of 1 nF

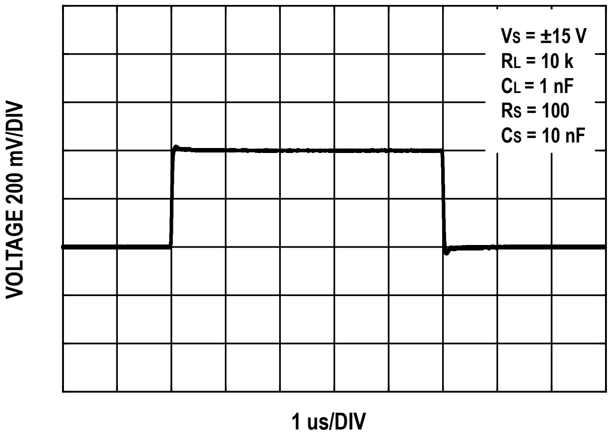


Figure 35. Capacitive Load Drive of 1 nF with Snubber

The optimal values of R_S and C_S depend on the load capacitance and input capacitance of ZJA3512, which is summarized in Table 1.

C_{LOAD}	R_S (Ω)	C_S
1 nF	100	10 nF
2 nF	50	10 nF
5 nF	20	10 nF

Table 1 Optimum Values for Capacitive Loads

Open-Loop Gain and Phase Response

In addition to impressive low noise, low offset voltage and offset current, ZJA3512 has excellent loop gain and phase response even when driving heavy resistive or capacitive load. Compare them to competitor JFET amplifier mentioned above in Figure 36 and Figure 37. When the output is loaded with 2.5 kΩ resistor, ZJA3512 has unity gain frequency of 7 MHz and a phase margin of 63 ° while the competitor 8MHz and 52°. Although the competitor is of higher bandwidth, ZJA3512 is much more stable, showing much less peaking in transient response and thus much faster settling time.

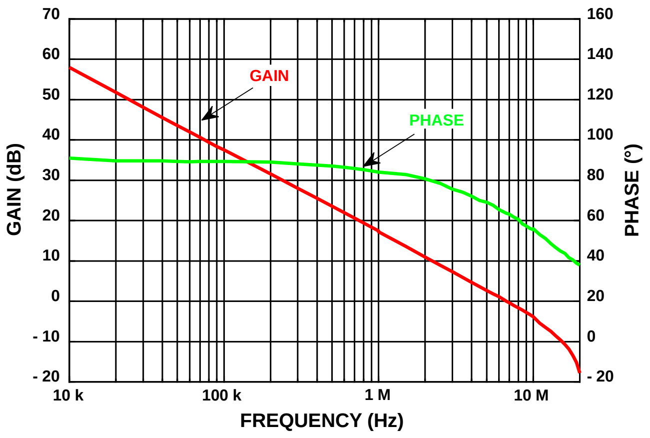


Figure 36. Frequency Response of ZJA3512

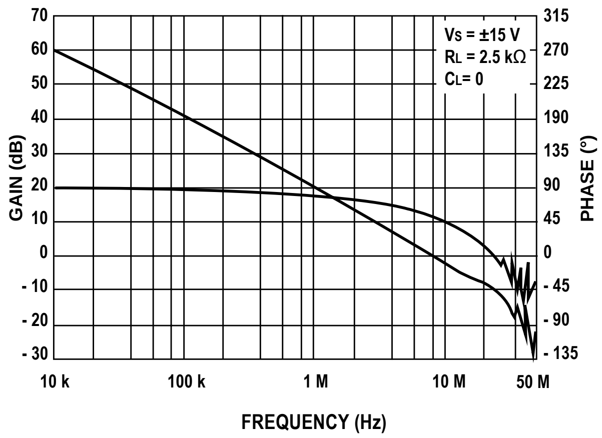


Figure 37. Frequency Response of Competitor JFET Amplifier

I-V Conversion Applications

Photodiode Circuits

Common applications for I-V conversion include photodiode circuits, where the amplifier is used to convert a current, generated by a photo diode placed at the inverting input terminal, into an output voltage.

ZJA3512's low input bias current, wide bandwidth, and low noise make it an excellent choice for various photodiode applications, including fiber optic controls, motion sensors, and bar code readers.

The circuit shown in Figure 38 uses a silicon diode with zero bias voltage. This is known as a Photovoltaic Mode; this configuration limits the overall noise and is suitable for instrumentation applications.

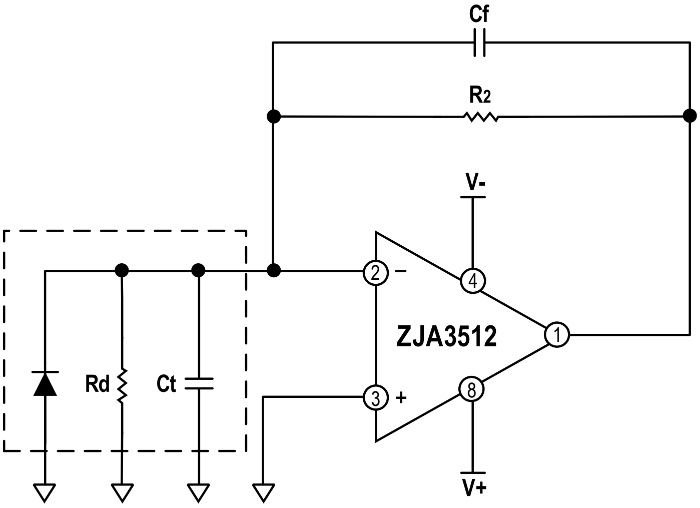


Figure 38. Equivalent Preamplifier Photodiode Circuit

A larger signal bandwidth can be attained at the expense of additional output noise. The total input capacitance (Ct) consists of the sum of the diode capacitance (typically 3 pF to 4 pF) and the amplifier's input capacitance (12 pF), which includes external parasitic capacitance. Ct creates a pole in the frequency response, which may lead to an unstable system. To ensure stability and optimize the bandwidth of the signal, a capacitor is placed in the feedback loop of the circuit shown in Figure 38 It creates a zero and yields a bandwidth whose corner frequency is $1/(2\pi (R_2Cf))$.

The value of R_2 can be determined by the ratio V/I_D, where V is the desired output voltage of the op amp and I_D is the diode current. For example, if I_D is 100 µA and a 10 V output voltage is desired, R_2 should be 100 kΩ. Rd is a junction resistance that drops typically by a factor of 2 for every 10°C increase in temperature. A typical value for Rd is 1000 MΩ. Since Rd >> R_2, the circuit behavior is not impacted by the effect of the junction resistance. The maximum signal bandwidth is

$$f_{MAX} = \sqrt{\frac{ft}{2\pi R_2 Ct}}$$

where f_t is the unity gain frequency of the amplifier.

Using the parameters above, Cf ≈ 1 pF, which yields a signal bandwidth of about 2.6 MHz.

$$Cf = \sqrt{\frac{Ct}{2\pi R_2 ft}}$$

where ft is the unity gain frequency of the op amp, achieves a phase margin, Φm, of approximately 45°.

A higher phase margin can be obtained by increasing the value of Cf. Setting Cf to twice the previous value yields approximately Φ_m = 65° and a maximally flat frequency response, but reduces the maximum signal bandwidth by 50 %.

Crosstalk

Crosstalk, also known as channel separation, measures the signal feedthrough from one channel to another. The channel separation of ZJA3512 is better than -100 dB at frequencies below 10 kHz, and higher than -55 dB at frequencies above 10 MHz. Figure 39 shows the typical channel separation behavior between the two amplifiers in ZJA3512-2.

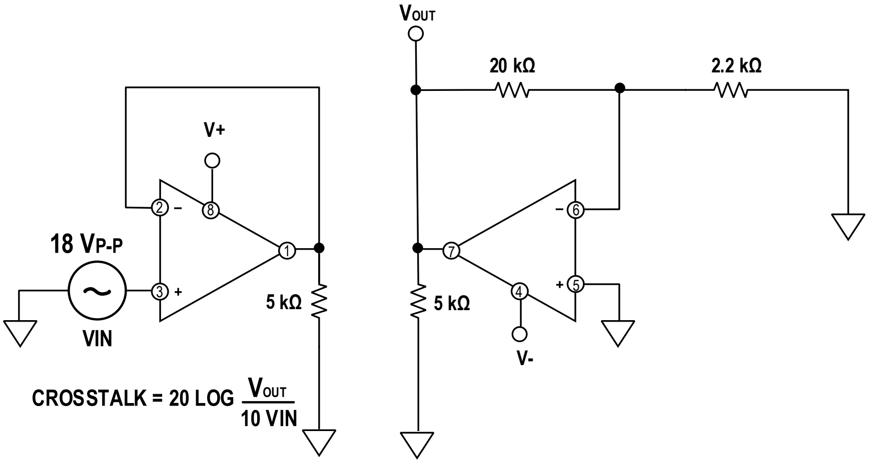


Figure 39. Crosstalk Test Circuit

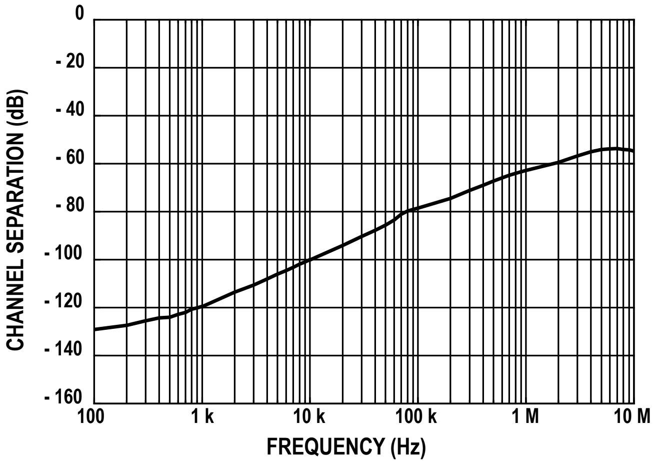


Figure 40. Dual Channel Crosstalk

Layout Guidance

For optimized performances of the device, good PCB layout practices are recommended, including:

- Noise may be conducted into the analog circuit through the op amp supply pins, using the low ESR 0.1 μF ceramic capacitor as decoupling capacitor. Put it as close as possible to the power pin can effectively reduce the noise caused by the power supplies.
- Normally input trace is more sensitive, keep the trace as short as possible. In order to reduce the noise of parasitic coupling, keep the input signals far from the power supply and/or outputs. If this is not possible, the sensitive traces should be perpendicular to others, so that the noise coupled through the parasitic capacitance can be as small as possible.
- If the it is high impedance signal source, it is necessary to design a guard ring. Guard rings can significantly reduce leakage currents from nearby traces that are at different potentials.
- Place the peripheral components as close as possible to the pins of the op amp, such as placing R_F, C_F and R_G. And delete the PCB ground plane below the inverting input to minimize parasitic capacitance.
- For best leakage performance, it is recommended to clean the PCBA after soldering and baking at 85°C for 30 minutes to remove any potential moisture from the package.
- In addition, separate grounding of the analog and digital parts of the circuit is one of the simplest and most effective noise suppression methods. When designing the PCB, plan the layout of the ground current return paths of the analog and digital parts so that the ground current return paths do not interfere each other. Using one or more layers of the multi-layer PCB as the ground also helps to reduce the ground impedance and noise.

Outline Information

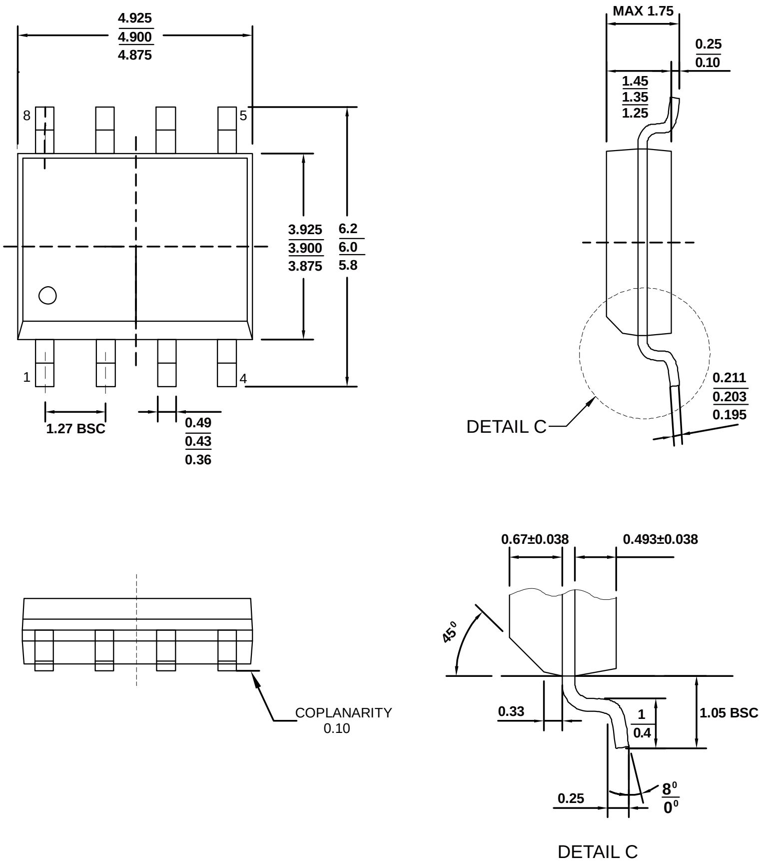


Figure 41. 8-Lead SOIC Package Dimensions shown in millimeters

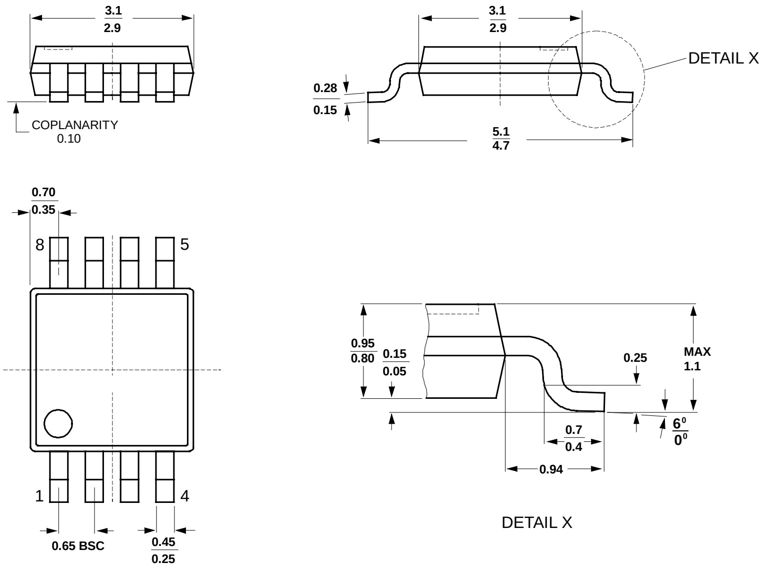


Figure 42. 8-Lead MSOP Package Dimensions shown in millimeters

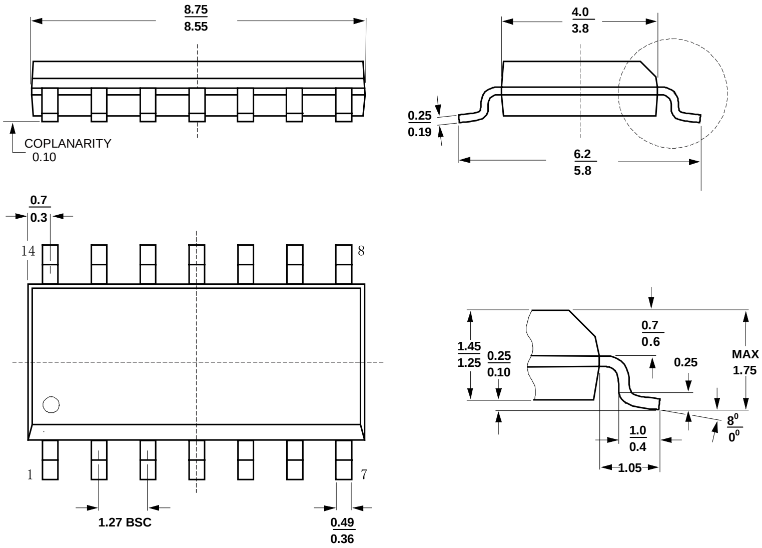
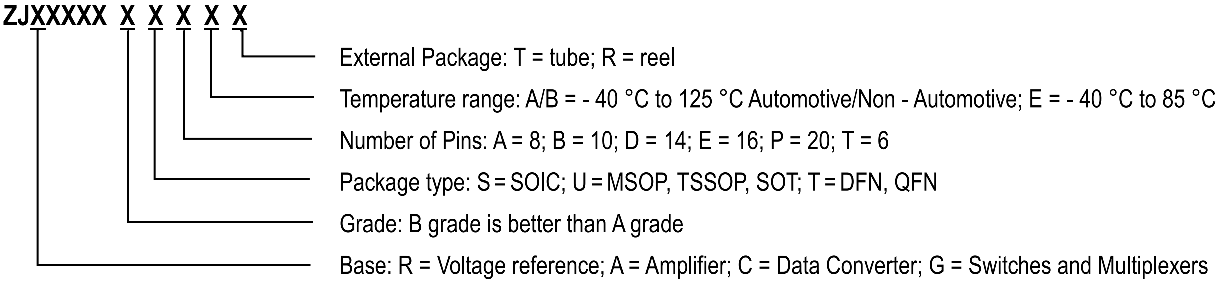


Figure 43. 14-Lead SOIC Package Dimensions shown in millimeters

Ordering Guide

Model	Channels	Pacakge	Orderable Device	Temperature Range (°C)	External Package
ZJA3512-2	2	SOIC-8	ZJA3512-2BSABT	- 40 to +125	Tube
		SOIC-8	ZJA3512-2BSABR	- 40 to +125	13” Reel
		SOIC-8	ZJA3512-2ASABT	- 40 to +125	Tube
		SOIC-8	ZJA3512-2ASABR	- 40 to +125	13” Reel
		MSOP-8	ZJA3512-2BUABT	- 40 to +125	Tube
		MSOP-8	ZJA3512-2BUABR	- 40 to +125	13” Reel
		MSOP-8	ZJA3512-2AUABT	- 40 to +125	Tube
		MSOP-8	ZJA3512-2AUABR	- 40 to +125	13” Reel
ZJA3512-4	4	SOIC-14	ZJA3512-4BSDBT	- 40 to +125	Tube
		SOIC-14	ZJA3512-4BSDBR	- 40 to +125	13” Reel
		SOIC-14	ZJA3512-4ASDBT	- 40 to +125	Tube
		SOIC-14	ZJA3512-4ASDBR	- 40 to +125	13” Reel

Product Order Model



External Package: T = tube; R = reel

Temperature range: A/B = - 40 °C to 125 °C Automotive/Non - Automotive; E = - 40 °C to 85 °C

Number of Pins: A = 8; B = 10; D = 14; E = 16; P = 20; T = 6

Package type: S = SOIC; U = MSOP, TSSOP, SOT; T = DFN, QFN

Grade: B grade is better than A grade

Base: R = Voltage reference; A = Amplifier; C = Data Converter; G = Switches and Multiplexers

Related Parts

Part Number	Description	Comments
ADC		
ZJC2000/2010	18-bit 400 kSPS/200 kSPS SAR ADC	Fully differential input, SINAD 99.3 dB, THD - 113 dB
ZJC2001/2011	16-bit 500 kSPS/250 kSPS SAR ADC	Fully differential input, SINAD 95.3 dB, THD - 113 dB
ZJC2002/2012 ZJC2003/2013	16-bit 500 kSPS/250 kSPS SAR ADC	Pseudo-differential unipolar input, SINAD 91.7 dB, THD - 105 dB Pseudo-differential bipolar input, SINAD 91.7 dB, THD - 105 dB
ZJC2004/2014 ZJC2005/2015	18-bit 400 kSPS/200 kSPS SAR ADC	Pseudo-differential unipolar input, SINAD 94.2 dB, THD - 105 dB Pseudo-differential bipolar input, SINAD 94.2 dB, THD - 105 dB
ZJC2007/2017 ZJC2008/2018	14-bit 600 kSPS/300 kSPS SAR ADC	Pseudo-differential unipolar input, SINAD 85 dB, THD - 105 dB Pseudo-differential bipolar input, SINAD 85 dB, THD - 105 dB
ZJC2100/1-18	18-bit 400 kSPS/200 kSPS 4-ch differential SAR ADC, SINAD 99.3 dB, THD - 113 dB	
ZJC2100/1-16	16-bit 500 kSPS/250 kSPS 4-ch differential SAR ADC, SINAD 95.3 dB, THD - 113 dB	
ZJC2102/3-18	18-bit 400 kSPS/200 kSPS 8-ch pseudo-differential SAR ADC, SINAD 94.2 dB, THD - 105 dB	
ZJC2102/3-16	16-bit 500 kSPS/250 kSPS 8-ch pseudo-differential SAR ADC, SINAD 91.7 dB, THD - 105 dB	
ZJC2102/3-14	14-bit 600 kSPS/300 kSPS 8-ch pseudo-differential SAR ADC, SINAD 85 dB, THD - 105 dB	
ZJC2104/5-18	18-bit 400 kSPS/200 kSPS 4-ch pseudo-differential SAR ADC, SINAD 94.2 dB, THD - 105 dB	
ZJC2104/5-16	16-bit 500 kSPS/250 kSPS 4-ch pseudo-differential SAR ADC, SINAD 91.7 dB, THD - 105 dB	
DAC		
ZJC2541-18/16/14 ZJC2543-18/16/14	18/16/14-bit 1 MSPS single channel DAC with unipolar output	Power on reset to 0 V (ZJC2541) or $V_{REF}/2$ (ZJC2543), 1 nV-S glitch, SOIC-8/MSOP-10/DFN-10 packages
ZJC2542-18/16/14 ZJC2544-18/16/14	18/16/14-bit 1 MSPS single channel DAC with bipolar output	Power on reset to 0 V (ZJC2542) or $V_{REF}/2$ (ZJC2544), 1 nV-S glitch, SOIC-14/TSSOP-16/QFN-16 packages
Amplifier		
ZJA3000-1/2/4	Single/Dual/Quad 36 V low bias current precision Op Amps	3 MHz GBW, 35 μV max Vos, 0.5 μV/°C max Vos drift, 25 pA max Ibias, 1 mA/Amplifier, input to V-, RRO, 4.5 V to 36 V
ZJA3001-1/2/4	Single/Dual/Quad 36 V low bias current precision Op Amps	3 MHz GBW, 35 μV max Vos, 0.5 μV/°C max Vos drift, 25 pA max Ibias, 1 mA/Amplifier, RRO, 4.5 V to 36 V
ZJA3512-2/4	Dual/Quad 36 V 7 MHz precision JFET Op Amps	7 MHz GBW, 35 V/μS SR, 50 μV max Vos, 1 μV/°C max Vos drift, 2 mA/Amplifier, RRO, 4.5V to 35 V
ZJA3600/1	36 V ultra-high precision in-amp	CMRR 105 dB min (G = 1), 25 pA max Ibias, 25 μV max Vosi, gain error 0.001 % max (G = 1), 625 kHz BW (G = 10), 3.3 mA/Amplifier, ± 2.4 V to ± 18 V, - 40 °C to 125 °C specified
ZJA3622/8	36 V low cost precision in-amp	CMRR 93 dB min (G = 10), 0.5 nA max Ibias, 125 μV max Vosi, 625 kHz BW (G = 10), 3.3 mA/Amplifier, ± 2.4 V to ± 18 V
ZJA3611, ZJA3609	36 V ultra-high precision wider bandwidth precision in-amp (min gain of 10)	CMRR 120 dB min (G = 10), 25 pA max Ibias, 25 μV max Vosi, 1.2 MHz BW (G = 10), 3.3 mA/Amplifier, ± 2.4 V to ± 18 V, - 40 °C to 125 °C specified
ZJA3676/7	Low power, G = 1 Single/Dual 36 V difference amplifier	Input protection to ± 65 V, CMRR 104 dB min, Vos 100 μV max, gain error 15 ppm max, 500 kHz BW, 330 μA, 2.7 to 36 V
Voltage Reference		
ZJR1000	15 V supply precision voltage reference	V_{OUT} = 1.25/2.048/2.5/3/4.096/5 V, 5 ppm/°C max drift - 40 °C to 125 °C, ± 0.05 % initial error
ZJR1001 ZJR1002 ZJR1003	5.5V low power voltage reference (ZJR1001 with noise filter option)	V_{OUT} = 2.5/3/4.096/5 V, 5 ppm/°C max drift - 40 °C to 125 °C, ± 0.05 % initial error, 130 μA, ZJR1001/2 in SOT23-6, ZJR1003 in SOIC/MS-8
Switches and Multiplexers		
ZJG4438/4439	36V fault protection 8:1/dual 4:1 multiplexer	Protection to ± 50 V power on & off, latch-up immune, Ron 270 Ω, 14.8 pC charge injection, t_{ON} 166 ns, 10 V to 36 V