## GENERAL DESCRIPTION

The LW82XX Series is a group of voltage regulators with high accuracy, high speed, low drop-out, reverse current protection, high ripple rejection and fast discharge function.

The series consists of a voltage reference, an error amplifier, a driver transistor, a current limiter, a thermal protection circuit, a reverse current protection circuit and a phase compensation circuit.

Output voltage is selectable from 0.8V to 5.0V which fixed by laser trimming technologies, Step=100mV.

The LW82XX Series is available in DFN2x2-6L, DFN3x3-8L, SOT23-5 and SOT89-5L packages.

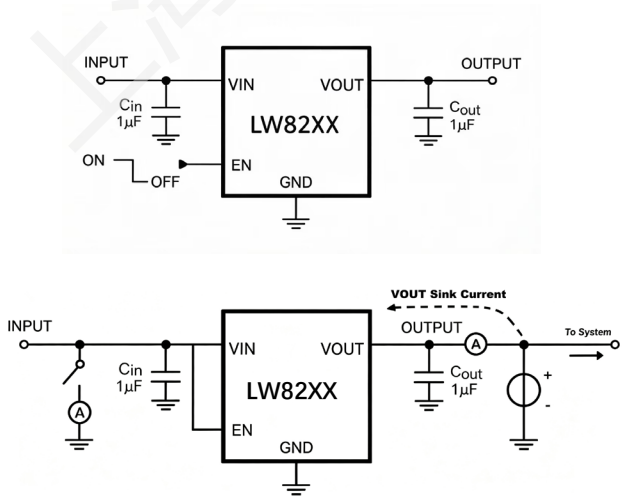
## FEATURES

- Low Quiescent Current: 28μA(Typ.)
- Operating Voltage Range: from 1.8V to 7.0V
- Output Voltage Range: from 0.8V to 5.0V
- Max Output Current: 1000mA
- Output Accuracy: ±1.0%@+25℃
- Low Dropout Voltage: 330mV@1000mA/3.3V
- High PSRR: 75dB@1kHz, 10mA
- Current Limiting Protection
- Output Short-Circuit Protection
- Over-Temperature Protection
- Fast Discharge Function
- Excellent Line and Load Transient Response
- Reverse Current Protection Function
- Stable with 1μF Output Capacitor

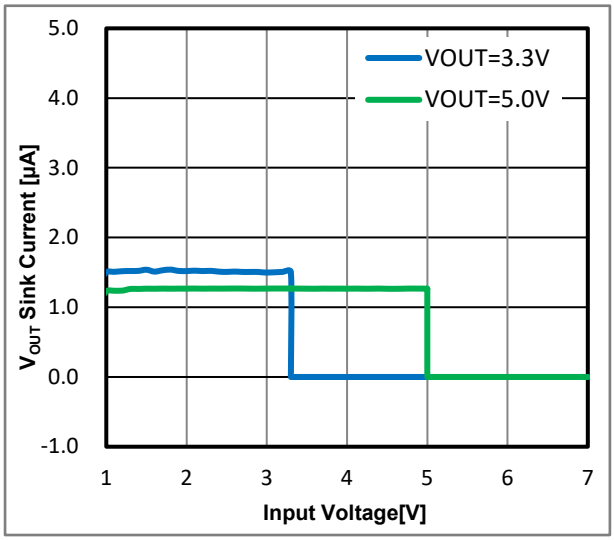
## APPLICATIONS

- Battery-Powered Devices
- Reference Voltage Sources
- USB products and HDMI Equipment
- Other Low Voltage Power Supplies

## TYPICAL APPLICATION CIRCUIT



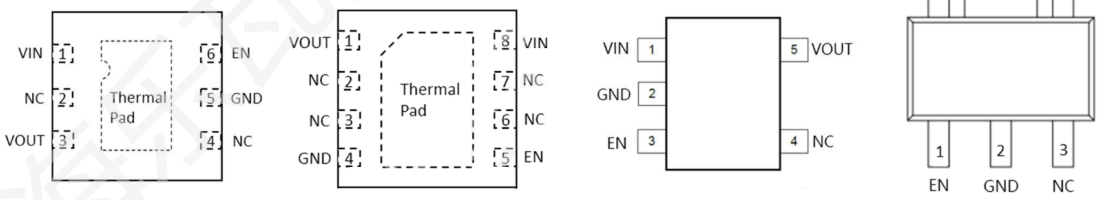

## TYPICAL PERFORMANCE CHARACTERISTICS



## PIN DESCRIPTION:

| PIN No. | | | | SYMBOL | DESCRIPTION |
|---|---|---|---|---|---|
| DFN2x2-6L | DFN3x3-8L | SOT23-5L | SOT89-5L | | |
| 1 | 8 | 1 | 4 | VIN | Input Voltage Pin. It is recommended to use a ceramic capacitor with a minimum effective capacitance of 1μF from $V_{IN}$ pin to ground. |
| 5 | 4 | 2 | 2, Tab | GND | Ground pin. |
| 6 | 5 | 3 | 1 | EN | Enable pin. Drive EN greater than $V_{ENH}$ to turn on the regulator. Drive EN less than $V_{ENL}$ to put the low-dropout regulator (LDO) into shutdown mode. |
| 2,4 | 2,3,6,7 | 4 | 3 | NC | Not Connection. Ground this pin for better thermal performance. |
| 3 | 1 | 5 | 5 | VOUT | Output Voltage Pin. It is recommended to use a ceramic capacitor with a minimum effective capacitance of 1μF from $V_{OUT}$ pin to ground. |
| Thermal pad | | -- | -- | Pad | The thermal pad is electrically connected to the GND node. Connect to the GND plane for improved thermal performance. |

## PIN ASSIGNMENT:



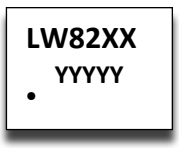

DFN2x2-6L(Type-A) DFN3x3-8L SOT23-5L SOT89-5L

## MARK INFORMATION:

**DFN2X2-6L/DFN3X3-8L**

**XX: VOLTAGE**

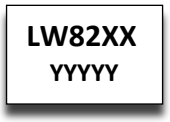
**YY: DATE CODE**




**SOT23-5L**

**XX: VOLTAGE**

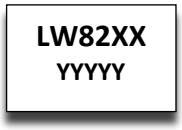
**YY: DATE CODE**




**SOT89-5L**

**X: VOLTAGE**

**YY: DATE CODE**



## ABSOLUTE MAXIMUM RATINGS (1):

($T_A$ =25℃, unless otherwise specified.)

| SYMBOL | ITEM | | RATING | UNIT |
|---|---|---|---|---|
| $V_{IN}$ | Supply Voltage | | -0.3~8.0 | V |
| $V_{EN}$ | EN Pin Voltage | | -0.3~8.0 | V |
| $V_{OUT}$ | $V_{OUT}$ pin Voltage | | -0.3~ ($V_{IN}$+0.3) | V |
| $V_{(ESD)}$ | ESD Susceptibility, HBM(2) | | ±4000 | V |
| $R_{\theta JA}$ | Junction-to-ambient Thermal Resistance (3) | DFN2x2-6L | 80 | ℃/W |
| | | DFN3x3-8L | 52 | |
| | | SOT23-5L | 210 | |
| | | SOT89-5L | 76 | |
| $T_J$ | Junction Temperature Range | | -40~150 | ℃ |
| $T_{STG}$ | Storage Temperature Range | | -40~150 | ℃ |
| $T_{SOLDER}$ | Lead Temperature (Soldering) | | 260℃, 10s | |

**Note:**

1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability

2. per ANSI/ESDA/JEDEC JS-001

3. Device mounted on FR-4 PCB, Refer to JESD51-3 for detailed information on the board construction.

## RECOMMENDED OPERATING RANGE:

| SYMBOL | ITEM | VALUE | UNIT |
|---|---|---|---|
| $V_{IN}$ | $V_{IN}$ Supply Voltage | 1.8~7.0 | V |
| $V_{EN}$ | EN Pin Voltage | 0~7.0 | V |
| $V_{OUT}$ | $V_{OUT}$ Pin Voltage | 0.8~5.0 | V |
| $I_{OUT}$ | Output Current | 0~1.0 | A |
| $T_J$ | Junction Temperature Range | -40~125 | ℃ |

## ELECTRICAL CHARACTERISTICS:

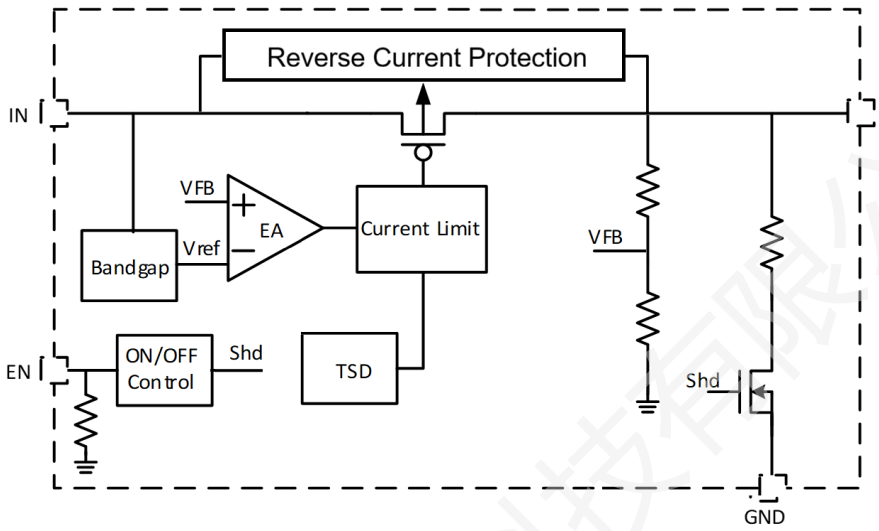
$V_{IN}$=$V_{OUT(NOM)}$+1V or +2V, whichever is greater, $C_{IN}$= $C_{OUT}$=1μF, unless otherwise specified, typical values are at $T_A$= 25°C.

| Symbol | Parameter | Conditions | | MIN | TYP | MAX | Units |
|---|---|---|---|---|---|---|---|
| $V_{IN}$ | Input Voltage | | | 1.8 | | 7.0 | V |
| $V_{OUT}$ | Output Accuracy | $I_{OUT}$=1mA | | -1.0 | | 1.0 | % |
| $I_{LIM}$ | Current Limit(1) | | | 1.1 | 1.45 | | A |
| $I_Q$ | Quiescent Current | $V_{IN}$=$V_{EN}$=$V_{OUT}$+1V, No Load | | | 28 | 45 | μA |
| $I_{SHD}$ | Shutdown Current | $V_{IN}$=7.0V, $V_{EN}$=0V | | | | 0.1 | μA |
| $V_{DROP}$ | Dropout Voltage(1) (2) | $V_{OUT}$=3.3V | $I_{OUT}$=300mA | | 95 | | mV |
| | | | $I_{OUT}$=500mA | | 160 | | |
| | | | $I_{OUT}$=1000mA | | 330 | | |
| | | $V_{OUT}$=5.0V | $I_{OUT}$=300mA | | 75 | | |
| | | | $I_{OUT}$=500mA | | 120 | | |
| | | | $I_{OUT}$=1000mA | | 250 | | |
| $\Delta V_{OUT}$/ ($\Delta V_{IN}$*$V_{OUT(NOM)}$) | Line Regulation | $V_{IN}$= $V_{OUT}$ +1V to 7.0V, $I_{OUT}$=1mA | | | 0.05 | 0.2 | %/V |
| $\Delta V_{OUT}$ | Load Regulation | 1mA≤$I_{OUT}$≤1000mA | | | 10 | 60 | mV |
| $I_{SHORT}$ | Short Current(1) | $V_{OUT}$=0V | | | 100 | | mA |
| $V_{ENH}$ | EN High Voltage | $V_{IN}$=1.8V to 7.0V, $I_{OUT}$=1mA | | 1.5 | | | V |
| $V_{ENL}$ | EN Low Voltage | | | | | 0.5 | V |
| $T_{STR}$ | Startup Time | From $V_{EN}$ 'L'→'H' to 95%*$V_{OUT}$, $C_{OUT}$=1μF, No Load | | | 50 | | μs |
| PSRR | Power Supply Rejection Ratio | $V_{IN}$= 4.3V, $V_{OUT}$=3.3V, $V_{PP}$=0.5V, $I_{OUT}$=10mA, $C_{IN}$=0.22μF, $C_{OUT}$=1μF | f=217Hz | | 74 | | dB |
| | | | f=1kHz | | 75 | | |
| | | | f=10kHz | | 70 | | |
| $e_n$ | Output Voltage Noise | $V_{IN}$= 4.3V, $V_{OUT}$=3.3V, f=10Hz to 100kHz | $I_{OUT}$=0mA | | 21 | | $\mu V_{RMS}$ |
| | | | $I_{OUT}$=10mA | | 31 | | |
| $I_{REV}$ | Reverse Current(3) | $V_{EN}$=$V_{IN}$=0V, $V_{OUT}$=7.0V | | | 0.01 | 0.5 | μA |
| $I_{REVS}$ | $V_{OUT}$ Pin Sink Current(4) | $V_{EN}$=$V_{IN}$=6.0V, $V_{OUT}$=7.0V | | | 1.5 | 2.5 | μA |
| $T_{SD}$ | Thermal Shutdown | Temperature rising | | | 160 | | °C |
| $\Delta T_{SD}$ | TSD Hysteresis | Temperature falling | | | 20 | | °C |
| $R_{DISCHRG}$ | Output Discharge Resistance | $V_{IN}$= 7.0V, $V_{EN}$=0V | | | 80 | | Ω |

**NOTES:**

1. Guaranteed by design
2. The dropout voltage is defined as $V_{IN}$ - $V_{OUT}$, when $V_{OUT}$ =95%*$V_{OUT(NOM)}$
3. Reverse Current ($I_{REV}$) flows from $V_{OUT}$ to $V_{IN}$
4. $V_{OUT}$ Pin Sink Current ($I_{REVS}$) flows from $V_{OUT}$ to GND

## SIMPLIFIED BLOCK DIAGRAM:




## DETAIL OPERATION DESCRIPTION:

The LW82XX Series is a low noise, high PSRR, low drop-out voltage regulator. It consists of a current limiter circuit, a driver transistor, a precision voltage reference, a thermal protection circuit, a reverse current protection circuit and an error correction circuit, and is compatible with low ESR ceramic capacitors. The current limiter's fold-back circuit operates as a short circuit protection as well as the output current limiter.

### *Reverse Current Protection*

The LW82XX series includes reverse current protection to prevent the damage as a result of current flow from $V_{OUT}$ pin to the $V_{IN}$ pin when the power supply is connected to the $V_{OUT}$ pin. When $V_{IN}$ is smaller than $V_{OUT}$, the reverse current protection works and suppress the reverse current to 0.5μA (MAX.). When $V_{IN}$ is smaller than $V_{OUT}$, the $V_{OUT}$ pin sink current flowing from the $V_{OUT}$ pin to the GND pin is 1.5μA (TYP.) as the IC operation current. Please also note when an external power supply is connected to the $V_{OUT}$ pin, please use it within 7.0V.

### *Current Limiting and Short-Circuit Protection*

The current limit circuitry prevents damage to the MOSFET switch can deliver load current up to the current limit threshold through the switch. When a heavy load or short circuit is applied to an enabled switch, a large transient current may flow until the current limit circuitry responds. Once this current limit threshold is exceeded the device enters constant current mode until the thermal shutdown occurs or the fault is removed.

### *Thermal Shutdown*

When the junction temperature of the built-in driver transistor reaches the temperature limit level (160°C TYP.), the thermal shutdown circuit operates and the driver transistor will be turned OFF. The IC resumes its operation when the thermal shutdown function is released and the IC's operation is automatically restored because the junction temperature drops to the level of 140°C (TYP.) as the thermal shutdown release threshold.

### *Chip Enable*

The LW82XX series can be turned off via the EN pin signal. In shutdown mode, output at the $V_{OUT}$ pin will be pulled down to the GND.

The LW82XX series has a pull-down resistor in order to operate normally even the EN pin is floating.

If the EN pin voltage is set with the specified voltage range, the logic is fixed and the IC will operate normally.

## TYPICAL OPERATING CHARACTERISTICS:

(Tested under $T_A$ =25°C,$C_{IN}$= $C_{OUT}$=1μF, unless otherwise specified)

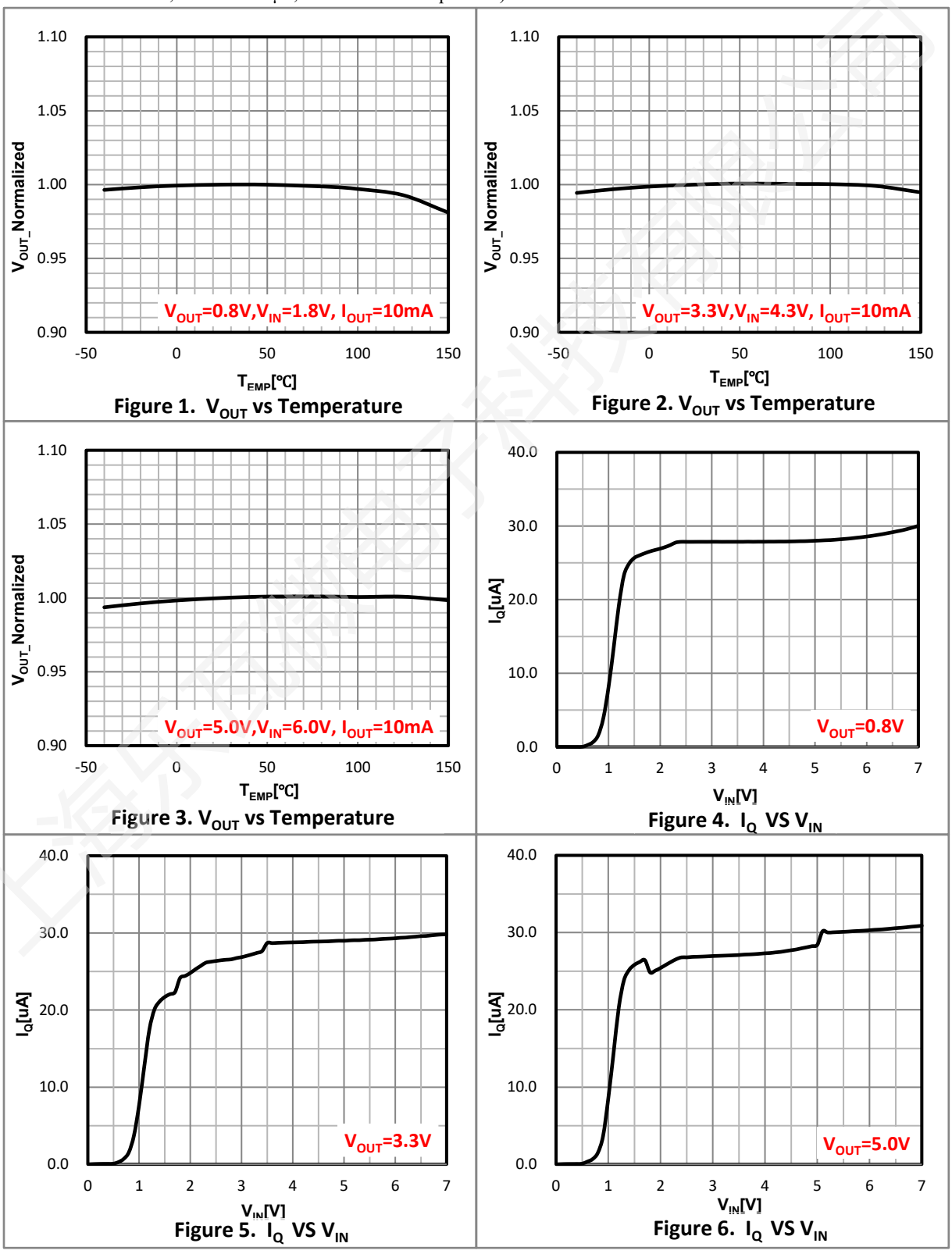



Figure 1. $V_{OUT}$ vs Temperature

Figure 2. $V_{OUT}$ vs Temperature

Figure 3. $V_{OUT}$ vs Temperature

Figure 4. $I_Q$ VS $V_{IN}$

Figure 5. $I_Q$ VS $V_{IN}$

Figure 6. $I_Q$ VS $V_{IN}$

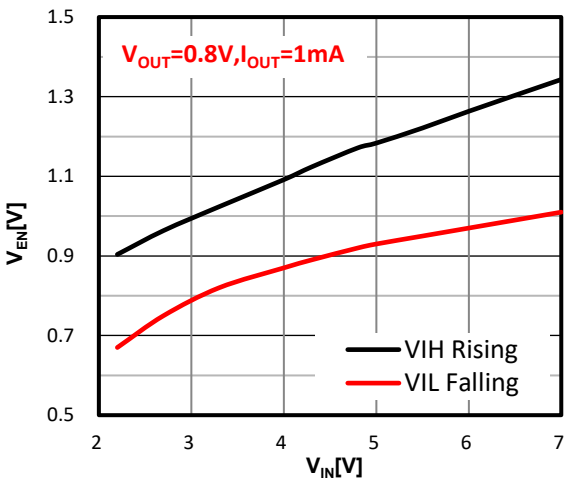


Figure 7. $V_{EN}$ vs $V_{IN}$

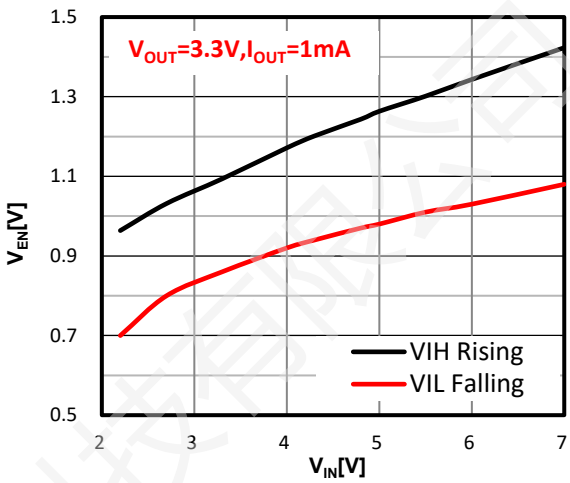


Figure 8. $V_{EN}$ vs $V_{IN}$

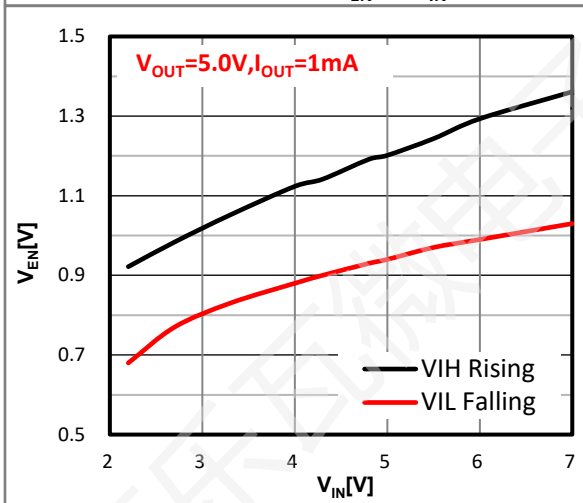


Figure 9. $V_{EN}$ vs $V_{IN}$

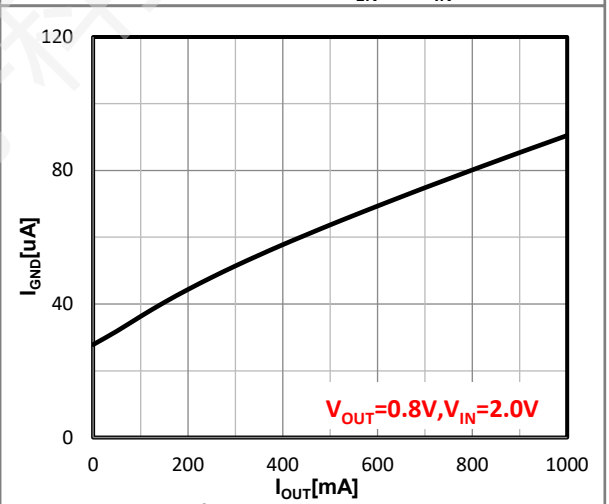


Figure 10. $I_{GND}$ vs $I_{OUT}$

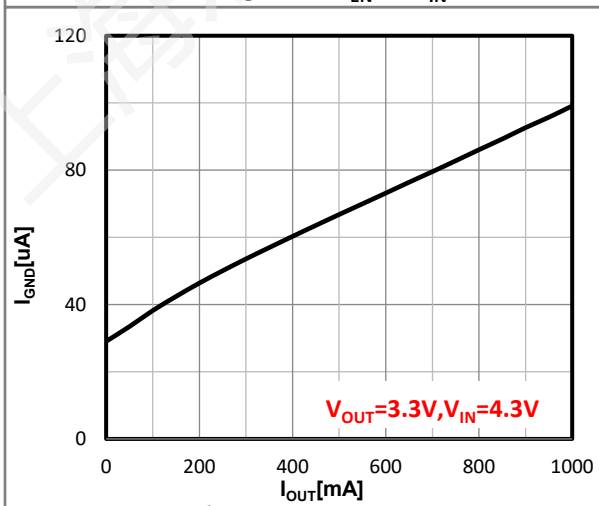


Figure 11. $I_{GND}$ vs $I_{OUT}$

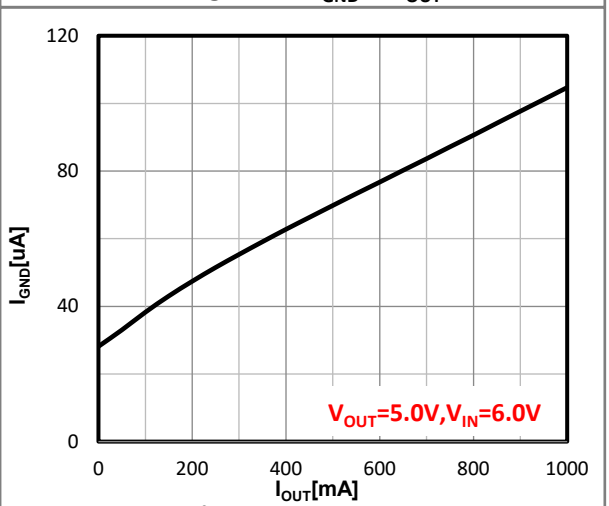


Figure 12. $I_{GND}$ vs $I_{OUT}$

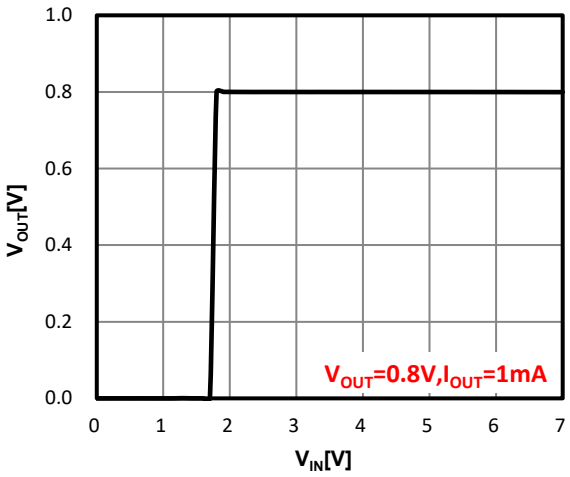



Figure 13. $V_{OUT}$ vs $V_{IN}$

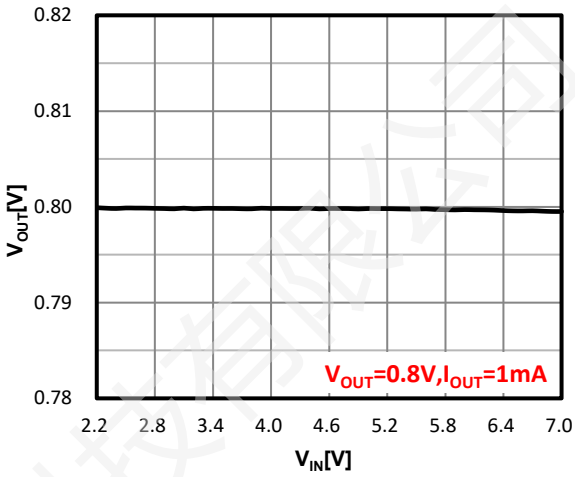



Figure 14. Line Regulation

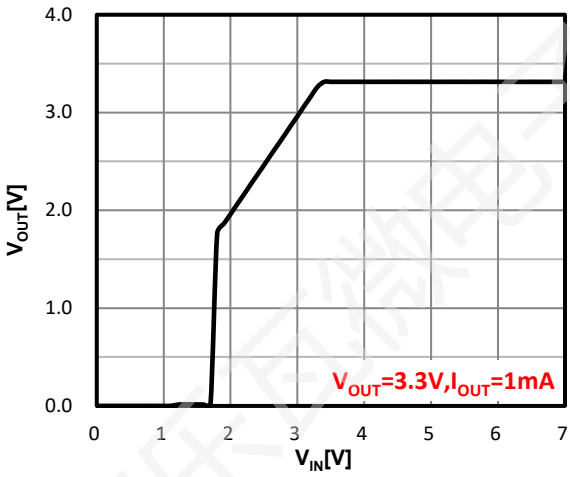



Figure 15. $V_{OUT}$ vs $V_{IN}$

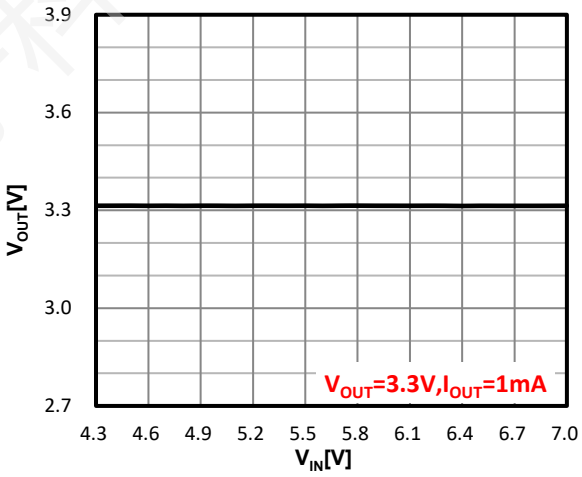



Figure 16. Line Regulation

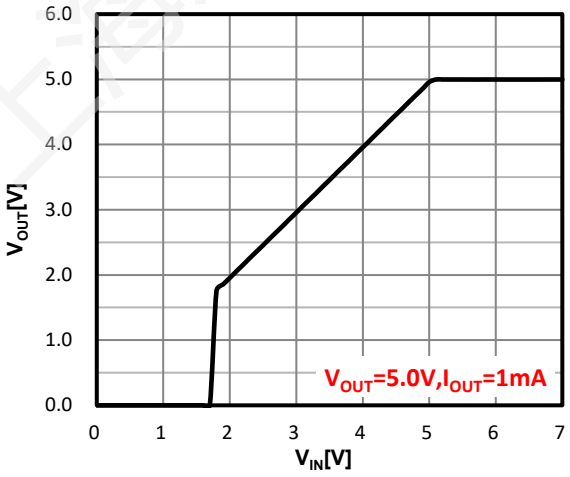



Figure 17. $V_{OUT}$ vs $V_{IN}$

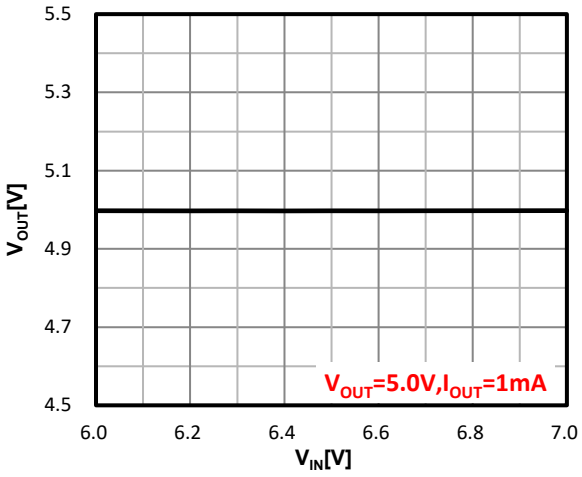



Figure 18. Line Regulation

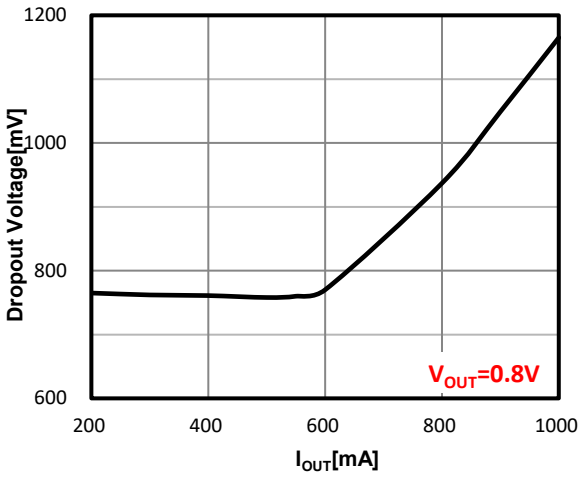



Figure 19. Dropout Voltage VS $I_{OUT}$

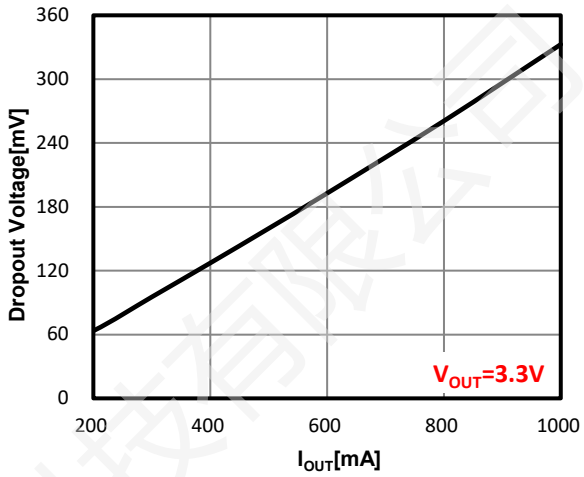



Figure 20. Dropout Voltage VS $I_{OUT}$

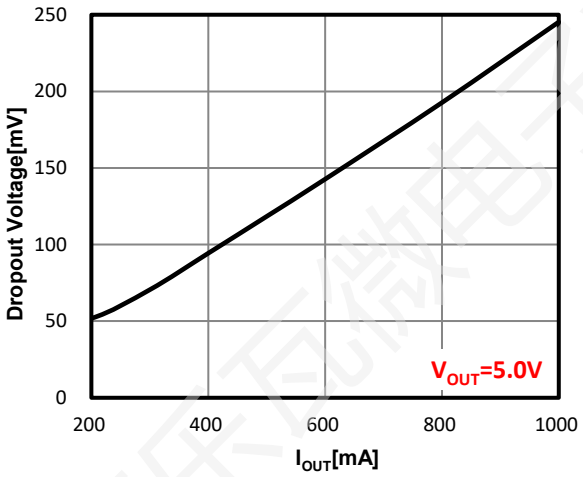



Figure 21. Dropout Voltage VS $I_{OUT}$

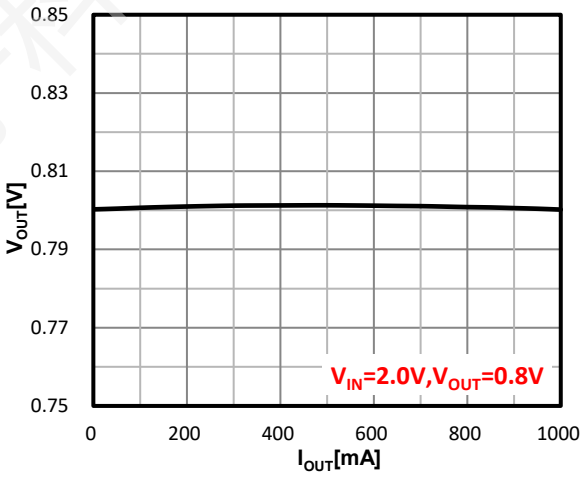



Figure 22. Load Regulation

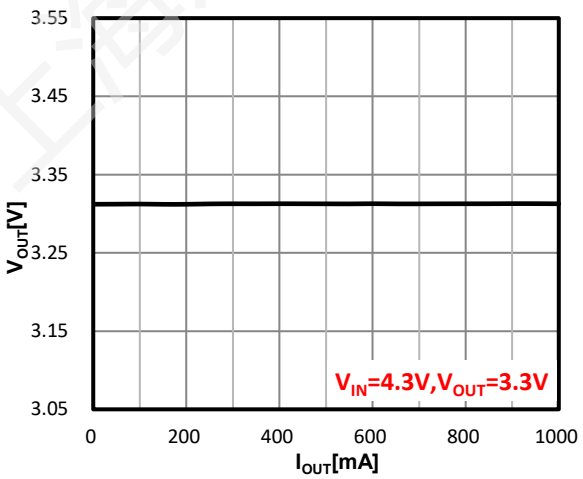



Figure 23. Load Regulation

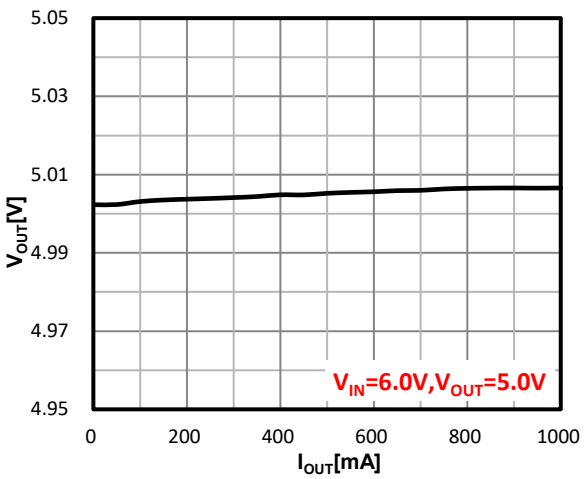
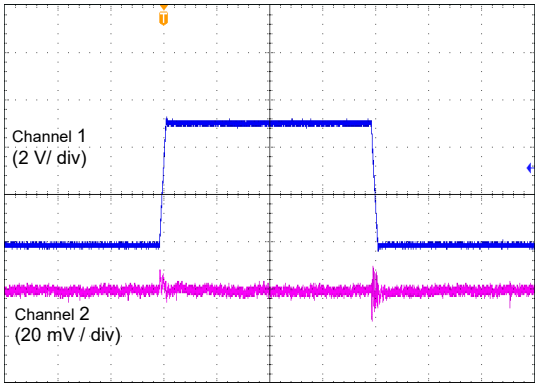
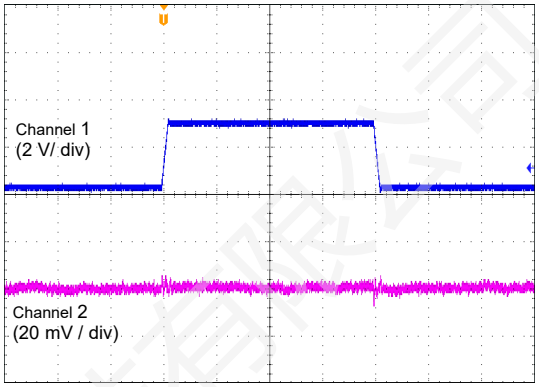



Figure 24. Load Regulation



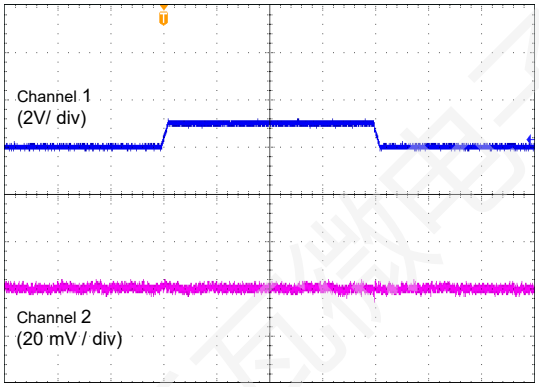

Channel 1 = $V_{IN}$, channel 2 =$V_{OUT}$, $V_{IN}$=1.8V→7.0V,
$t_R$=$t_F$=10µs, $V_{OUT}$=0.8V, $I_{OUT}$=10mA

**Figure 25. Line Transient**



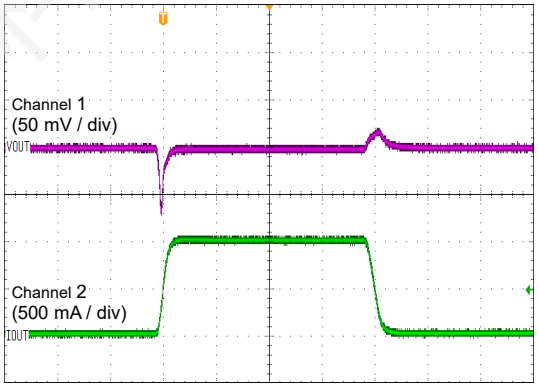

Channel 1 = $V_{IN}$, channel 2 =$V_{OUT}$, $V_{IN}$=4.3V→7.0V,
$t_R$=$t_F$=10µs, $V_{OUT}$=3.3V, $I_{OUT}$=10mA

**Figure 26. Line Transient**



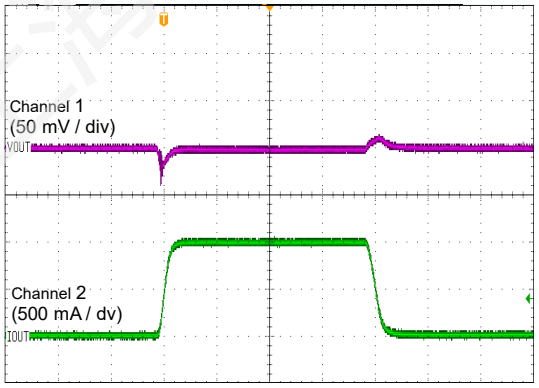

Channel 1 = $V_{IN}$, channel 2 =$V_{OUT}$, $V_{IN}$=6.0V→7.0V,
$t_R$=$t_F$=10µs, $V_{OUT}$=5.0V, $I_{OUT}$=10mA

**Figure 27. Line Transient**



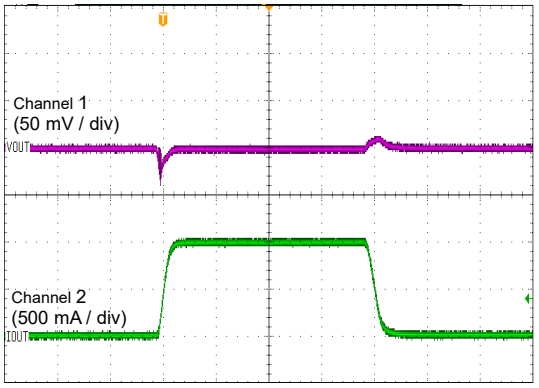

Channel 1 = $V_{OUT}$, channel 2 =$I_{OUT}$, $V_{IN}$=2.0V, $V_{OUT}$=0.8V
$C_{IN}$=$C_{OUT}$=1µF

**Figure 28. Load Transient (1 mA to 1A)**



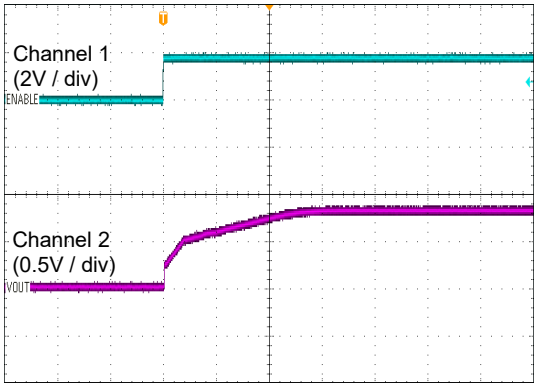

Channel 1 = $V_{OUT}$, channel 2 =$I_{OUT}$, $V_{IN}$=4.3V, $V_{OUT}$=3.3V
$C_{IN}$=$C_{OUT}$=1µF

**Figure 29. Load Transient (1 mA to 1A)**




Channel 1 = $V_{OUT}$, channel 2 =$I_{OUT}$, $V_{IN}$=6.0V, $V_{OUT}$=5.0V
$C_{IN}$=$C_{OUT}$=1µF

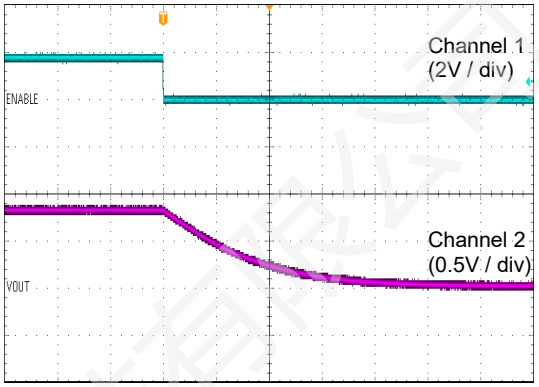
**Figure 30. Load Transient (1 mA to 1A)**




**Time (40 μs / div)**

Channel 1 = EN, channel 2 =$V_{OUT}$, $V_{IN}$=1.8V, EN=0→1.8V, $V_{OUT}$=0.8V, $C_{IN}$=$C_{OUT}$=1μF, No Load

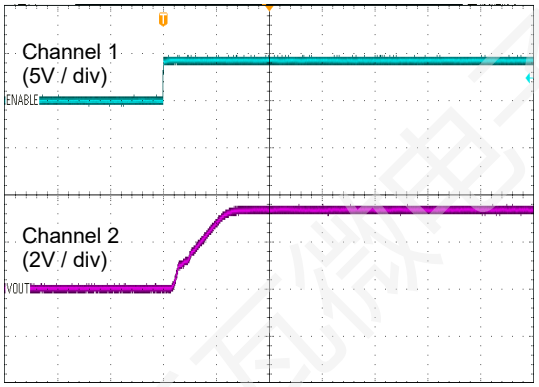
**Figure 31. Power-Up with Enable**




**Time (40 μs / div)**

Channel 1 = EN, channel 2 =$V_{OUT}$, $V_{IN}$=1.8V, EN=1.8→0V, $V_{OUT}$=0.8V, $C_{IN}$=$C_{OUT}$=1μF, No Load

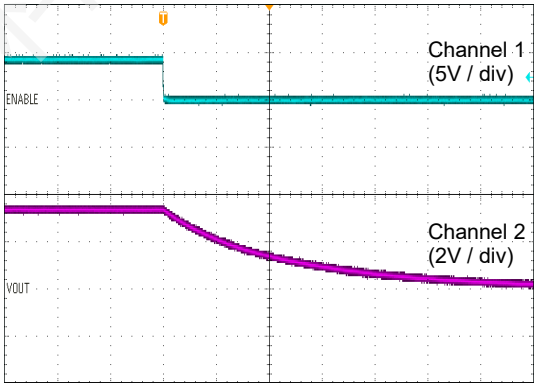
**Figure 32. Shut-Down with Enable**




**Time (40 μs / div)**

Channel 1 = EN, channel 2 =$V_{OUT}$, $V_{IN}$=4.3V, EN=0→4.3V, $V_{OUT}$=3.3V, $C_{IN}$=$C_{OUT}$=1μF, No Load

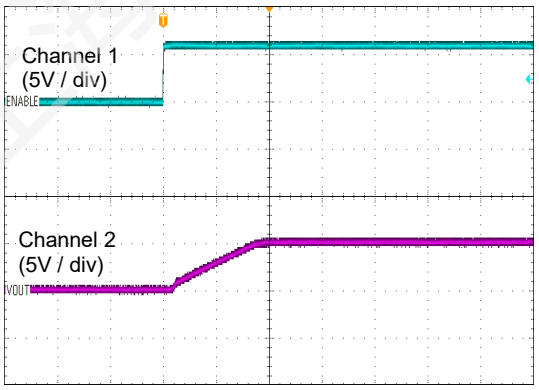
**Figure 33. Power-Up with Enable**




**Time (40 μs / div)**

Channel 1 = EN, channel 2 =$V_{OUT}$,$V_{IN}$=4.3V, EN=4.3→0V, $V_{OUT}$=3.3V, $C_{IN}$=$C_{OUT}$=1μF, No Load

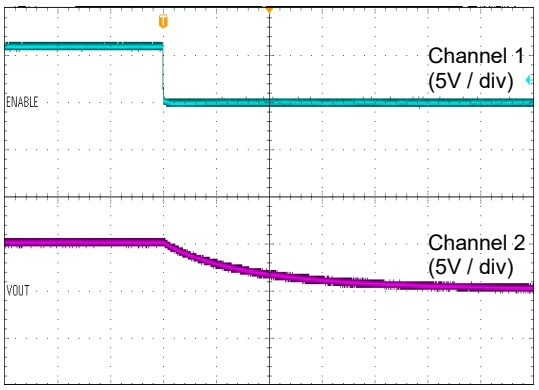
**Figure 34. Shut-Down with Enable**




**Time (40 μs / div)**

Channel 1 = EN, channel 2 =$V_{OUT}$, $V_{IN}$=6.0V, EN=0→6.0V, $V_{OUT}$=5.0V, $C_{IN}$=$C_{OUT}$=1μF, No Load

**Figure 35. Power-Up with Enable**




**Time (40 μs / div)**

Channel 1 = EN, channel 2 =$V_{OUT}$, $V_{IN}$=6.0V,EN=6.0→0V, $V_{OUT}$=5.0V, $C_{IN}$=$C_{OUT}$=1μF, No Load

**Figure 36. Shut-Down with Enable**

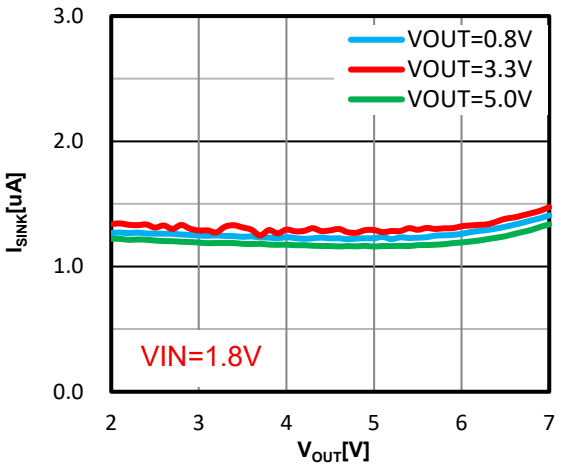



Figure 37. $V_{OUT}$ Sink Current VS Output Voltage

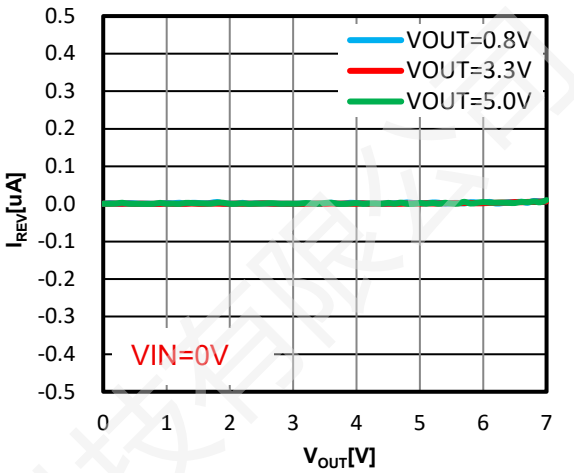
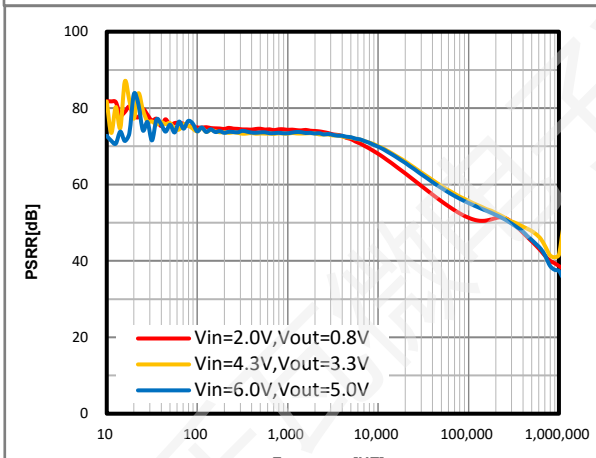
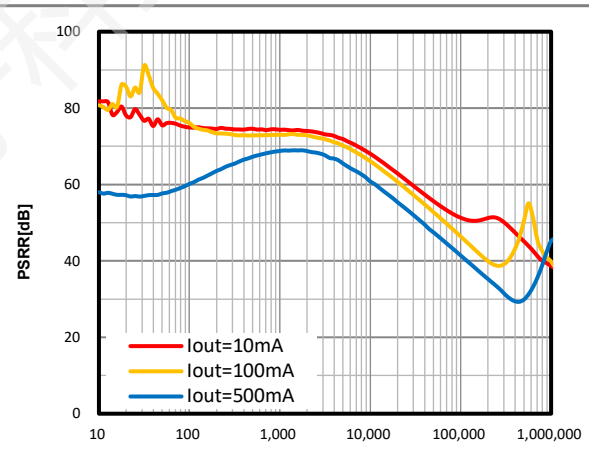



Figure 38. Reverse Current VS Output Voltage



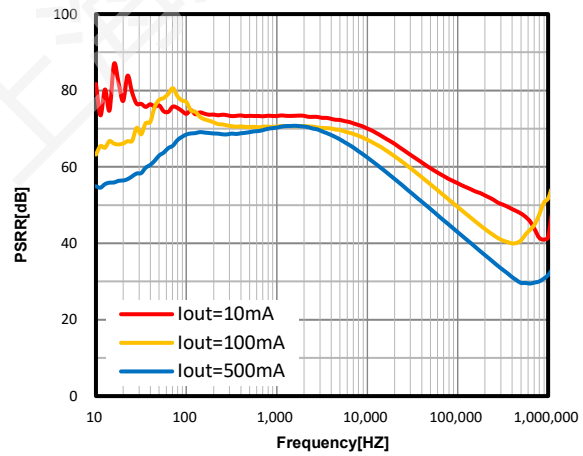

$V_{PP}$=0.5V,$C_{IN}$=0.22µF,$C_{OUT}$=1µF,$I_{OUT}$=10mA

Figure 39. PSRR vs Frequency



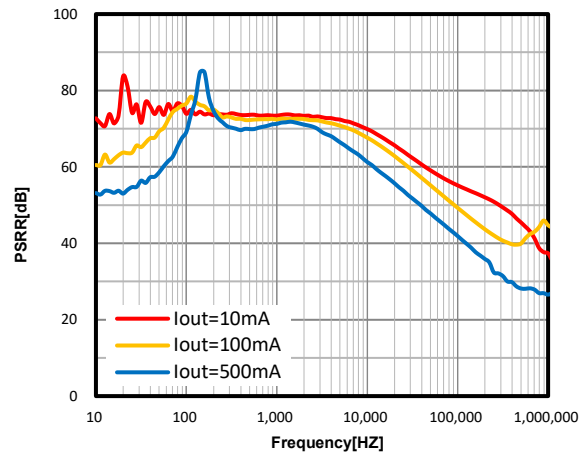

$V_{OUT}$=0.8V, $V_{IN}$=2.0V, $V_{PP}$=0.5V,$C_{IN}$=0.22µF,$C_{OUT}$=1µF

Figure 40. PSRR vs Frequency



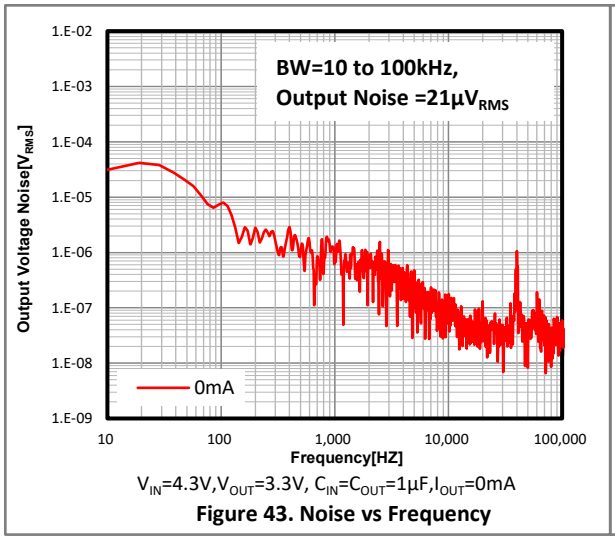

$V_{OUT}$=3.3V, $V_{IN}$=4.3V, $V_{PP}$=0.5V, $C_{IN}$=0.22µF,$C_{OUT}$=1µF

Figure 41. PSRR vs Frequency



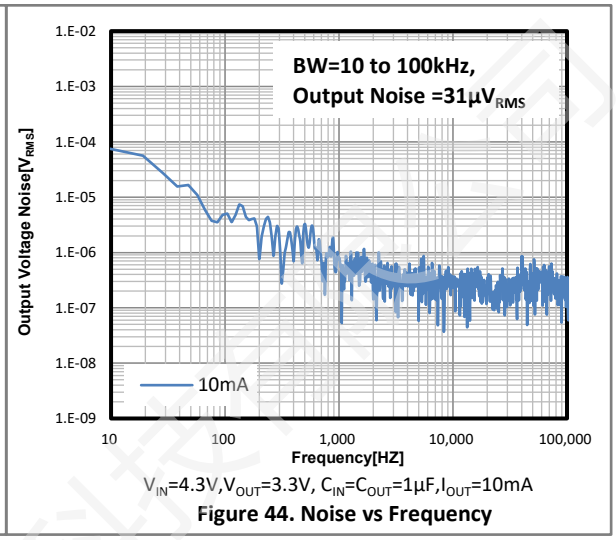

$V_{OUT}$=5.0V, $V_{IN}$=6.0V, $V_{PP}$=0.5V, $C_{IN}$=0.22µF,$C_{OUT}$=1µF

Figure 42. PSRR vs Frequency




$V_{IN}$=4.3V,$V_{OUT}$=3.3V, $C_{IN}$=$C_{OUT}$=1μF,$I_{OUT}$=0mA

**Figure 43. Noise vs Frequency**




$V_{IN}$=4.3V,$V_{OUT}$=3.3V, $C_{IN}$=$C_{OUT}$=1μF,$I_{OUT}$=10mA

**Figure 44. Noise vs Frequency**

## APPLICATION INFORMATION:

- **Input Capacitor Selection**

Like any low-dropout regulator, the external capacitors used with the LW82XX Series must be carefully selected for regulator stability and performance. Using a capacitor whose value is ≥1μF on the LW82XX Series input and the amount of capacitance can be increased without limit. The input capacitor must be located a distance less than 0.5 inch from the input pin of the IC and returned to a clean analog ground. Any good quality ceramic or tantalum can be used for this capacitor. The capacitor with larger value and lower ESR (equivalent series resistance) provides better PSRR and line-transient response.

- **Output Capacitor Selection**

The output capacitor must meet both requirements for minimum amount of capacitance and ESR in all LDOs application. The LW82XX Series is designed specifically to work with low ESR ceramic output capacitor in space-saving and performance consideration. Using a ceramic capacitor whose value is at least 1μF on the LW82XX Series output ensures stability. An appropriate output capacitor can reduce noise and improve load transient response and PSRR. The output capacitor should be located not more than 0.5 inch from the $V_{OUT}$ pin of the LW82XX Series and returned to a clean analog ground.

- **Layout considerations**

To improve ac performance such as PSRR, output noise, and transient response, it is recommended that the PCB be designed with separate ground planes for $V_{IN}$ and $V_{OUT}$, with each ground plane connected only at the GND pin of the device.

## ORDER INFORMATION:

LW82①②③④⑤⑥

| Designator | Item | Symbol | Description |
|---|---|---|---|
| ①② | Output Voltage | 08~50 | e.g.1.2V→①=1,②=2 |
| ③④⑤⑥ | Packages | A22G | DFN2x2-6L(Type-A) |
| | | AD3H | DFN3x3-8L |
| | | A23E | SOT23-5L |
| | | A89E | SOT89-5L |

| Part # | Output Voltage | Package | Shipping |
|---|---|---|---|
| LW8208A22G | 0.8V | DFN2x2-6L | 3000 Pcs/ Tape & Reel |
| LW8212A22G | 1.2V | | |
| LW8215A22G | 1.5V | | |
| LW8218A22G | 1.8V | | |
| LW8228A22G | 2.8V | | |
| LW8230A22G | 3.0V | | |
| LW8233A22G | 3.3V | | |
| LW8236A22G | 3.6V | | |
| LW8242A22G | 4.2V | | |
| LW8250A22G | 5.0V | | |
| LW8208AD3H | 0.8V | DFN3x3-8L | 5000 Pcs/ Tape & Reel |
| LW8212AD3H | 1.2V | | |
| LW8215AD3H | 1.5V | | |
| LW8218AD3H | 1.8V | | |
| LW8228AD3H | 2.8V | | |
| LW8230AD3H | 3.0V | | |
| LW8233AD3H | 3.3V | | |
| LW8236AD3H | 3.6V | | |
| LW8242AD3H | 4.2V | | |
| LW8250AD3H | 5.0V | | |

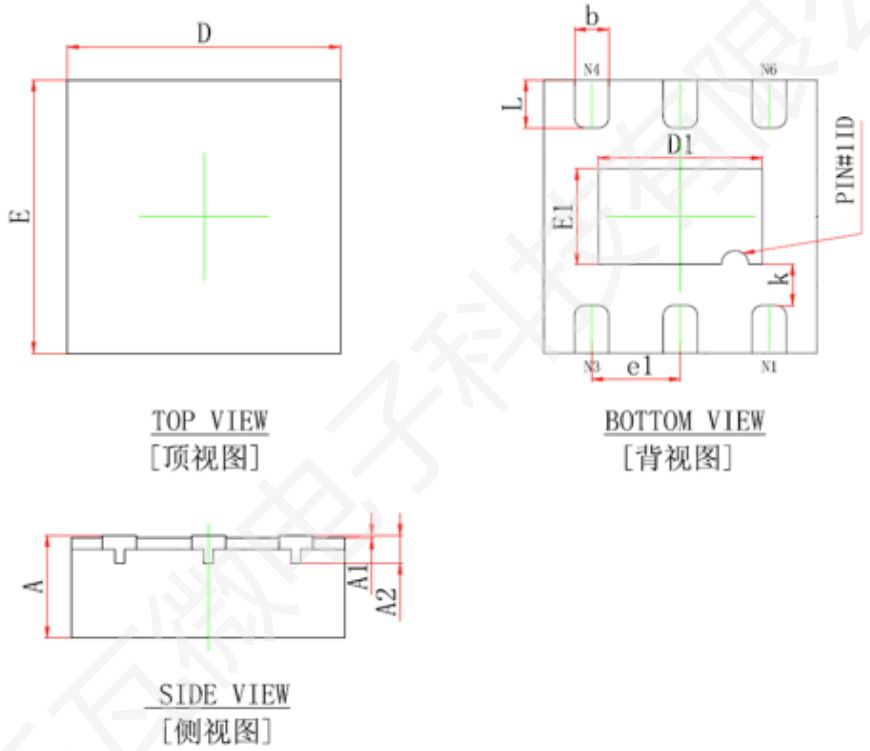
| Part # | Output Voltage | Package | Shipping |
|---|---|---|---|
| LW8208A23E | 0.8V | SOT23-5L | 3000 Pcs / Tape & Reel |
| LW8212A23E | 1.2V | | |
| LW8215A23E | 1.5V | | |
| LW8218A23E | 1.8V | | |
| LW8228A23E | 2.8V | | |
| LW8230A23E | 3.0V | | |
| LW8233A23E | 3.3V | | |
| LW8236A23E | 3.6V | | |
| LW8242A23E | 4.2V | | |
| LW8250A23E | 5.0V | | |
| LW8208A89E | 0.8V | SOT89-5L | 1000 Pcs/ Tape & Reel |
| LW8212A89E | 1.2V | | |
| LW8215A89E | 1.5V | | |
| LW8218A89E | 1.8V | | |
| LW8228A89E | 2.8V | | |
| LW8230A89E | 3.0V | | |
| LW8233A89E | 3.3V | | |
| LW8236A89E | 3.6V | | |
| LW8242A89E | 4.2V | | |
| LW8250A89E | 5.0V | | |

If customers have special output voltage requirements, please contact us.

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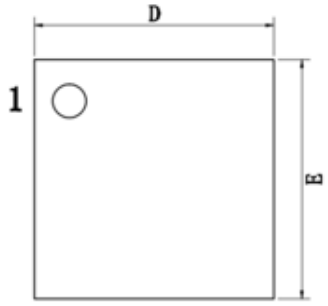
## PACKAGE OUTLINE:

### DFN2x2-6L Package

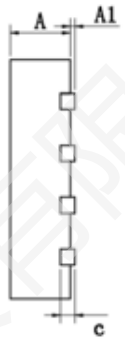



| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|---|---|---|---|---|
| | Min. | Max. | Min. | Max. |
| A | 0.700 | 0.800 | 0.028 | 0.031 |
| A1 | 0.000 | 0.050 | 0.000 | 0.002 |
| A2 | 0.203REF. | | 0.008REF. | |
| D | 1.924 | 2.076 | 0.076 | 0.082 |
| E | 1.924 | 2.076 | 0.076 | 0.082 |
| D1 | 1.150 | 1.250 | 0.045 | 0.049 |
| E1 | 0.650 | 0.750 | 0.026 | 0.030 |
| b | 0.200 | 0.300 | 0.008 | 0.012 |
| e1 | 0.650TYP. | | 0.026TYP. | |
| k | 0.200MIN. | | 0.008MIN. | |
| L | 0.300 | 0.400 | 0.012 | 0.016 |

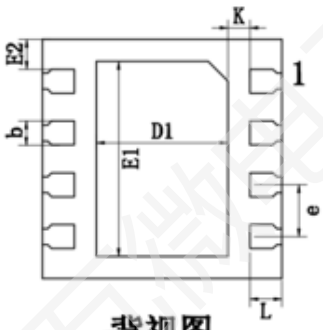
## DFN3x3-8L Package




俯视图




侧视图



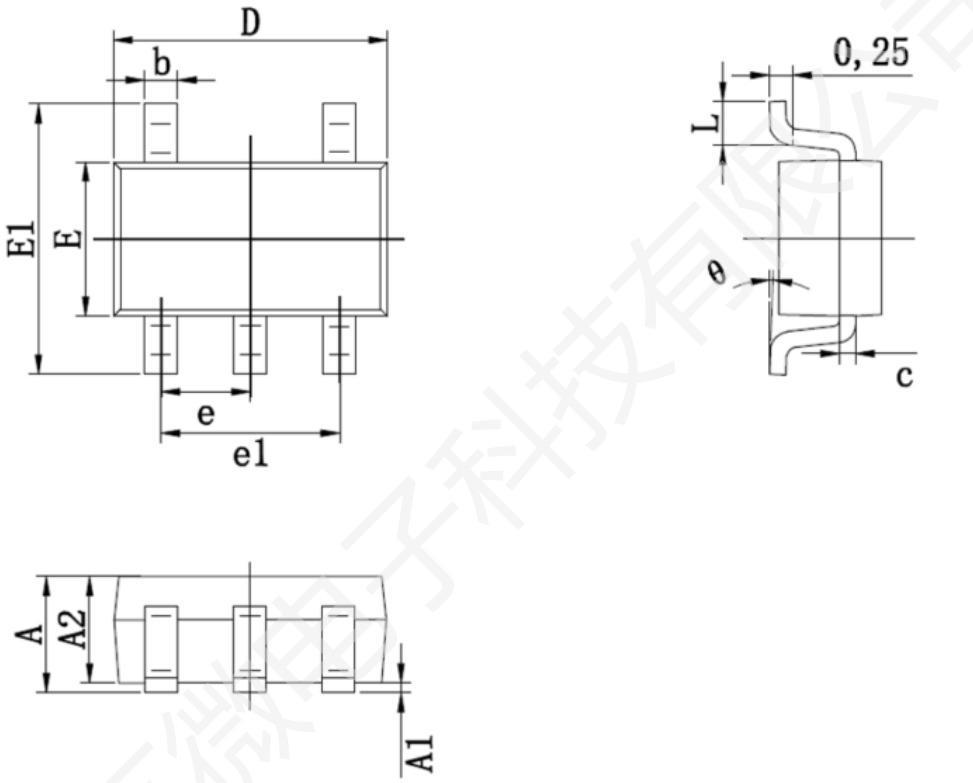

背视图

| SYMBOL | MILLMETER | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| * A | 0.50 | 0.55 | 0.60 |
| | 0.70 | 0.75 | 0.80 |
| A1 | 0.00 | — | 0.05 |
| b | 0.25 | 0.30 | 0.35 |
| c | 0.203 TYP | | |
| D | 2.95 | 3.00 | 3.05 |
| D1 | 1.55 | 1.65 | 1.75 |
| E | 2.95 | 3.00 | 3.05 |
| E1 | 2.35 | 2.45 | 2.55 |
| E2 | 0.375 REF | | |
| e | 0.65 BSC | | |
| K | 0.275 REF | | |
| L | 0.35 | 0.40 | 0.45 |

注：* A值为可选择封装厚度值，
封装厚度以焊线图定义为准

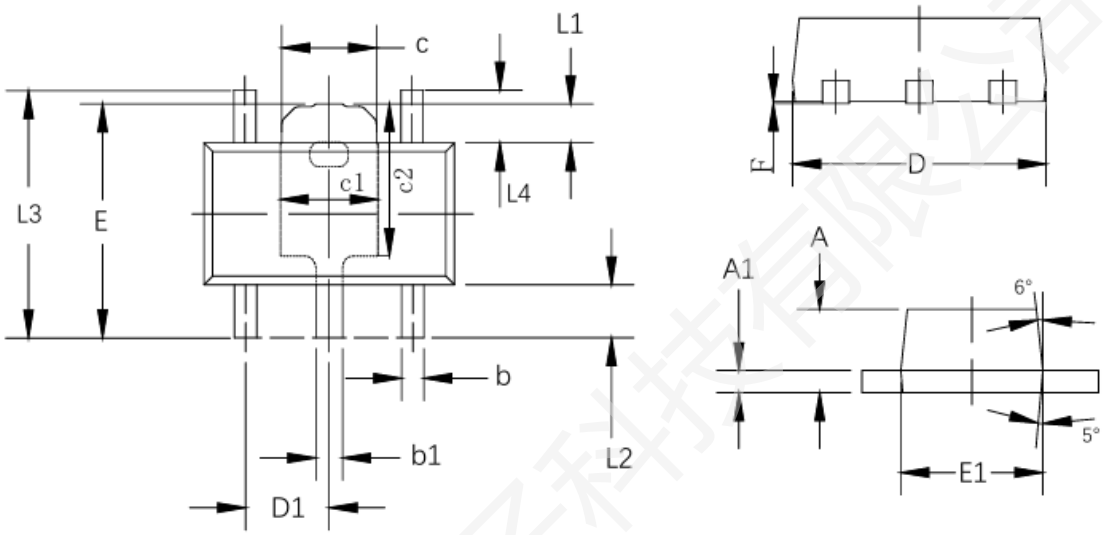
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## SOT23-5L Package




| COMMON DIMENSION (MM) | | | |
|---|---|---|---|
| PKG | SOT23-5L | | |
| Symbol | MIN | NOM | MAX |
| A | — | — | 1.300 |
| A1 | 0.010 | — | 0.150 |
| A2 | 1.050 | 1.100 | 1.150 |
| b | 0.300 | 0.350 | 0.400 |
| c | 0.125 | 0.150 | 0.175 |
| D | 2.870 | 2.920 | 2.980 |
| E | 1.550 | 1.610 | 1.670 |
| E1 | 2.650 | 2.850 | 3.000 |
| e | 0.95 BSC | | |
| e1 | 1.800 | 1.900 | 2.000 |
| L | 0.300 | 0.450 | 0.600 |
| θ | 0° | 4° | 8° |

## SOT89-5L Package




| COMMON DIMENSION(MM) | | | |
|---|---|---|---|
| PKG | SOT-89-5L | | |
| SYMBOL | MIN | TYP | MAX |
| A | 1.450 | 1.500 | 1.550 |
| A1 | 0.373 | 0.381 | 0.389 |
| b | 0.390 | 0.440 | 0.490 |
| b1 | 0.470 | 0.520 | 0.570 |
| c | 1.650 | 1.700 | 1.750 |
| c1 | 1.700 | 1.750 | 1.800 |
| c2 | 2.800 | 2.850 | 2.900 |
| D | 4.445 | 4.500 | 4.550 |
| D1 | 1.470 | 1.500 | 1.550 |
| E | 4.100 | 4.200 | 4.300 |
| E1 | 2.450 | 2.500 | 2.550 |
| F | - | - | 0.050 |
| L1 | 0.630 | 0.680 | 0.730 |
| L2 | 0.890 | 0.940 | 0.990 |
| L3 | 4.300 | 4.400 | 4.500 |
| L4 | 0.880 | 0.930 | 0.980 |

## Revision History:

| Revision | Date | Descriptions |
|---|---|---|
| Rev 0.1 | Sep.2023 | Initial Version |
| Rev 1.0 | Nov.2023 | Formal Version |
| Rev 1.1 | Sep.2026 | Added some parameters for the 0.8V and 5V versions |
| Rev 1.2 | Nov.2026 | Update Typical Performance & Operating Characteristics and Block |

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