HB10N200S

N-CHANNEL MOSFET

R+O 宏嘉诚科技
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TO-252 Plastic-Encapsulate MOSFETS

● Features

· V_{DS}=100V
· I_D=45A
· $R_{DS(on)}@V_{GS}$=10V $<$ 20mΩ
· SGT technology
· Avalanche energy tested
· Fast Switching Speedze

Drain-source Voltage
100 V
Drain Current
45 Ampere
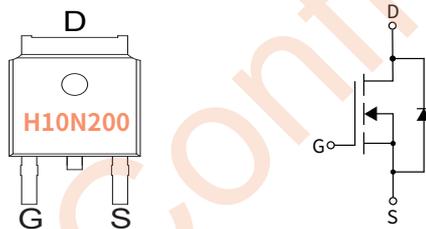
TO-252

● Applications

· Battery protection
· Load switch
· Power management

● Mechanical Data

· Case: TO-252
  Molding compound meets UL 94V-0 flammability rating, RoHS-compliant,halogen-free
· Terminals: Solder plated, solderable per MIL-STD-750,Method 2026

● Function Diagram

● Maximum Ratings (Ta=25℃ Unless otherwise specified)

PARAMETER	SYMBOL	UNIT	VALUE
Drain-source Voltage	V_{DS}	V	100
Gate-source Voltage	V_{GS}	V	±20
Drain Current	I_D	A	45
Pulsed Drain Current [1]	I_{DM}	A	130
Total Power Dissipation	P_D	W	52
Single pulse avalanche energy[2]	EAS	mJ	60
Junction temperature	T_J	℃	-55 ~+150
Storage temperature	T_{stg}	℃	-55 ~+150
Thermal Resistance Junction-to-Case	$R_{θJC}$	℃ / W	2.4
Thermal resistance, junction – ambient	R_{thJA}	℃ / W	50

● Ordering Information

PACKAGE	PACKAGE CODE	UNIT WEIGHT(g)	REEL(pcs)	BOX(pcs)	CARTON(pcs)	DELIVERY MODE
TO-252	R3	0.305	2500	5000	50000	13''

● Static Parameter Characteristics (Tj=25℃ Unless otherwise specified)

PARAMETER	SYMBOL	Condition	UNIT	Min	Typ	Max
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V$, $I_D=250\mu A$	V	100	—	—
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=100V$, $V_{GS}=0V$	μA	—	—	1.0
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm20V$, $V_{DS}=0V$	nA	—	—	±100
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}$, $I_D=250\mu A$	V	1.2	1.6	2.2
Static Drain-Source On-Resistance [3]	$R_{DS(ON)}$	$V_{GS}=10V$, $I_D=20A$	mΩ	—	14	20
Forward Transconductance	g_{FS}	$V_{DS}=5.0V$, $I_D=20A$	S	—	48	—

● Dynamic Parameters

PARAMETER	SYMBOL	Condition	UNIT	Min	Typ	Max
Input Capacitance	C_{iss}	$V_{DS}=50V$, $V_{GS}=0V$, f=1MHZ	pF	—	1020	—
Output Capacitance	C_{oss}			—	540	—
Reverse Transfer Capacitance	C_{rss}			—	40	—

● Switching Parameters

PARAMETER	SYMBOL	Condition	UNIT	Min	Typ	Max
Turn-on Delay Time	$t_{D(on)}$	$V_{GS}=10V$, $V_{DD}=50V$, $I_D=10A$, $R_{GEN}=6\Omega$	nS	—	4.3	—
Turn-on Rise Time	t_r		nS	—	5.1	—
Turn-off Delay Time	$t_{D(off)}$		nS	—	16.7	—
Turn-off fall Time	t_f		nS	—	8.7	—
Total Gate Charge	Q_g	$V_{DS}=50V$, $I_D=10A$, $V_{GS}=10V$	nC	—	12.7	—
Gate-Source Charge	Q_{gs}		nC	—	2.1	—
Gate-Drain Charge	Q_{gd}		nC	—	3.3	—

● Drian-Source Diode Characteristics

PARAMETER	SYMBOL	Condition	UNIT	Min	Typ	Max
Diode Forward Voltage	V_{SD}	$I_S=20A$, $V_{GS}=0V$	V	—	—	1.2
Maximum Body-Diode Continuous Current	I_S	—	A	—	—	45
Reverse Recovery Time	t_{rr}	Tj=25℃, $I_{F}=20A$ di/dt=100A/μs	nS	—	39	—
Reverse Recovery Charge	Q_{rr}		nC	—	30	—

Note :

(1)Repetitive Rating: Pulse width limited by maximum junction temperature.

(2)EAS condition : Tj=25℃ ,VDD=20V,VG=10V,L=0.5mH,IAS=15.5A,Rg=25Ω.

(3)Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.

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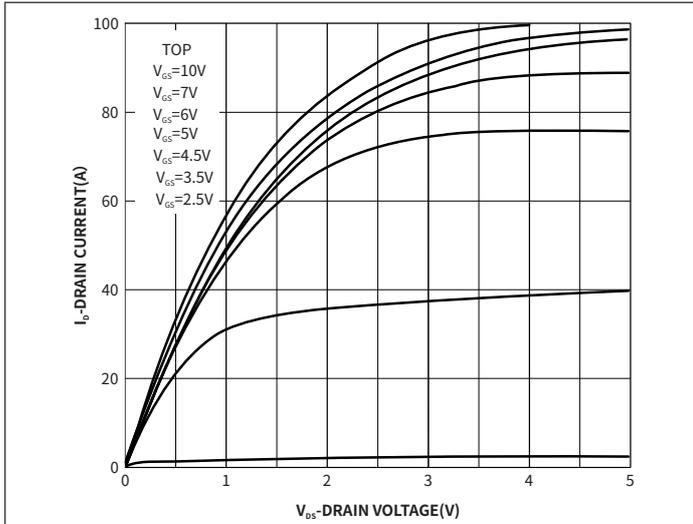● **Ratings And Characteristics Curves** (Ta=25°C Unless otherwise specified)
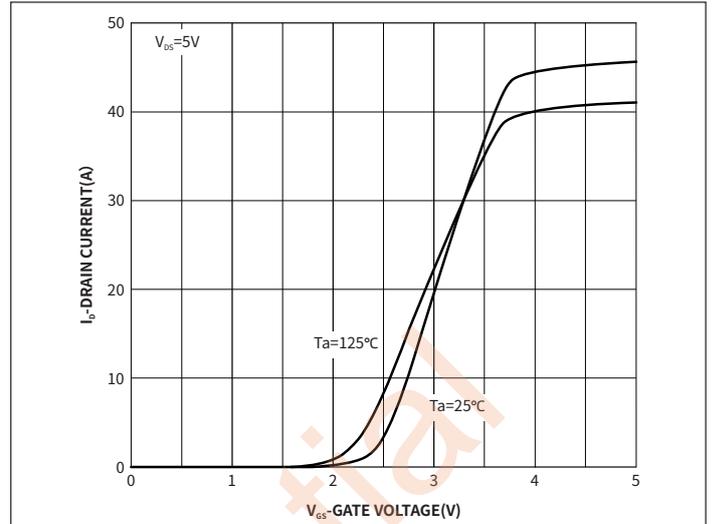

Fig.1 Output Characteristics
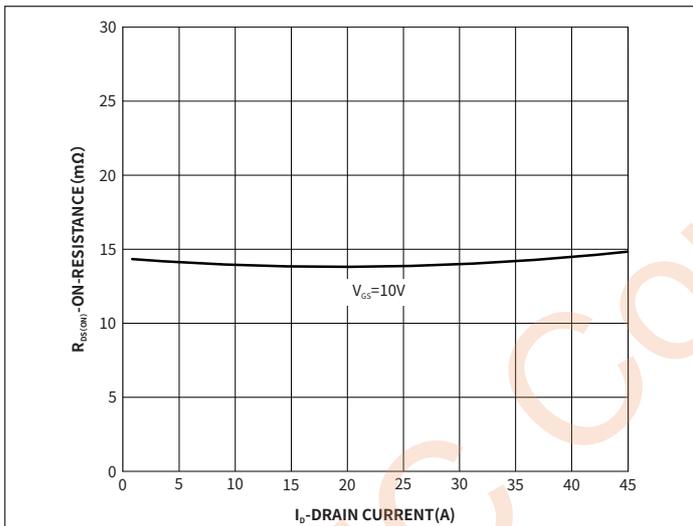

Fig.2 Transfer Characteristics

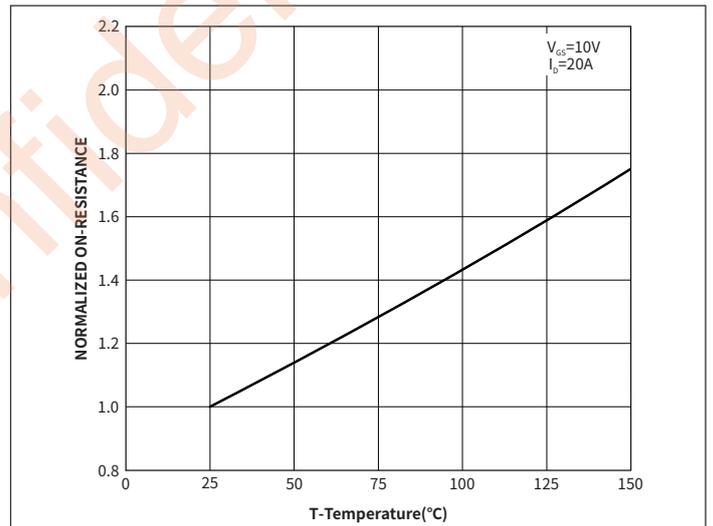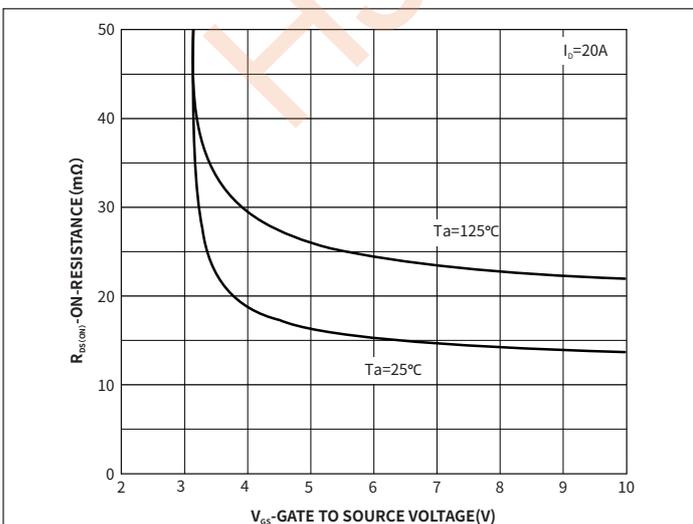Fig.3 On-Resistance vs. Drain Current and Gate Voltage

Fig.4 On-Resistance vs. Junction Temperature
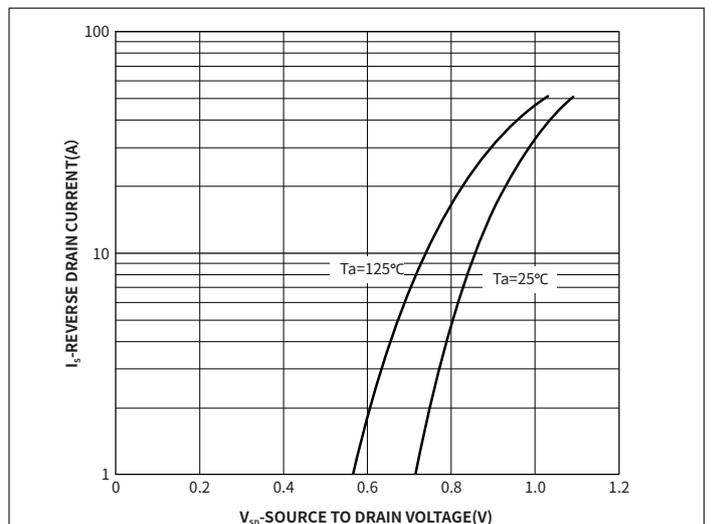

Fig.5 On-Resistance vs. Gate to Source Voltage

Fig.6 Typical Body-Diode Forward Characteristics

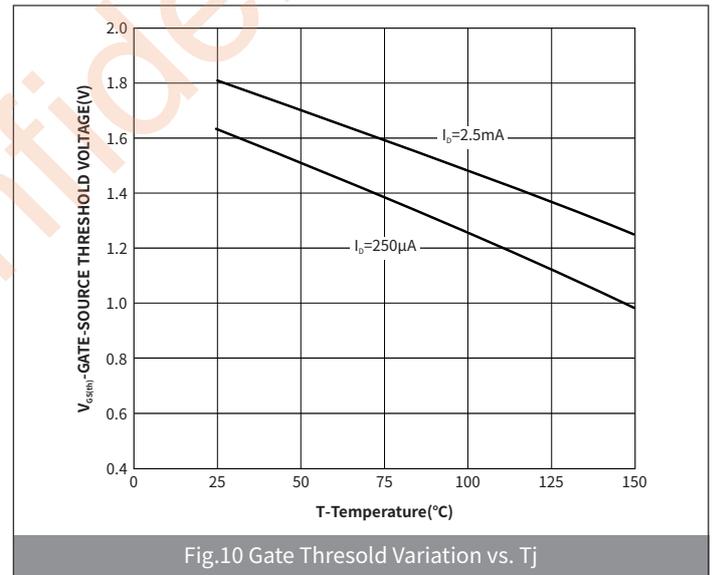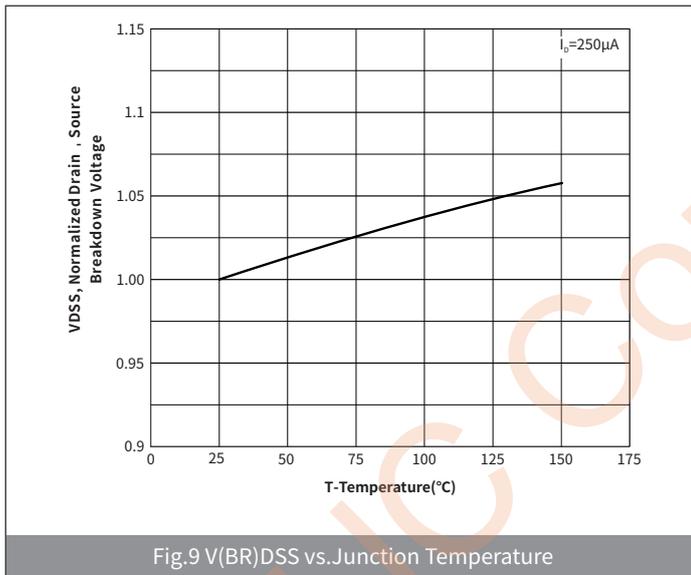# HB10N200S

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● **Ratings And Characteristics Curves** (Ta=25℃ Unless otherwise specified)

Fig.7 Capacitance Characteristics

Fig.8 Gate Charge

Fig.9 V(BR)DSS vs.Junction Temperature

Fig.10 Gate Thresold Variation vs. Tj

Fig.11 Safe Operation Area

● Ratings And Characteristics Curves (Ta=25℃ Unless otherwise specified)

$D=T_{on}/T$
$T_{J1PK}=T_C+P_{DM}\cdot Z_{\theta JC}\cdot R_{\theta JC}$
$R_{\theta JC}=2.3℃/W$

In descending order
D=0.9,0.7,0.5,0.3, 0.1,0.05 ,0.02,0.01,0.005,0.002, single pulse

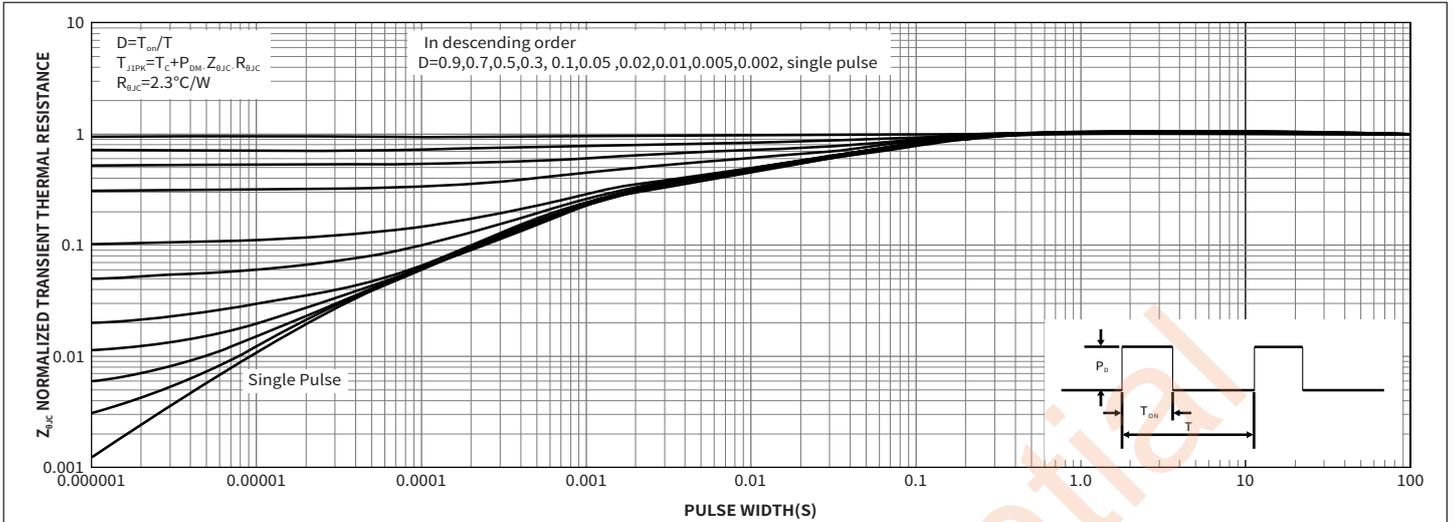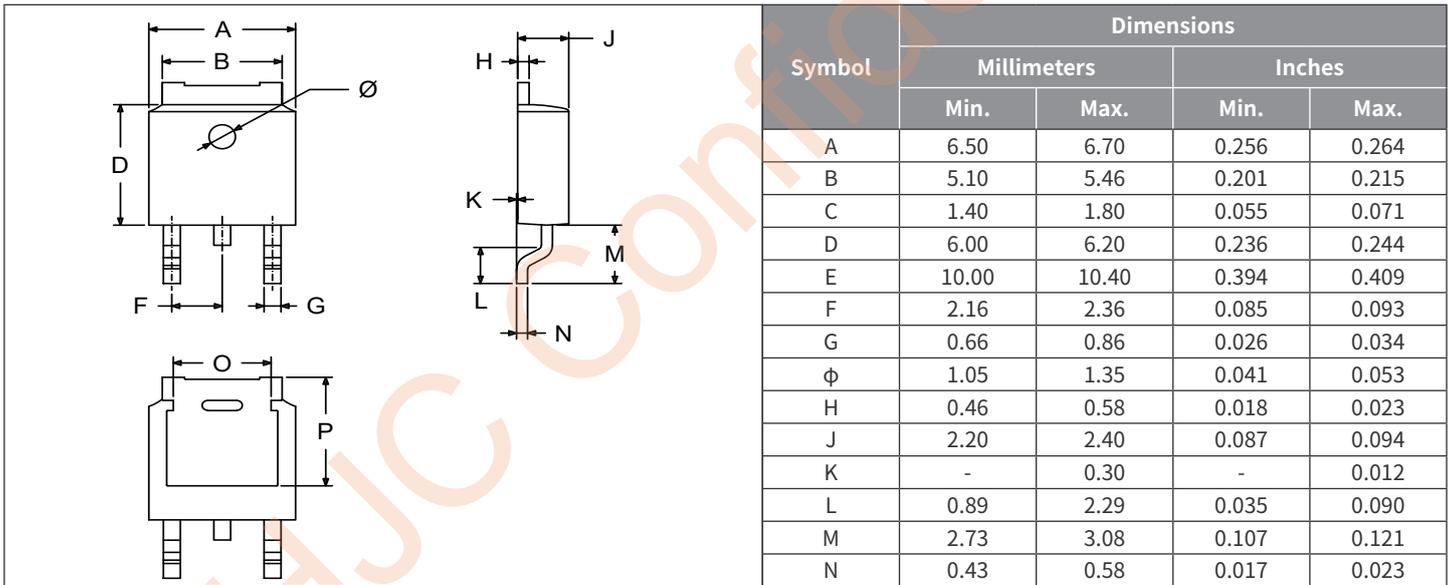Single Pulse

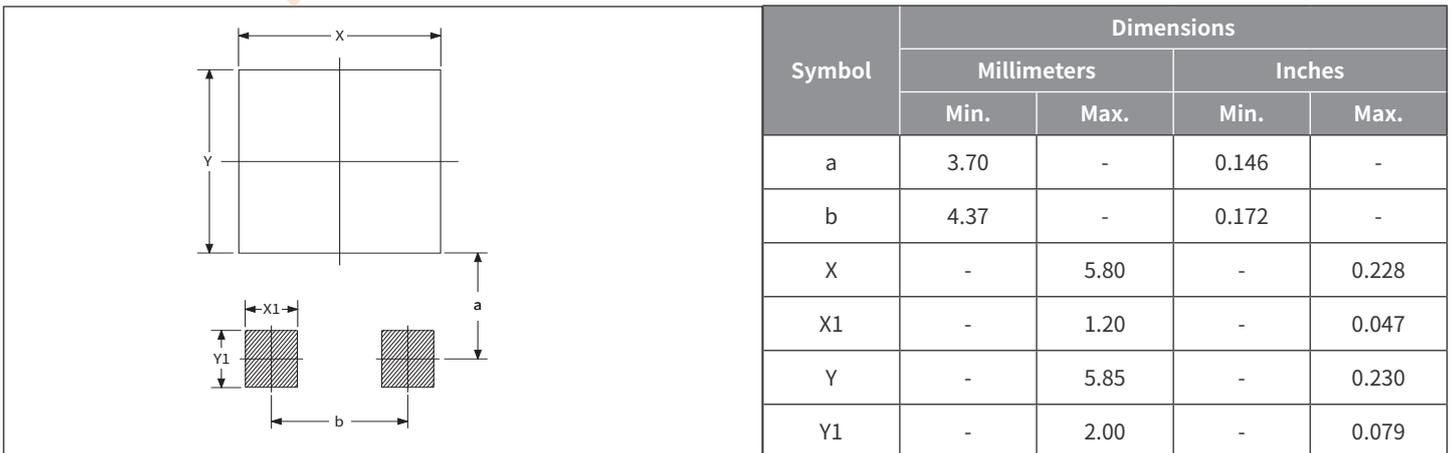$Z_{\theta JC}$ NORMALIZED TRANSIENT THERMAL RESISTANCE
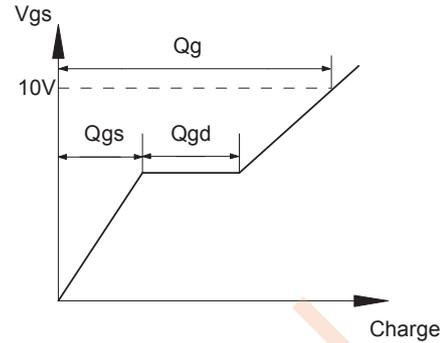
PULSE WIDTH(S)

Fig.12 Normalized Maximum Transient Thermal Impedance

● Package Outline Dimensions (TO-252)

| Symbol	Dimensions			
	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	6.50	6.70	0.256	0.264
B	5.10	5.46	0.201	0.215
C	1.40	1.80	0.055	0.071
D	6.00	6.20	0.236	0.244
E	10.00	10.40	0.394	0.409
F	2.16	2.36	0.085	0.093
G	0.66	0.86	0.026	0.034
Φ	1.05	1.35	0.041	0.053
H	0.46	0.58	0.018	0.023
J	2.20	2.40	0.087	0.094
K	-	0.30	-	0.012
L	0.89	2.29	0.035	0.090
M	2.73	3.08	0.107	0.121
N	0.43	0.58	0.017	0.023

● Suggested Pad Layout

Symbol	Dimensions			
	Millimeters		Inches	
	Min.	Max.	Min.	Max.
a	3.70	-	0.146	-
b	4.37	-	0.172	-
X	-	5.80	-	0.228
X1	-	1.20	-	0.047
Y	-	5.85	-	0.230
Y1	-	2.00	-	0.079

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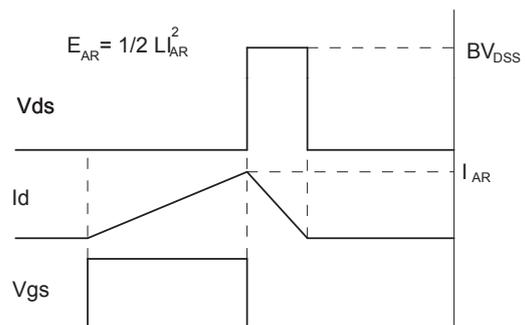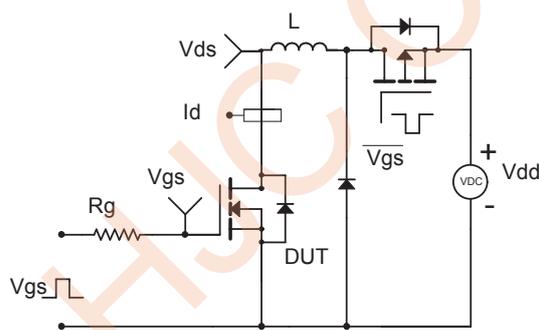
1.Gate Charge Test Circuit & Waveforms
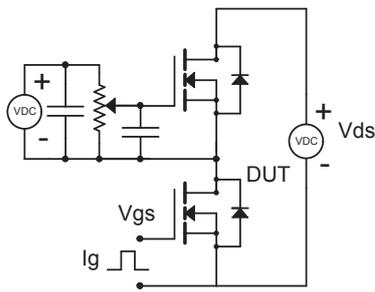
2. Resistive Switching Test Circuit & Waveforms
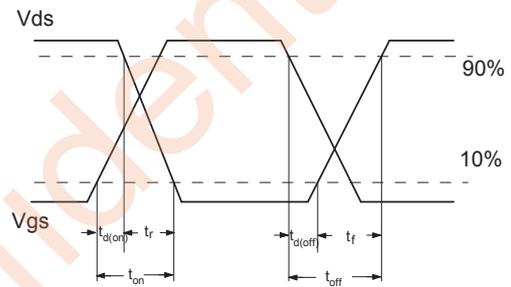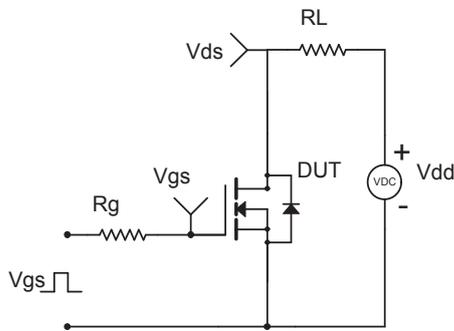
3.Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

$$E_{AR} = 1/2 \ LI_{AR}^2$$

4.Diode Recovery Test Circuit & Waveforms

$$Q_{rr} = -\int Idt$$