RoHS HAL Pb Green

Stereo Continuous Calibration DAC

(compatible to TDA3111&TP8211)

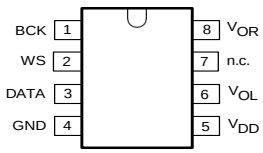
The HT1311A is a voltage-driven digital-to-analog converter and is new generation of DAC devices which embodies the innovative technique of Continuous Calibration (CC). The largest bit-currents are repeatedly generated by one single current reference source. This duplication is based upon an internal charge storage principle which has an accuracy insensitive to ageing, temperature matching and process variations.The HT1311A is fabricated in a 1.0 μm CMOS process and features an extremely low-power dissipation, small package size and easy application. Furthermore, the accuracy of the intrinsic high coarse-current combined with the implemented symmetrical offset decoding method preclude zero-crossing distortion and ensures high quality audio reproduction. Therefore, the CC-DAC is eminently suitable for use in (portable) digital audio equipment.

FEATURES

- Voltage output
- Low power consumption
- Wide dynamic range (16-bit resolution)
- Continuous Calibration (CC) concept
- Easy application:
  - single 4 to 5.5 V rail supply
  - output current and bias current are proportional to the supply voltage
  - integrated current-to-voltage converter
- Fast settling time permits 2, 4 and 8 × oversampling (serial input) or double-speed operation at 4 × oversampling
- Internal bias current ensures maximum dynamic range
- Wide operating temperature range (–40 °C to +85 °C)
- Compatible with most current Japanese input formats: time multiplexed, two's complement, TTL
- No zero-crossing distortion
- Cost efficient.

PIN CONFIGURATION

(TOP VIEW)

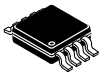


SOP (R), MSOP (M), DFN8 (D)

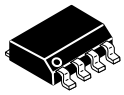
ORDERINGINFORMATION

1

DFN8 D SUFFIX HT1311ARDZ



MSOP−8 M SUFFIX HT1311ARMZ



SOP−8 R SUFFIX HT1311ARZ

&HT1311	= Specific Device Code
&A	= Version
&RD,RM,R	= Packaging
&Z	= Pb−Free Package
&#	=Date Code

T_A = -40° to 85°C for all packages

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage		4	5	5.5	V
I_{DD}	supply current	V_{DD} = 5 V at code 0000H	–	3.4	6.0	mA
V_{FS}	full scale output voltage	V_{DD} = 5 V	1.8	2.0	2.2	V
(THD+N)/S	total harmonic distortion plus noise	at 0 dB signal level	–	–68	–63	dB
			–	0.04	0.07	%
		at –60 dB signal level	–	–30	–24	dB
			–	3	6	%
		at –60 dB signal level; A-weighted	–	–33	–	dB
			–	2	–	%
S/N	signal-to-noise ratio at bipolar zero	A-weighted at code 0000H	86	92	–	dB
t_{cs}	current settling time to ±1 LSB		–	0.2	–	µs
BR	input bit rate at data input		–	–	18.4	Mbits/s
f_{BCK}	clock frequency at clock input		–	–	18.4	MHz
TC_{FS}	full scale temperature coefficient at analog outputs (I_{OL}; I_{OR})		–	±400	–	ppm
T_{amb}	operating ambient temperature		–40	–	+85	°C
P_{tot}	total power dissipation	V_{DD} = 5 V at code 0000H	–	17	30	mW

BLOCK DIAGRAM

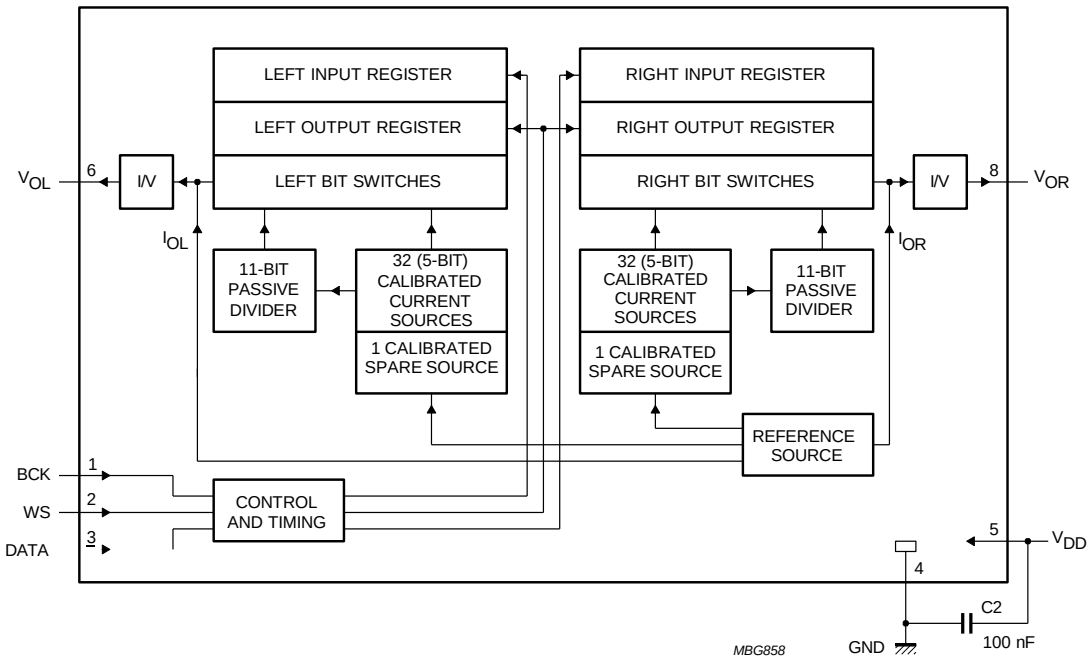


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
BCK	1	bit clock input
WS	2	word select input
DATA	3	data input
GND	4	ground
V_{DD}	5	supply voltage
V_{OL}	6	left channel output
n.c.	7	not connected
V_{OR}	8	right channel output

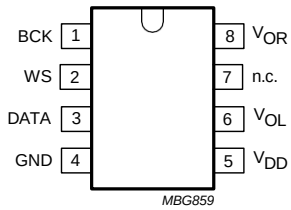


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The basic operation of the continuous calibration DAC is illustrated in Fig.3. The figure shows the calibration and operation cycle. During calibration of the MOS current source (see Fig.3a) transistor M1 is connected as a diode by applying a reference current. The voltage V_{gs} on the intrinsic gate-source capacitance C_{gs} of M1 is then determined by the transistor characteristics. After calibration of the drain current to the reference value I_{REF}, the switch S1 is opened and S2 is switched to the other position (see Fig.3b). The gate-to-source voltage V_{gs} of M1 is not changed because the charge on C_{gs} is preserved. Therefore, the drain current of M1 will still be equal to I_{REF} and this exact duplicate of I_{REF} is now available at the OUT terminal.

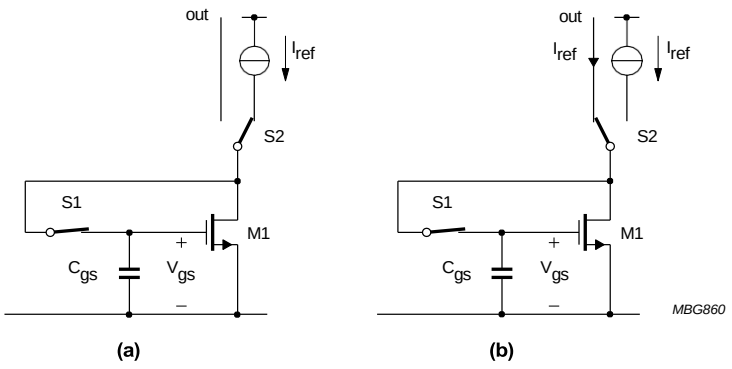
The 32 current sources and the spare current source of the HT1311A; AT are continuously calibrated (see Fig.1). The spare current source is included to allow continuous converter operation. The output of one calibrated source is connected to an 11-bit binary current divider consisting of 2048 transistors.

A symmetrical offset decoding principle is incorporated that arranges the bit switching in such a way that the zero-crossing is performed only by switching the LSB currents.

The HT1311A; AT (CC-DAC) accepts serial input data formats of 16-bit word length. Left and right data words are time multiplexed. The most significant bit (bit 1) must always be first. The input data format is shown in Figs 4 and 5.

With a HIGH level on the word select input (WS), data is placed in the left input register and with a LOW level on the WS input, data is placed in the right input register (see Fig.1). The data in the input registers are simultaneously latched in the output registers which control the bit switches.

An internal offset voltage V_{OS} is added to the full scale output voltage V_{FS}; V_{OS} and V_{FS} are proportional to V_{DD}: $V_{DD1}/V_{DD2} = V_{FS1}/V_{FS2} = V_{OS1}/V_{OS2}$.



(a) = calibration.
(b) = operation.

Fig.3 Calibration principle.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage		–	6.0	V
T_{stg}	storage temperature		–55	+150	°C
T_{XTAL}	maximum crystal temperature		–	+150	°C
T_{amb}	operating ambient temperature		–40	+85	°C
V_{es}	electrostatic handling	note 1	–2000	+2000	V
		note 2	–200	+200	V

Note

1. Human body model: C = 100 pF, R = 1500 Ω, 3 pulses positive and 3 pulses negative.
2. Machine model: C = 200 pF, L = 0.5 μH, R = 10 Ω, 3 pulses positive and 3 pulses negative.

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air		
	DIL8	100	K/W
	SO8	210	K/W

QUALITY SPECIFICATION

In accordance with SNW-FQ-0611.

CHARACTERISTICS

V_{DD} = 5 V; T_{amb} = 25 °C; measured in Fig.1; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage		4.0	5.0	5.5	V
I_{DD}	supply current	at code 0000H	–	3.4	6.0	mA
Digital inputs; pins WS, BCK and DATA						
$\|I_{IL}\|$	input leakage current LOW	V_I = 0.8 V	–	–	10	μA
$\|I_{IH}\|$	input leakage current HIGH	V_I = 2.4 V	–	–	10	μA
f_{BCK}	clock frequency		–	–	18.4	MHz
BR	bit rate data input		–	–	18.4	Mbits/s
f_{WS}	word select input frequency		–	–	384	kHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Timing (see Fig.4)						
t_r	rise time		–	–	12	ns
t_f	fall time		–	–	12	ns
t_{CY}	bit clock cycle time		54	–	–	ns
t_{BCKH}	bit clock pulse width HIGH		15	–	–	ns
t_{BCKL}	bit clock pulse width LOW		15	–	–	ns
$t_{SU;DAT}$	data set-up time		12	–	–	ns
$t_{HD:DAT}$	data hold time to bit clock		2	–	–	ns
$t_{HD:WS}$	word select hold time		2	–	–	ns
$t_{SU;WS}$	word select set-up time		12	–	–	ns
Analog outputs; pins V_{OL} and V_{OR}						
V_{FS}	full-scale voltage		1.8	2.0	2.2	V
TC_{FS}	full-scale temperature coefficient		–	±400	–	ppm
V_{os}	offset voltage	$V_{DD} = V_{OL/ORmax}$	0.45	0.50	0.55	V
(THD+N)/S	total harmonic distortion plus noise	at 0 dB signal level; note 1	–	–68	–63	dB
			–	0.04	0.07	%
		at –60 dB signal level; note 1	–	–30	–24	dB
			–	3	6	%
		at –60 dB signal level; A-weighted; note 1	–	–33	–	dB
			–	2	–	%
		at 0 dB signal level; f = 20 Hz to 20 kHz	–	–65	–61	dB
			–	0.05	0.09	%
t_{cs}	current settling time to ±1 LSB		–	0.2	–	µs
α_{cs}	channel separation		75	80	–	dB
$\lvert\delta I_O\rvert$	unbalance between outputs	note 1	–	0.2	0.3	dB
$\lvert t_d\rvert$	time delay between outputs		–	±0.2	–	µs
S/N	signal-to-noise ratio at bipolar zero	A-weighted at code 0000H	86	92	–	dB

Note

1. Measured with 1 kHz sinewave generated at sampling rate of 192 kHz.

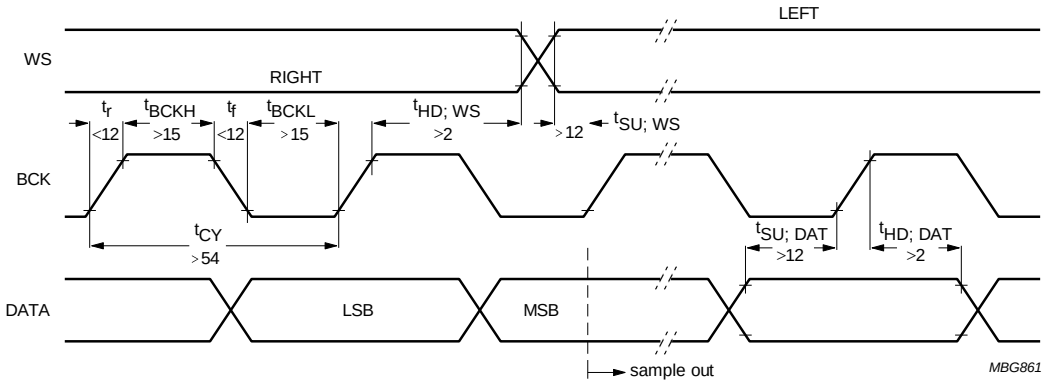


Fig.4 Timing and input signals.

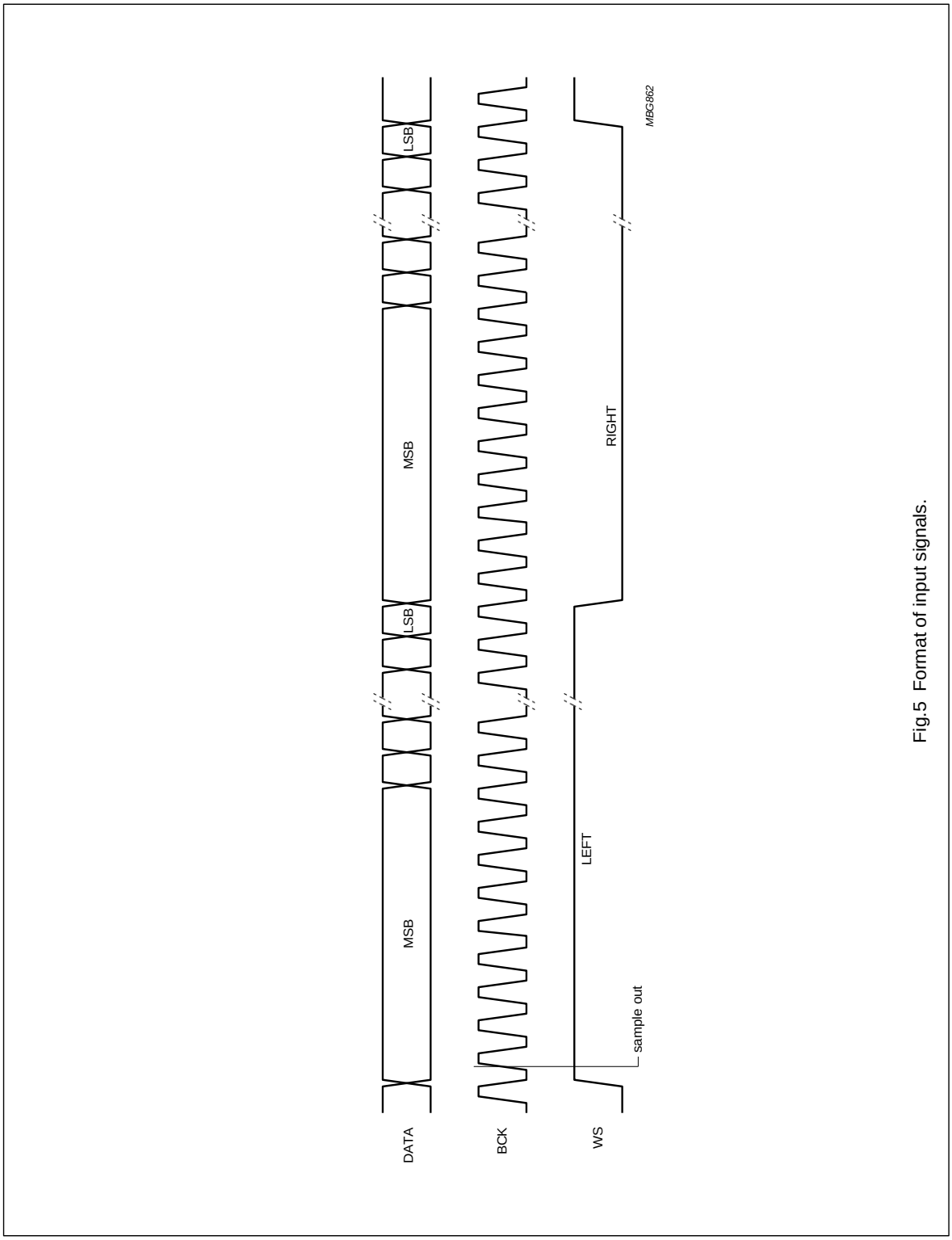


Fig.5 Format of input signals.

APPLICATION INFORMATION

Basic application example

A typical example of a CD-application with the HT1311A; AT is shown in Fig.6. It features typical decoupling components and a third-order analog post-filter stage providing a line output.

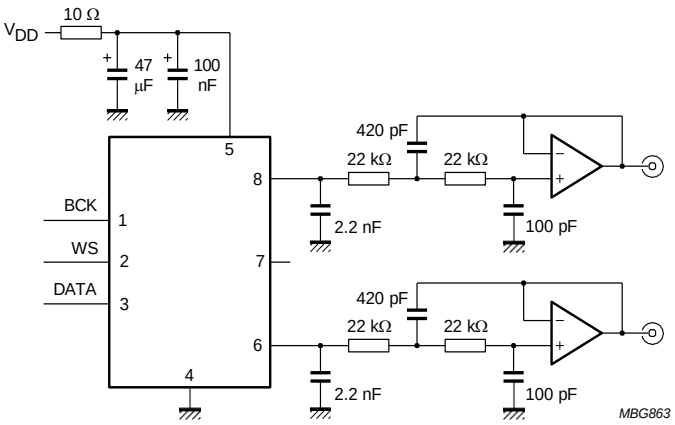


Fig.6 Example of a 3rd order filter application.

Attention to printed circuit board layout

The HT1311A and even more so the offers great ease in designing-in to printed-circuit boards due to its small size and low pin count. The HT1311A; AT being a mixed-signal IC in CMOS, some attention needs to be paid to layout and topology of the application PCB. Following some basic rules will yield the desired performance. The most important considerations are:

1. Supply: care should be taken to supply the HT1311A; AT with a clean, noiseless V_{DD}, for a good noise performance of the analog parts of the DAC. Supply purity can easily be achieved by using an RC-filtered supply.
2. Grounding: preferably a ground plane should be used, in order to have a low-impedance return available at any point in the layout. It is advantageous to make a partitioning of the ground plane according to the nature of the expected return currents (digital input returns separate from supply returns and separate from the analog section).
3. Topology: the capacitor decoupling high-frequency supply interference from V_{DD} to GND should be placed as close as is physically possible to the IC body, ensuring a low-inductance path to ground. The digital input conductors may be shielded by ground leads running alongside. The placement of a passive ground plane underside the entire IC surface gives `free` additional decoupling from the IC body to ground as well as providing a shield between the digital input pins and the analog output pins.

Figure 7 shows recommended layouts for printed-circuit boards for the SO8 and DIL8 versions respectively. Both layouts use a single-interconnect layer.

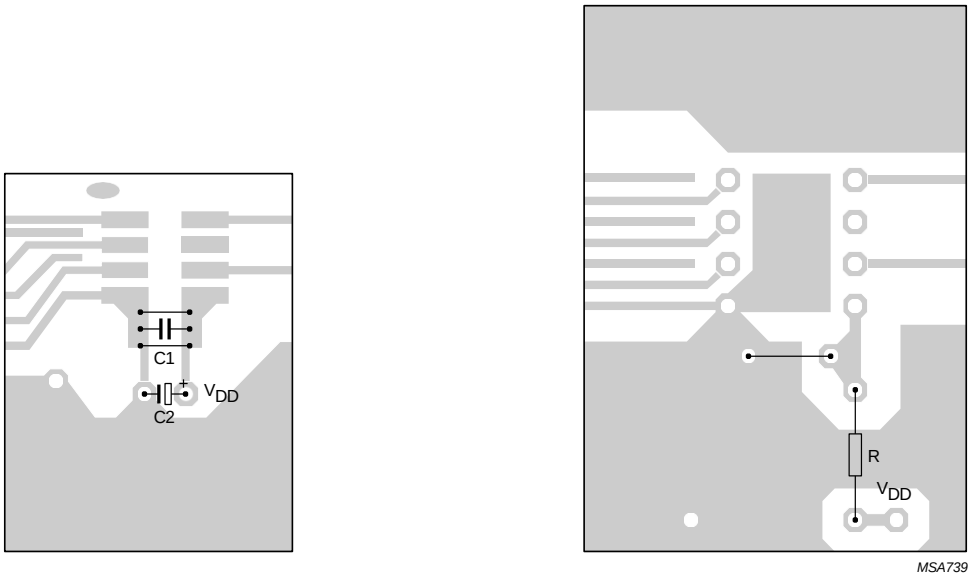
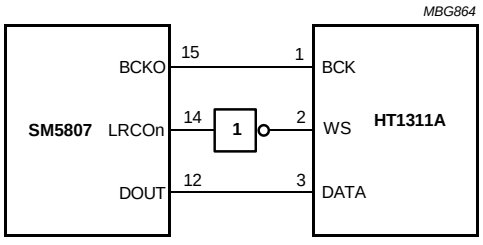


Fig.7 Recommended printed-circuit board layouts.

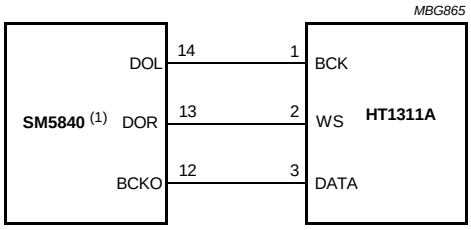
Interface examples

The following figures (Figs 8 to 14) show examples of connections to commonly used decoder and digital filter ICs. The digital interface part is shown only, for clarity. The diagrams are for guidance purposes only - **no** guarantee for industrial exploitation is implied.



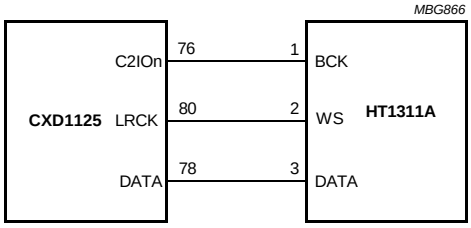
remark: SCSLn – signal SM5807 both "L" and "H" supported by TDA1311A and TDA1311AT

Fig.8 NPC SM5807 digital filter (4FS).



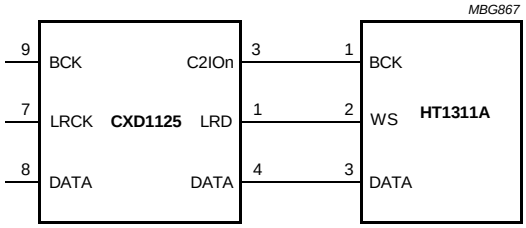
OMODn pin 19: "L" for 4FS operation
(1) versions A/B/G

Fig.9 NPC SM5840 digital filter (4FS).



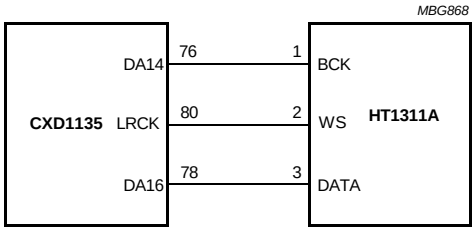
MODE SELECT:
MD1 pin 55: "L"
MD2 pin 56: "L" to use DOTX function
MD3 pin 57: "H"
PSSL pin 59: "L"
SLOB pin 58: "L"

Fig.10 Sony CXD1125 decoder (1FS).



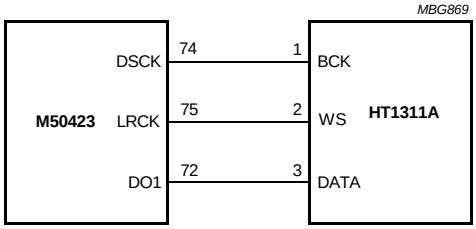
remark: CXD1162 input connectable to CXD1125
in the same way as for TDA1311A; AT to CXD1125

Fig.11 Sony CXD1162 digital filter (4FS).



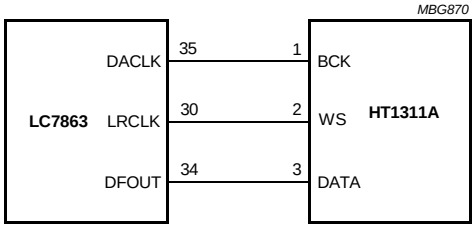
MODE SELECT:
MD1 pin 55: "L"
MD2 pin 56: "L" to use DOTX function
MD3 pin 57: "H" for 1FS; "L" for 2FS
PSSL pin 59: "L"
SLOB pin 58: "L"

Fig.12 Sony CXD1135 decoder (1FS) and digital filter (2FS).



MODE SELECT:
DOBSEL pin 7: "L"
DASEL1 pin 8: "H"
DASEL2 pin 9: "L"
DASEL3 pin 10: "H"
DASEL4 pin 11: "L"

Fig.13 Mitsubishi M50423 decoder (1FS) and digital filter (4FS).



MODE SELECT:
DFOFF pin 27: "L"
MSBF pin 38: "H"

Fig.14 Sanyo LC7863 decoder (1FS).

The following measurement graphs are performed on singular engineering samples; therefore **no** guarantee of typical parameter values is implied. Measurement conditions are typical, as stated in the section Characteristics, unless otherwise indicated. The normal measurement set-up includes a 20 kHz band-limiting filter for bandwidth definition, and an A-weighting filter where indicated.

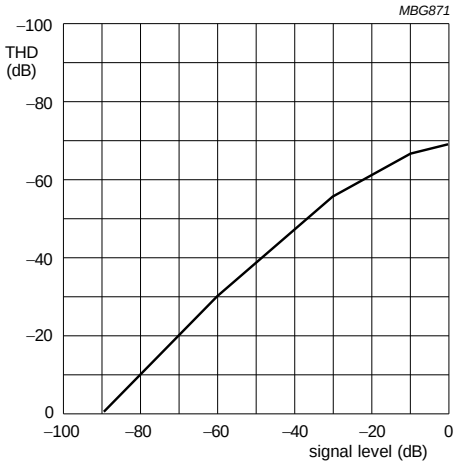
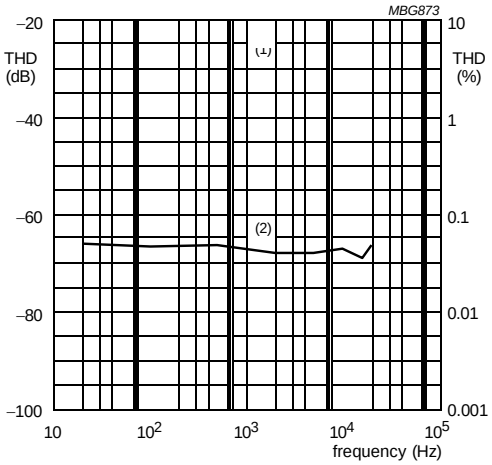
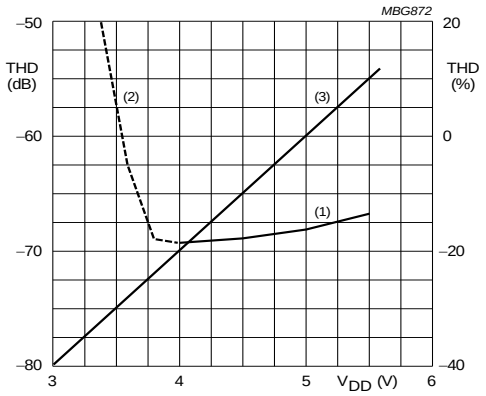


Fig.15 Total harmonic distortion plus noise as a function of signal level (4FS).



(1) Measured including all distortion plus noise at a signal level of −60 dB.
(2) Measured including all distortion plus noise at a signal level of 0 dB.

Fig.16 Total harmonic distortion plus noises as a function of frequency (4FS).

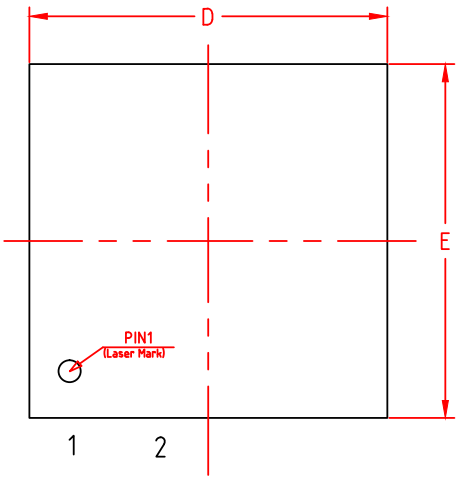


(1) Measured including all distortion plus noise within the specified operating supply voltage range.
(2) Measured including all distortion plus noise outside the specified operating supply voltage range.
(3) V_{FS} relative to nominal.

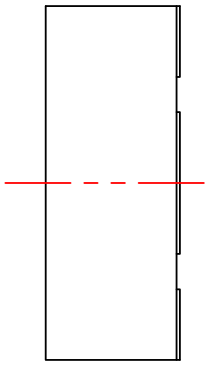
Fig.17 Total harmonic distortion plus noise as a function of supply voltage (4FS).

DFN8L(2X2X0.75-P0.50) 封装尺寸图

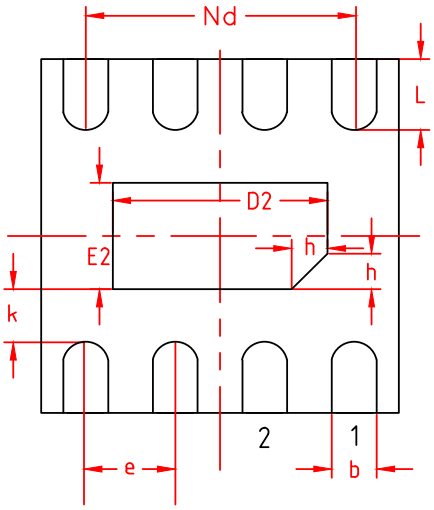
TOP VIEW
正视图



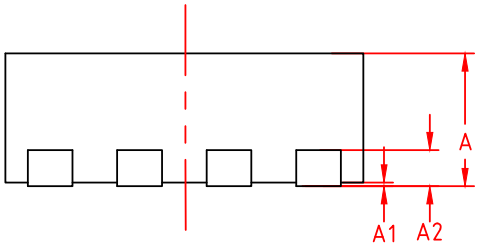
SIDE VIEW
侧视图



BOTTOM VIEW
背视图



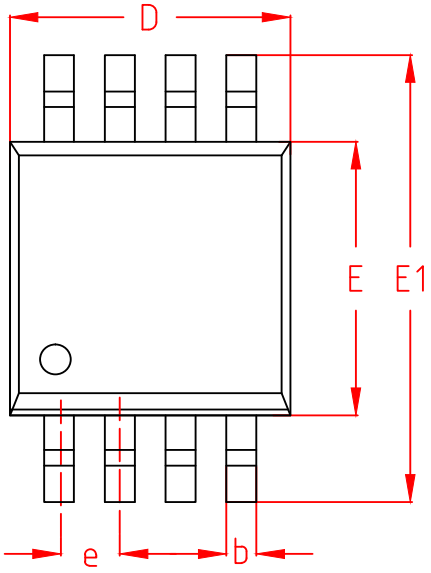
SIDE VIEW
侧视图



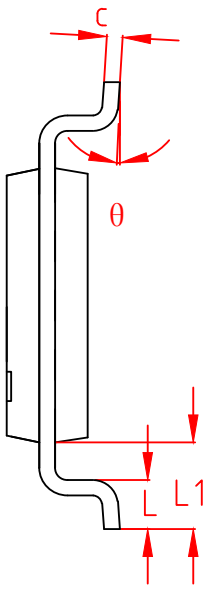
机械尺寸/mm			
字符 SYMBOL	最小值 MIN	典型值 NOMINAL	最大值 MAX
A	0.70	0.75	0.80
A1	-	0.02	0.05
A2	0.203 REF		
b	0.20	0.25	0.30
D	1.90	2.00	2.10
D2	1.10	1.20	1.30
E	1.90	2.00	2.10
E2	0.60	0.70	0.80
e	0.50 BSC		
K	0.25	0.30	0.35
L	0.30	0.35	0.40
h	0.15	0.20	0.25
Nd	1.50 BSC		

MSOP8 封装尺寸图

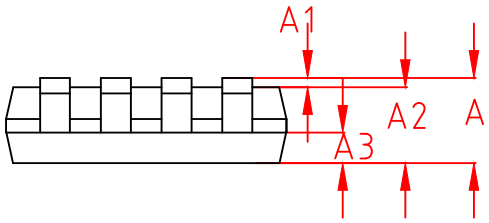
TOP VIEW
正视图



SIDE VIEW
侧视图



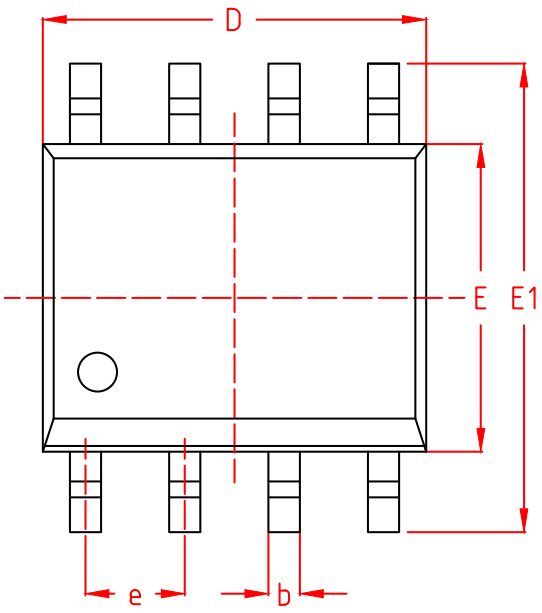
SIDE VIEW
侧视图



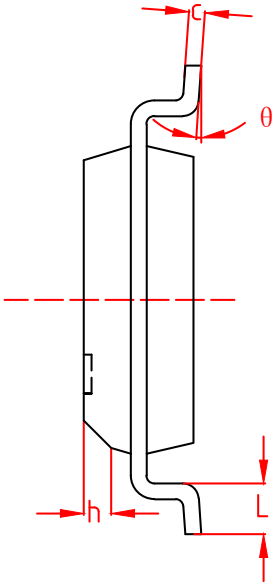
机械尺寸/mm Dimensions			
字符 SYMBOL	最小值 MIN	典型值 NOMINAL	最大值 MAX
A	–	–	1.10
A1	0.05	–	0.15
A2	0.75	0.85	0.95
A3	0.30	0.35	0.40
b	0.28	–	0.36
c	0.15	–	0.19
D	2.90	3.00	3.10
E	2.90	3.00	3.10
E1	4.70	4.90	5.10
e	0.65 BSC		
L1	0.95 REF		
L	0.40	–	0.70
θ	0°	–	8°

SOP8 封装尺寸图

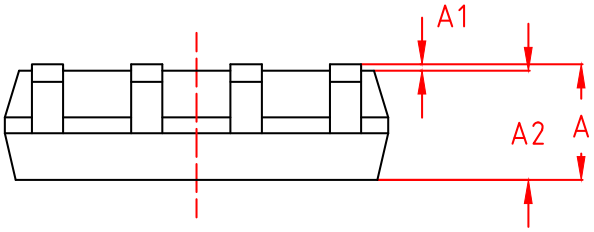
TOP VIEW
正视图



SIDE VIEW
侧视图



SIDE VIEW
侧视图



机械尺寸/mm Dimensions			
字符 SYMBOL	最小值 MIN	典型值 NOMINAL	最大值 MAX
A	–	–	1.75
A1	0.10	0.15	0.25
A2	1.30	1.40	1.50
b	0.35	–	0.50
c	0.19	–	0.25
D	4.80	4.90	5.00
E	3.80	3.90	4.00
E1	5.80	6.00	6.20
e	1.27 BSC		
h	0.25	–	0.45
L	0.50	–	0.80
θ	0°	–	8°