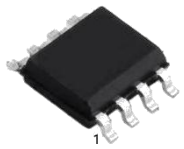
# 2A,40V,500KHz, Synchronous Step-Down DC/DC Converter

## FEATURES




ESOP-8


SOT-23-6

- 4.75V to 40V input voltage
- Output adjustable from 0.8V to 24V
- Output current up to 2A
- Integrated 170mΩ/135mΩ power MOSFET switches
- Shutdown current 5μA typical
- Efficiency up to 93%
- Fixed frequency 500KHz
- PFM mode in light load
- Internal soft start
- Over current protection and Hiccup
- Over temperature protection

## ORDERING INFORMATION

| DEVICE | Package Type | MARKING | Packing | Packing Qty |
|---|---|---|---|---|
| MP1482AME/TR-HG | ESOP-8 | MP1482A,1482A | REEL | 2500pcs/reel |
| MP1482AM6/TR-HG | SOT-23-6 | 1482A | REEL | 3000pcs/reel |

## DESCRIPTION

The MP1482A is high-frequency, synchronous, rectified, step-down, switch-mode converter with internal power MOSFETs. It offers a very compact solution to achieve a 2A continuous output current over a wide input supply range, with excellent load and line regulation.

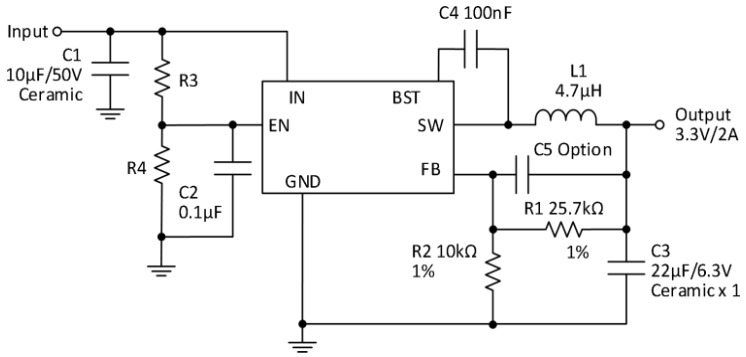
The MP1482A has synchronous-mode operation for higher efficiency over the output current-load range. Current-mode operation provides fast transient response and eases loop stabilization. Protection features include over-current protection and thermal shutdown.

The MP1482A requires a minimal number of readily available, standard external components and are available in ESOP-8 and SOT23-6 package.

## APPLICATIONS

- Distributed power systems
- Soundbar
- Industry Application
- Automotive

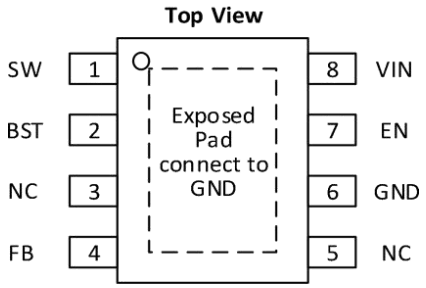
## TYPICAL APPLICATION



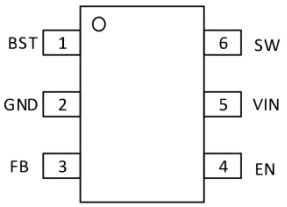


**EFFICIENCY**

## PIN CONFIGURATION AND FUNCTIONS



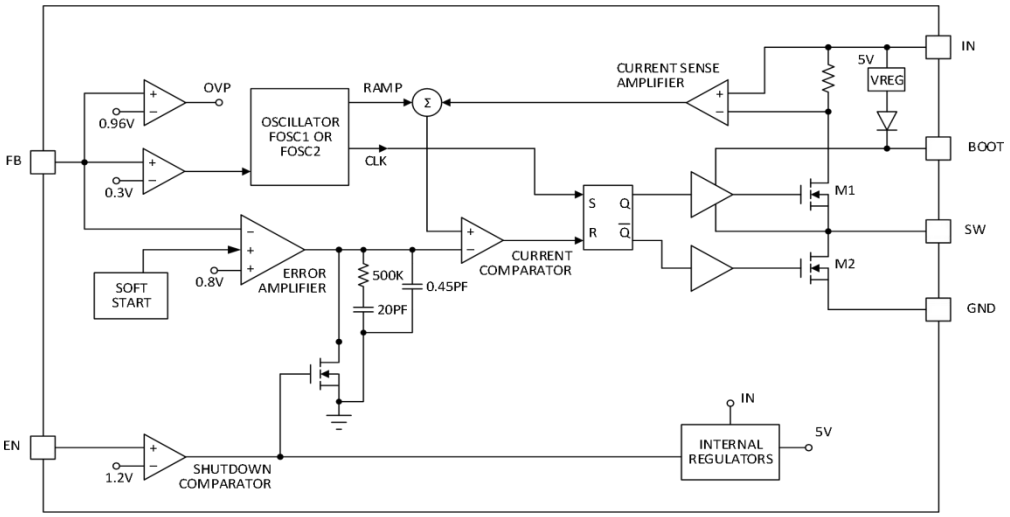

ESOP-8




SOT-23-6

| Pin | | Symbol | Description |
|---|---|---|---|
| ESOP8 | SOT23 | | |
| 1 | 6 | SW | SW is the switching node that supplies power to the output. Connect the output LC filter from SW to the output load. |
| 2 | 1 | BST | Bootstrap pin for top switch. A 0.1uF or larger capacitor should be connected between this pin and the SW pin to supply current to the top switch and top switch driver. |
| 3 | - | NC | Not connected. |
| 4 | 3 | FB | Output feedback pin. FB senses the output voltage and is regulated by the control loop to 0.8V. Connect a resistive divider at FB. |
| 5 | - | NC | Not connected. |
| 6 | 2 | GND | Ground. |
| 7 | 4 | EN | Drive EN pin high to turn on the regulator and low to turn off the regulator. |
| 8 | 5 | VIN | Input voltage pin. VIN supplies power to the IC. Connect a 4.75V to 40V supply to VIN and bypass VIN to GND with a suitably large capacitor to eliminate noise on the input to the IC. |

## BLOCK DIAGRAM




**Functional Block Diagram**

## ABSOLUTE MAXIMUM RATINGS

| Parameter | Parameter | Rating | UNIT |
|---|---|---|---|
| $V_{IN}$&$V_{EN}$ | Supply Voltage | -0.3V to 44V | V |
| $V_{SW}$ | Switch Node | –0.3V to $V_{IN}$+0.3V | V |
| $V_{BST}$ | Boost | $V_{SW}$–0.3V to $V_{SW}$+6V | V |
| V | All Other Pins | –0.3V to +6V | V |
| $T_J$ | Junction Temperature | +150 | °C |
| $T_{STG}$ | Storage Temperature Range | –65 to +150 | °C |
| $T_L$ | Lead Temperature (Soldering, 10 sec) | +260 | °C |

**NOTE:**Stresses above those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

## RECOMMENDED OPERATING CONDITIONS

| Parameter | Parameter | Rating | UNIT |
|---|---|---|---|
| $V_{IN}$ | Supply Voltage | -0.3V-40V | V |
| $V_{OUT}$ | Switch Node | –0.3V to VIN+0.3V | V |
| $T_{OP}$ | Operating Temperature Range | –40 to +125 | °C |

## PACKAGE THERMAL CHARACTERISTICS

| Parameter | Parameter | Rating | UNIT |
|---|---|---|---|
| $\theta_{JA}$ | Thermal Resistance | 50 | °C/W |
| $\theta_{JC}$ | Thermal Resistance | 10 | °C/W |

## ELECTRICAL CHARACTERISTICS

| PARAMETER | Symbol | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| Supply Voltage | $V_{IN}$ | | 4.75 | | 40 | V |
| Output Voltage | $V_{OUT}$ | | 0.8 | | 24 | V |
| Shutdown Supply Current | | $V_{EN}$ = 0V | | 5 | 6 | μA |
| Supply Current | | $V_{EN}$ = 2.0V, $V_{FB}$ = 1V | | 0.09 | | mA |
| Feedback Voltage | $V_{FB}$ | 4.75V ≤ $V_{IN}$≤ 40V | 0.785 | 0.8 | 0.815 | V |
| Feedback Over-voltage Threshold | | | | 0.96 | | V |
| High-Side Switch-On Resistance * | $R_{DS(ON)1}$ | | | 170 | | mΩ |
| Low-side Switch-On Resistance * | $R_{DS(ON)2}$ | | | 130 | | mΩ |
| High-Side Switch Leakage Current | | $V_{EN}$ = 0V, $V_{SW}$ = 0V, $T_A$ = +125°C | | | 10 | μA |
| Upper Switch Current Limit | | Minimum Duty Cycle | 2.5 | 3.0 | | A |
| Lower Switch Current Limit | | From Drain to Source | | 0 | | A |
| Oscillation Frequency | $F_{OSC1}$ | | 400 | 500 | 600 | KHz |
| Short Circuit Oscillation Frequency | $F_{OSC2}$ | $V_{FB}$ = 0V | 100 | 250 | 150 | KHz |
| Maximum Duty Cycle | $D_{MAX}$ | $V_{FB}$ = 0.5V | | 90 | | % |
| Minimum On Time * | | | | 80 | | ns |
| EN Falling Threshold Voltage | | $V_{EN}$ Falling | | 1.1 | | V |
| EN Rising Threshold Voltage | | $V_{EN}$ Rising | | 1.2 | | V |
| Input Under Voltage Lockout Threshold | | $V_{IN}$ Rising | | 4.2 | | V |
| Input Under Voltage Lockout Threshold Hysteresis | | | | 200 | | mV |
| Soft-Start Period | | | | 1 | | ms |
| Thermal Shutdown * | | | | 150 | | °C |

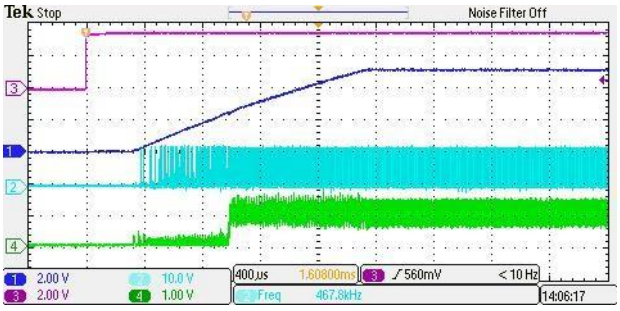
NOTE: * Guaranteed by design, not tested.

## TYPICAL CHARACTERISTICS

$V_{IN}$ = 12V, $V_O$ = 5V, L1 = 6.8μH, Cload=16μF,$T_A$ = +25°C, unless otherwise noted.

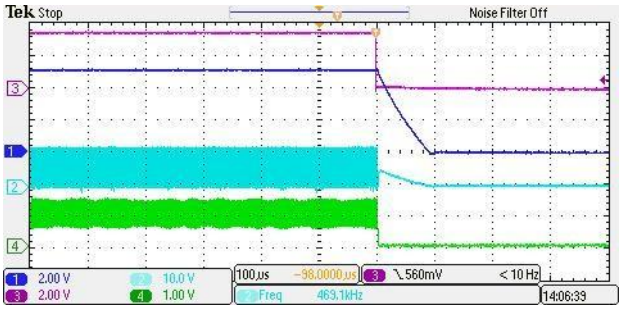
**Startup through Enable**

**VIN=12V,Vout=5V,Iout=1A(Resistive load)**

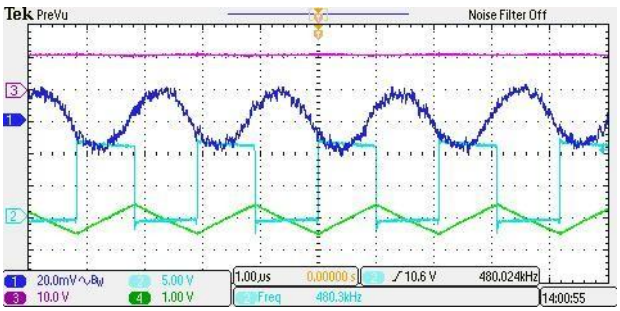



**Shutdown through Enable**

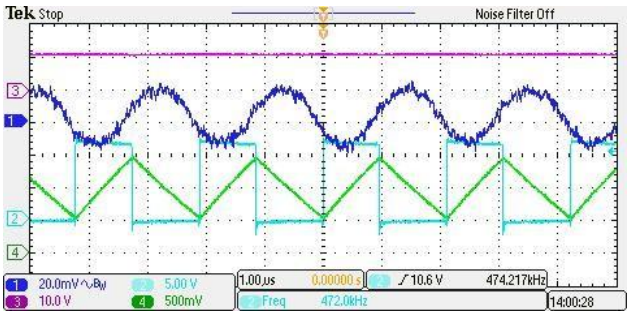
**VIN=12V,Vout=5V,Iout=1A(Resistive load)**



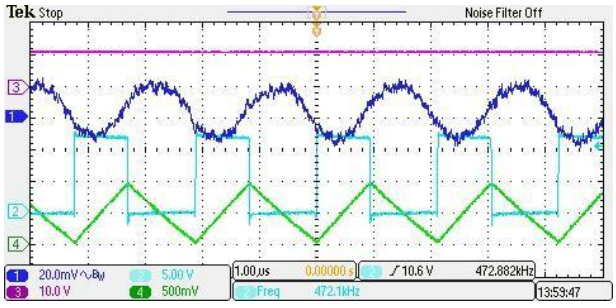

**Heavy Load Operation(2A LOAD)**



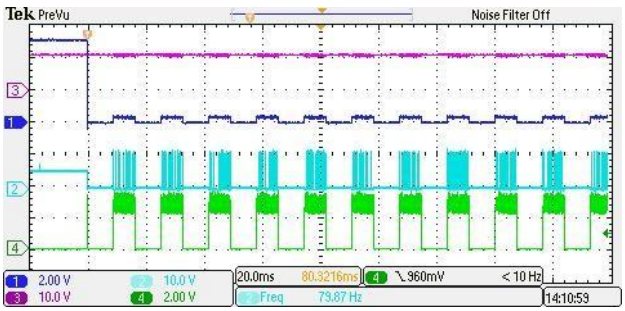

**Medium Load Operation(1A LOAD)**



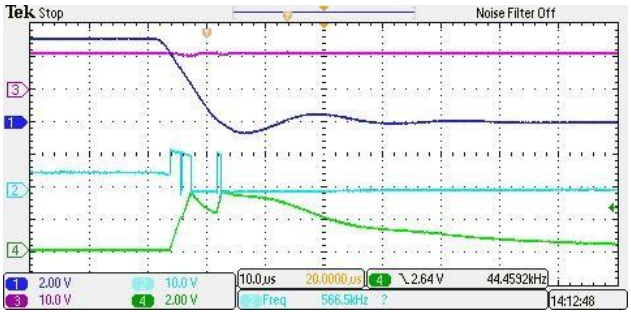

**Light Load Operation(0.5A LOAD)**



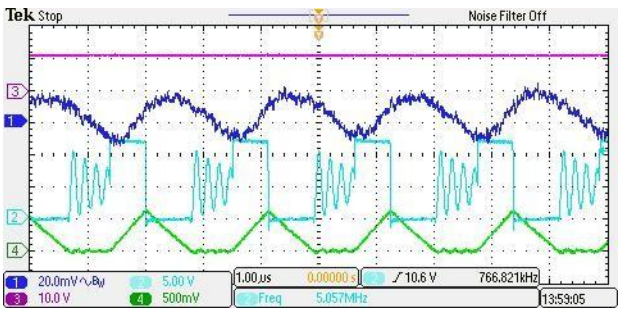

**Short&Hiccup Protection**



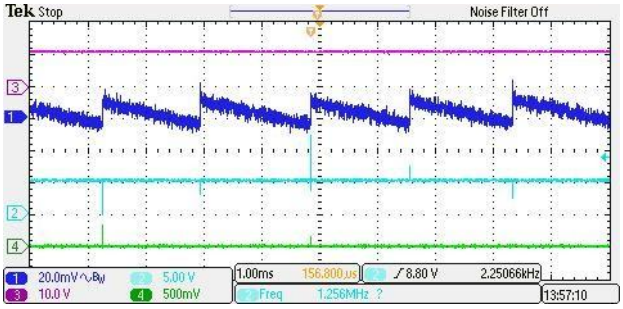

**Short Circuit Protection**



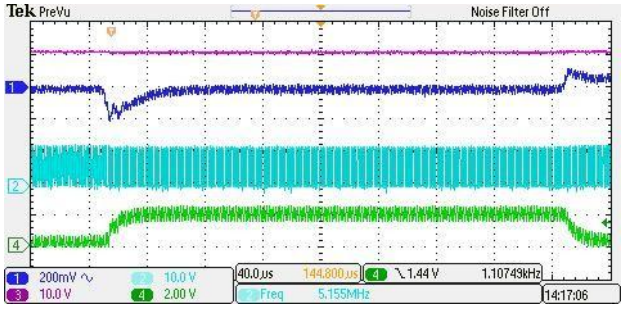

**Output Ripple(12V=>5V,Load=0.2A)**



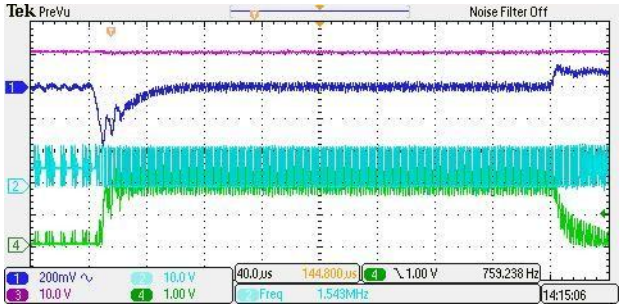
**Output Ripple(12V=>5V,Load=0A)**



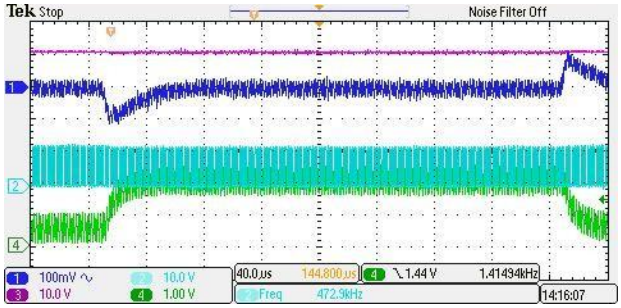

**Load Transient(0.2A--2A Load)**




**Load Transient(0.05A--2A Load)**




**Load Transient(0.5A--2A Load)**




# OPERATION

The MP1482A is 500KHz, synchronous, step down, switching regulator with integrated high side and low-side power MOSFETs. The MP1482A provides an internally compensated, highly efficient output of up to 2A with current mode control and also features a wide input voltage range, internal soft-start control, and a precision current limit. Its very low operational quiescent current makes it suitable for battery powered applications.

**Pulse-Width Modulation (PWM) Control**

At moderate-to-high output currents, the MP1482A operates in a fixed-frequency, peak current-control mode to regulate the output voltage. A pulse-width modulation (PWM) cycle initiated by the internal clock turns on the power high-side MOSFET (HS-FET). The HS-FET remains on until its current reaches the value set by the COMP voltage (VCOMP). After the HS FET is off, the low-side MOSFET (LS-FET) turns on, and the inductor current flows through

the LS-FET. To avoid a shoot-though, a dead time is inserted to prevent the HS-FET and LS FET from turning on at the same time. For each turn-on and turn-off in a switching cycle, the HS-FET turns on and off with a minimum on and off time limit. To prevent inductor current and output voltage runaway, the switching frequency folds back when the HS-FET minimum turn-on is detected internally. When the PWM signal goes low, the HS-FET turns off and remains off for at least 160ns before the next cycle begins. If the current in the HS-FET does not reach the COMP-set current value within one PWM cycle, the HS FET remains on to avoid a turn-off operation.

**Pulse-Frequency Mode (PFM)**

Under light-load conditions, the MP1482A enters pulse-frequency mode (PFM) to improve efficiency. PFM is triggered when VCOMP drops below the internal sleep threshold, which generates a pause command to block the turn on clock pulse, so the power MOSFET does not turn on. This reduces gate driving and switching losses. The pause command causes the entire chip to enter sleep mode, reducing the quiescent current to improve light-load efficiency. When VCOMP exceeds the sleep threshold, the pause signal resets, and the chip resumes normal PWM operation. Whenever the pause command changes from low to high, the PWM signal goes high immediately and turns on the power MMOSFET.

**Under-Voltage Lockout (UVLO)**

VIN under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The UVLO rising threshold is approximately 4.6V, while its falling threshold is 3.9V.

**Enable Control (EN)**

The MP1482A has a dedicated enable control pin (EN). When VIN rises above the threshold, EN can enable or disable the chip for high effective logic. Its falling threshold is 1.1V, and its rising threshold is about 1.2V. An internal 10MΩ resistor from EN to GND allows EN to be floated to shut down the chip. When the EN voltage is pulled to 0V, the chip enters the lowest shutdown current mode. When the EN voltage rises above 0V but remains below the rising threshold, the chip remains in shutdown mode with a slightly higher shutdown current.EN can directly connect to PVDD.

**Internal Soft Start (SS)**

A reference-type soft start (SS) prevents the converter output voltage from overshooting during start-up. When the chip starts up, the internal circuitry generates a soft-start voltage (VSS) that ramps up from 0V during the SS time. When VSS is lower than VREF, VSS overrides VREF as the error amplifier reference. The maximum VSS value isapproximately the same as VFB, so if VFB falls, the maximum of VSS falls. This accommodates short-circuit recovery. When the short circuit is removed, VSS ramps up to prevent an output voltage overshoot.

**Thermal Shutdown**

Thermal shutdown prevents thermal runaway. When the silicon die temperature exceeds its upper threshold, the entire chip shuts down. When the temperature drops below its lower threshold, the chip is enabled again.

**Floating Driver and Bootstrap Charging**

The floating power MOSFET driver is powered by an external bootstrap capacitor. This floating driver has its own UVLO protection with a rising threshold of about 2.7V and a falling threshold of about 300mV. During UVLO, VSS resets to zero. When the UVLO ends, the controller enters soft start. The bootstrap capacitor is charged and regulated to about 5V by the dedicated internal bootstrap regulator. When the voltage between the BST and SW nodes falls below its regulation, a PMOS pass transistor connected from VIN to BST turns on. The charging current path goes from VIN to BST to SW. The external circuit must provide enough voltage headroom to facilitate the charging.

**Current Comparator and Current Limit**

A current-sense MOSFET senses the power MOSFET current. This current is input to the high-speed current comparator for current mode control. When the power MOSFET turns on, the comparator is first blanked to limit noise, and then compares the power switch current against VCOMP. When the sensed value exceeds VCOMP, the comparator output goes low to turn off the power MOSFET. The maximum current of the internal power MOSFET is limited cycle by-cycle internally. The switching frequency folds back to prevent an inductor current runaway during start-up or a short circuit.

**Start-Up and Shutdown**

If both VIN and VEN exceed their respective thresholds, the chip starts up. The reference block first starts to generate a stable reference voltage and current, and then the internal regulator starts to provide a stable supply for the rest of the circuit. While the internal supply rail is up, an internal timer turns the power MOSFET off for about 50μs to blank any start-up noise. When the internal soft-start block is enabled, it first holds its SS output low to ensure that the rest of the circuit is ready before ramping up.

Three events can shut down the chip: EN low, VIN low, and thermal shutdown. During the shutdown procedure, the signaling path is blocked first to avoid any fault triggering. VCOMP and the internal supply rail are then pulled low. The floating driver is not subject to this shutdown command, but its charging path is disabled.

## APPLICATION INFORMATION

### OVERVIEW

The MP1482A is synchronous rectified, current-mode, step-down regulator. It regulates input voltages from 4.75V to 40V down to an output voltage as low as 0.8V to 24V, and supplies up to 2A of load current.

The MP1482A uses current-mode control to regulate the output voltage. The output voltage is measured at FB through a resistive voltage divider and amplified through the internal trans-conductance error amplifier. The converter uses internal N-Channel MOSFET switches to step-down the input voltage to the regulated output voltage. Since the high side MOSFET requires a gate voltage greater than the input voltage, a boost capacitor connected between SW and BOOT is needed to drive the high side gate. The boost capacitor is charged from the internal 5V rail when SW is low.

The MP1482A has power save mode for light load. During this time, the internal clock is blocked,thus the MP1482A reduces the frequency of pulses sent to the switches to achieve power saving through PFM mode.When the MP1482A FB pin exceeds 20% of the nominal regulation voltage of Vref, the over voltage comparator is tripped, forcing the high-side switch off.

### SETTING THE OUTPUT VOLTAGE

The external resistor divider sets the output voltage. The feedback resistor R2 also sets the feedback-loop bandwidth through the internal compensation capacitor (see the Typical Application circuit). Choose R2 around 10kΩ, and R1 by:

$$R2 = R1 / (V_{OUT}/V_{ref} - 1)$$

Use a network below for when $V_{OUT}$ is low.

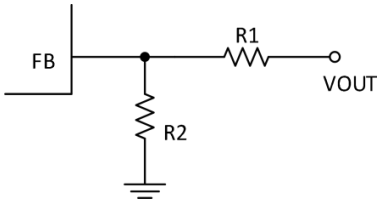



**Figure 1: Network.**

| VOUT | R1 | R2 |
|---|---|---|
| 1.8V | 12.5KΩ(1%) | 10KΩ(1%) |
| 2.5V | 21.5KΩ(1%) | 10KΩ(1%) |
| 3.3V | 39KΩ(1%) | 12.5KΩ(1%) |
| 5V | 52.5KΩ(1%) | 10KΩ(1%) |
| 12V | 140KΩ(1%) | 10KΩ(1%) |
| 24V | 290KΩ(1%) | 10KΩ(1%) |
| 36V | 440KΩ(1%) | 10KΩ(1%) |

**INDUCTOR**

The inductor is required to supply constant current to the output load while being driven by the switched input voltage. A larger value inductor will result in less ripple current that will result in lower output ripple voltage. However, the larger value inductor will have a larger physical size, higher series resistance, and/or lower saturation current. A good rule for determining，the inductance to use is to allow the peak-to-peak ripple current in the inductor to be approximately 30% of the maximum switch current limit. Also, make sure that the peak inductor current is below the maximum switch current limit. The inductance value can be calculated by:

$$L = [ V_{OUT} / (f_S \times \Delta I_L) ] \times (1 - V_{OUT}/V_{IN} )$$

Where $V_{OUT}$ is the output voltage, $V_{IN}$ is the input voltage, $f_S$ is the switching frequency, and $\Delta I_L$ is the peak-to-peak inductor ripple current.

Choose an inductor that will not saturate under the maximum inductor peak current. The peak inductor current can be calculated by:

$$ILP = I_{LOAD} + [ V_{OUT} / (2 \times f_S \times L) ] \times (1 - V_{OUT}/V_{IN})$$

Where $I_{LOAD}$ is the load current.

The choice of which style inductor to use mainly depends on the price vs. size requirements and any EMI requirements.

**INPUT CAPACITOR**

The input current to the step-down converter is discontinuous, therefore a capacitor is required to supply the AC current to the step-down converter while maintaining the DC input voltage. Use low ESR capacitors for the best performance. Ceramic capacitors are preferred, but tantalum or low-ESR electrolytic capacitors may also suffice. Choose X5R or X7R dielectrics when using ceramic capacitors.

Since the input capacitor (C1) absorbs the input switching current it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated by:

$$I_{C1} = I_{LOAD} \times [ (V_{OUT}/V_{IN}) \times (1 - V_{OUT}/V_{IN}) ]1/2$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, where $I_{C1} = I_{LOAD}/2$. For simplification, choose the input capacitor whose RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum or ceramic. When using electrolytic or tantalum capacitors, a small, high quality ceramic capacitor, i.e. 0.1μF, should be placed as close to the $I_C$ as possible. When using ceramic capacitors, make sure that they have enough capacitance to provide sufficient charge to prevent excessive voltage ripple at input. The input voltage ripple for low ESR capacitors can be estimated by:

$$\Delta V_{IN} = [ I_{LOAD}/(C_1 \times f_S) ] \times (V_{OUT}/V_{IN}) \times (1 - V_{OUT}/V_{IN})$$

Where C1 is the input capacitance value.

**OUTPUT CAPACITOR**

The output capacitor is required to maintain the DC output voltage. Ceramic, tantalum, or low ESR electrolytic capacitors are recommended. Low ESR capacitors are preferred to keep the output voltage ripple low. The output voltage ripple can be estimated by:

$$\Delta V_{OUT} = [\ V_{OUT}/(f_S \times L)\ ] \times (1 - V_{OUT}/V_{IN}) \times [\ R_{ESR} + 1 / (8 \times f_S \times C2)\ ]$$

Where C2 is the output capacitance value and RESR is the equivalent series resistance (ESR) value of the output capacitor.

In the case of ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is mainly caused by the capacitance. For simplification, the output voltage ripple can be estimated by:

$$\Delta V_{OUT} = [\ V_{OUT}/(8 \times f_{S2} \times L \times C2)\ ] \times (1 - V_{OUT}/V_{IN})$$

In the case of tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated to:

$$\Delta V_{OUT} = [\ V_{OUT}/(f_S \times L)\ ] \times (1 - V_{OUT}/V_{IN}) \times R_{ESR}$$

The characteristics of the output capacitor also affect the stability of the regulation system.

**EXTERNAL BOOTSTRAP DIODE**

An external bootstrap diode may enhance the efficiency of the regulator, the applicable conditions of external BOOT diode are:

- $V_{OUT}$ = 5V or 3.3V; and
- Duty cycle is high: D = $V_{OUT}/V_{IN}$ > 65%

In these cases, an external BOOT diode is recommended from the output of the voltage regulator to BOOT pin, as shown in Figure 2.

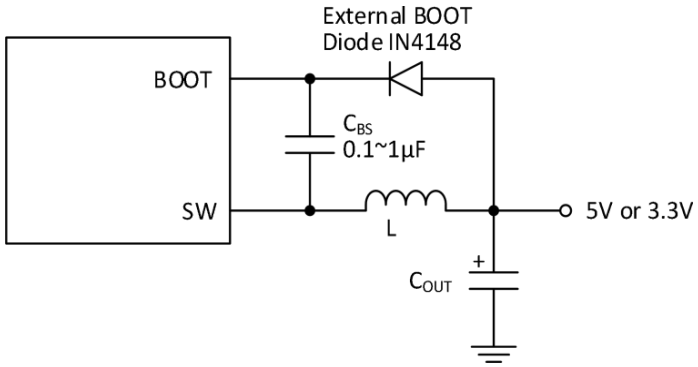


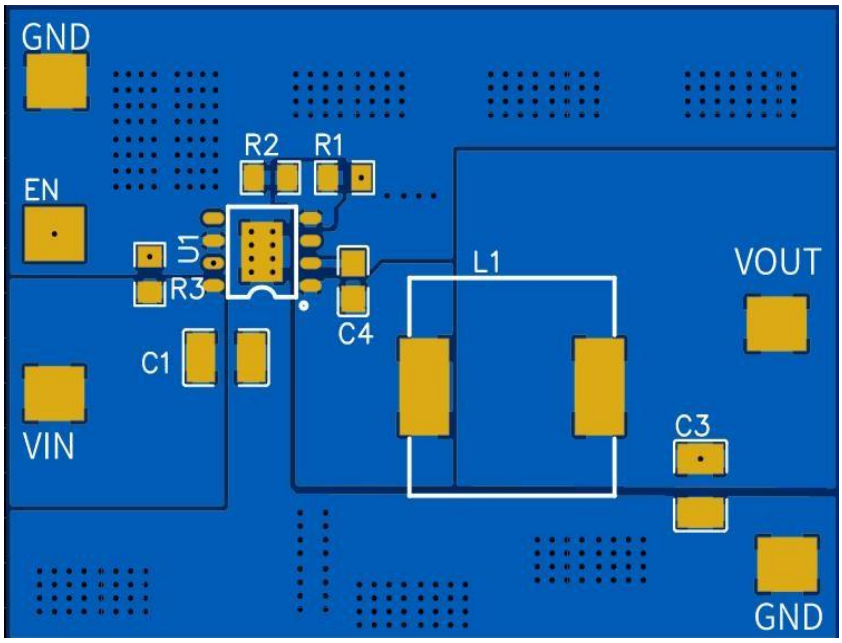

**Figure 2: Add optional external bootstrap diode to enhance efficiency.**

The recommended external BOOT diode is IN4148, and the BOOT capacitor is 0.1~1μF.

## LAYOUT

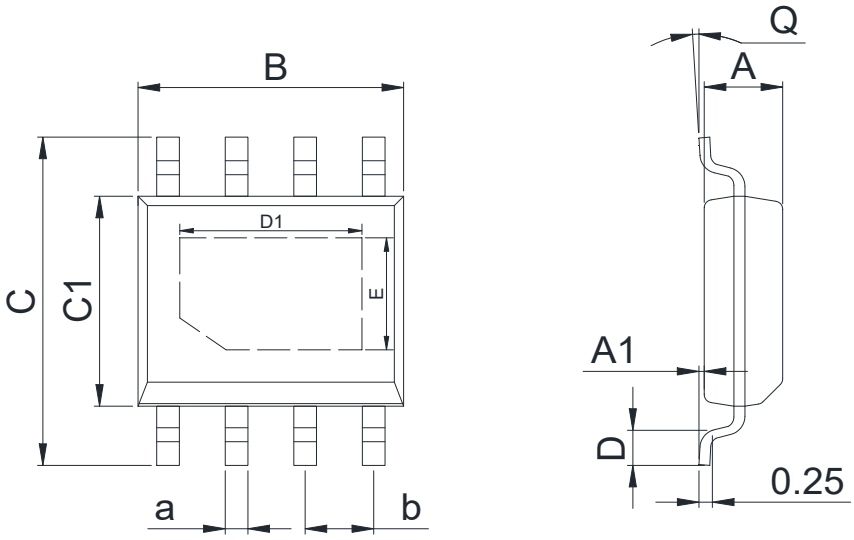
PCB layout is very important to achieve stable operation. Please follow the guidelines below.

1) Keep the path of switching current short and minimize the loop area formed by Input capacitor, high-side MOSFET and low-side MOSFET.
2) Bypass ceramic capacitors are suggested to be put close to the VIN Pin.
3) Ensure all feedback connections are short and direct. Place the feedback resistors and compensation components as close to the chip as possible.
4) Rout SW away from sensitive analog areas such as FB.
5) Connect IN, SW, and especially GND respectively to a large copper area to cool the chip to improve thermal performance and long-term reliability.
6) It is recommended to reserve a place for CFF in layout.



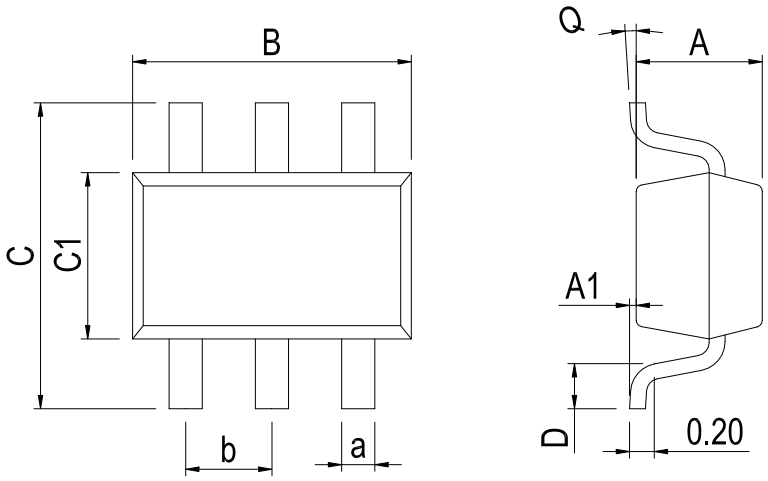
## Physical Dimensions

ESOP-8




| Dimensions In Millimeters(ESOP-8) | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Symbol:** | **A** | **A1** | **B** | **C** | **C1** | **D** | **D1** | **E** | **Q** | **a** | **b** |
| **Min:** | 1.35 | 0.05 | 4.90 | 5.80 | 3.80 | 0.40 | 3.20 | 2.31 | 0° | 0.35 | 1.27 BSC |
| **Max:** | 1.55 | 0.20 | 5.10 | 6.20 | 4.00 | 0.80 | 3.40 | 2.51 | 8° | 0.45 | |

SOT-23-6




| Dimensions In Millimeters(SOT-23-6) | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| **Symbol:** | A | A1 | B | C | C1 | D | Q | a | b |
| **Min:** | 1.00 | 0.00 | 2.82 | 2.65 | 1.50 | 0.30 | 0° | 0.30 | 0.95 BSC |
| **Max:** | 1.15 | 0.15 | 3.02 | 2.95 | 1.70 | 0.60 | 8° | 0.50 | |

## Revision History

| REVISION NUMBER | DATE | REVISION | PAGE |
|---|---|---|---|
| V1.0 | 2018-11 | New | 1-15 |
| V1.1 | 2025-1 | Document Reformatting | 1-15 |
| V1.2 | 2025-8 | Add marking content | 1 |
| V1.3 | 2025-12 | Update important statements | 15 |

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