钍地半导体
Tudi Semiconductor

Product Specification

TUDI-TJA1050

High speed CAN transceiver

网址 www.sztdbdt.com

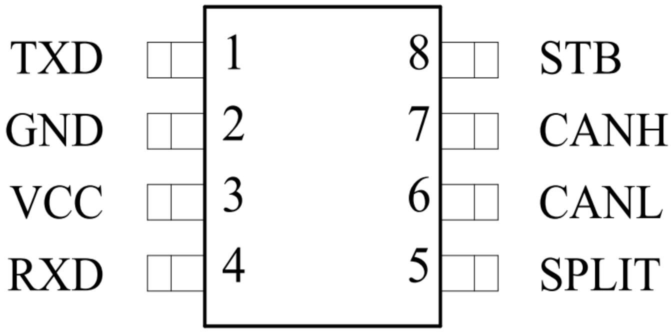
用芯智造·卓越品质

semiconductor device manufacturer

- Design
- research and development
- production
- and sales

Features

- Fully compatible with the “ ISO 11898 ” standard
- High speed (up to 1 Mbaud)
- Very low ElectroMagnetic Emission (EME)
- Differential receiver with wide common-mode range for high ElectroMagnetic Immunity (EMI)
- An unpowered node does not disturb the bus lines
- Transmit Data (TXD) dominant time-out function
- Silent mode in which the transmitter is disabled
- Bus pins protected against transients in an automotive environment
- Input levels compatible with 3.3 V and 5 V devices
- Thermally protected
- Short-circuit proof to battery and to ground
- At least 110 nodes can be connected.



Pin Diagram

Description

The TJA1050 is the interface between the Controller Area Network (CAN) protocol controller and the physical bus. The device provides differential transmit capability to the bus and differential receive capability to the CAN controller.
The TJA1050 most important differences are:

- Much lower electromagnetic emission due to optimal matching of the output signals CANH and CANL
- Improved behaviour in case of an unpowered node
- No standby mode.

This makes the TJA1050 eminently suitable for use in nodes that are in a power-down situation in partially powered networks.

Applications

- automotive electronics

Pin description

Pin Number	Symbol	Functional description
I	TXD	Send Data Input
2	GND	The earth
3	VCC	Source
4	RXD	Receive Data Output
5	SPLIT	Common-mode regulated output
6	CANL	Low-level CAN bus
7	CANH	High-level CAN bus
8	STB	Standby Mode Control Input

Block diagram

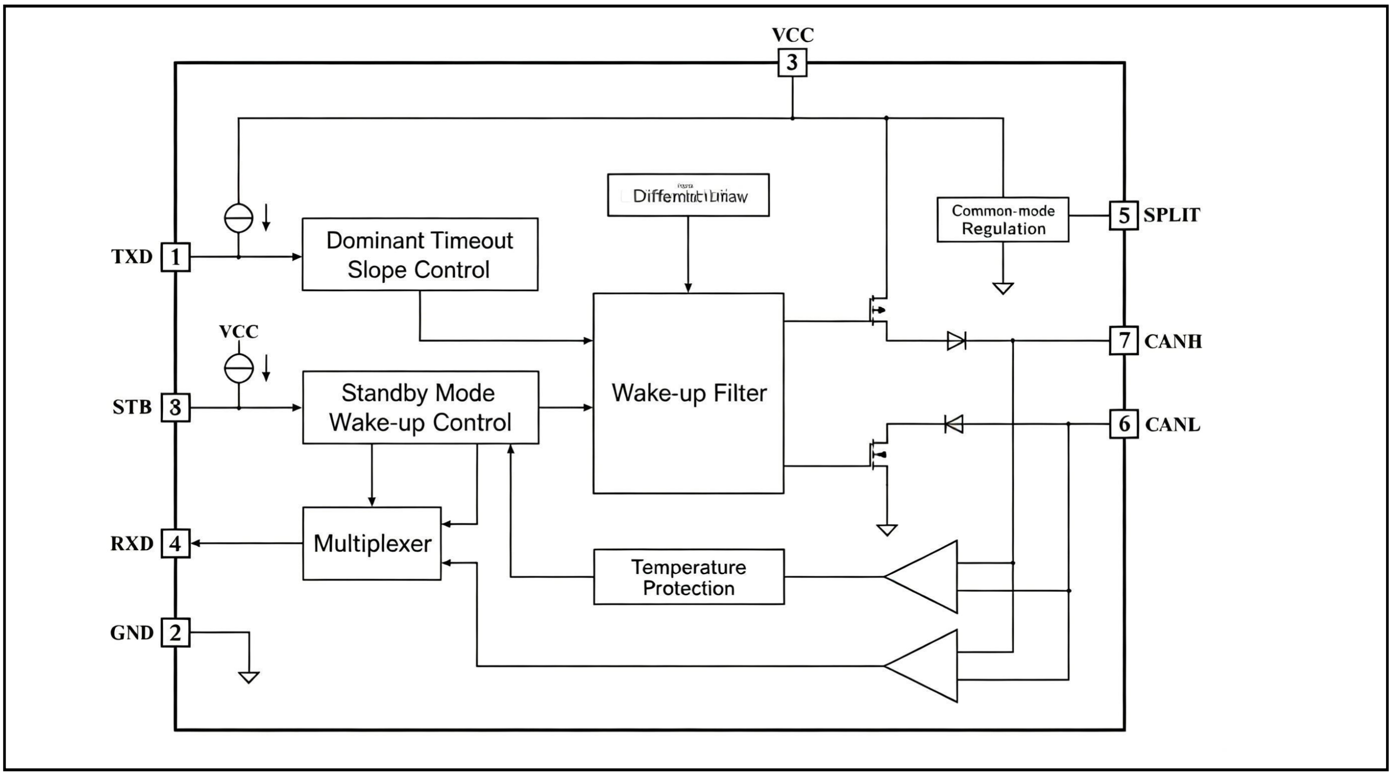


Figure 1 Functional Block Diagram

Typical Application Circuit Diagram

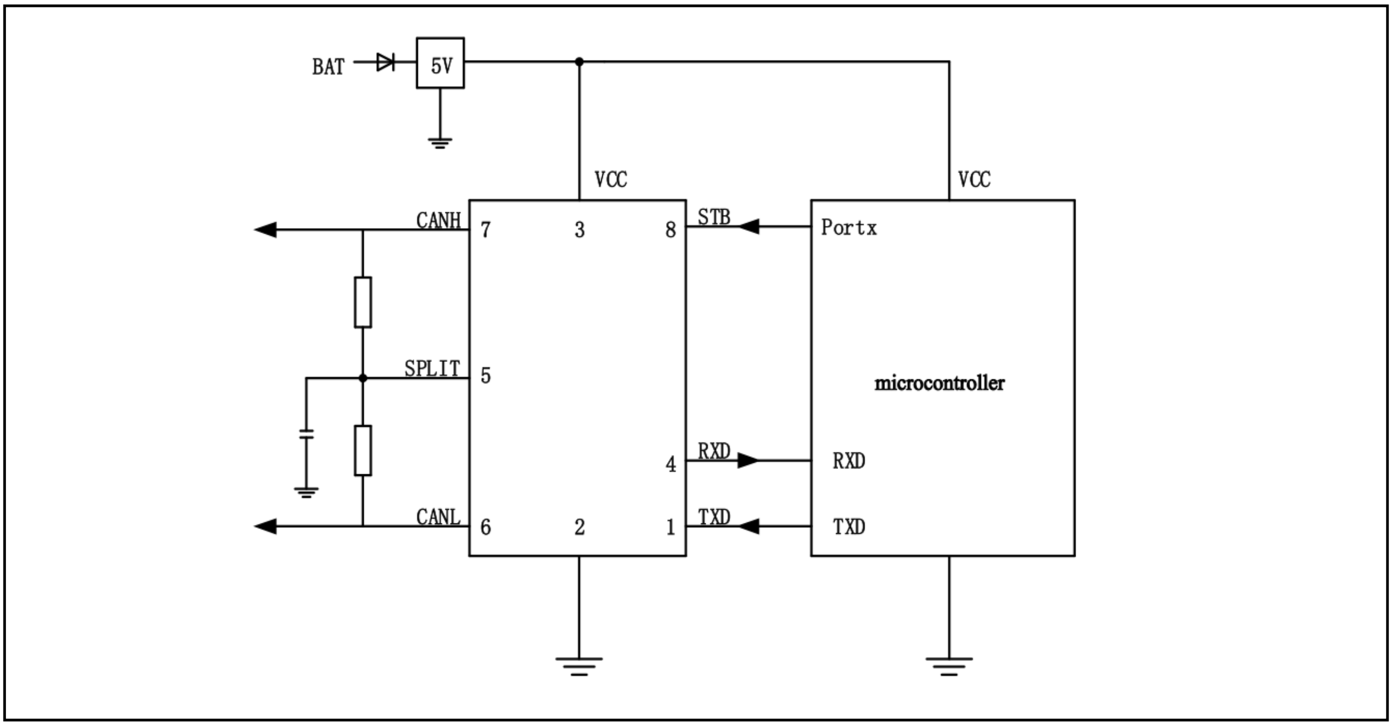


Figure 2 Typical Applications of a 5V Microcontroller

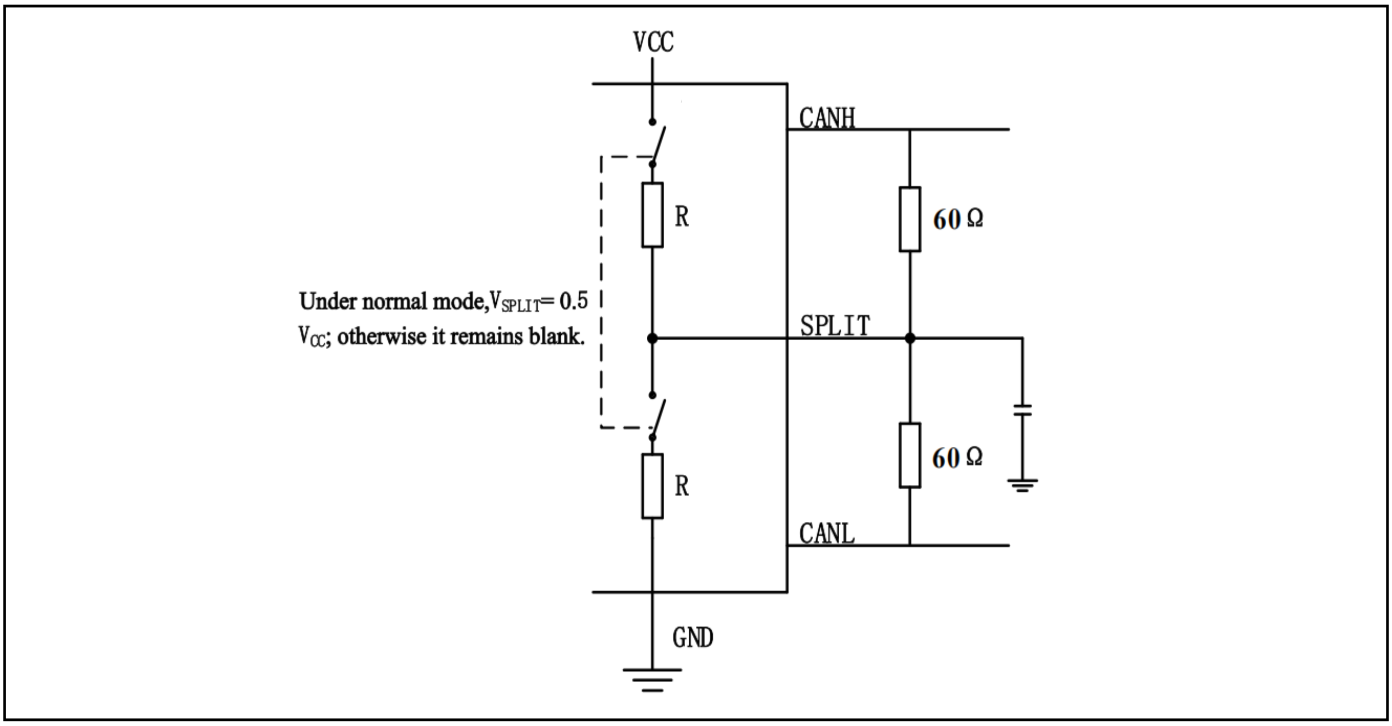


Figure 3 Common-Mode Voltage Regulation Application

Maximum rated value(unless otherwise specified,T_A=25°C

Project	Symbol	Condition	Scale	Unit
Supply voltage	V_{CC}	No time restrictions	-0.3～6	V
		Working range	4.75~5.25	V
DC voltage on the CANH pin	V_{CANH}	0<Vcc<5.25V with no time limit	-27～40	V
DC voltage on the CANL pin	V_{CANL}			
DC voltage on the SPLIT pin	V_{SPLIT}			
DC voltage on the TXD pin	V_{TXD}		-0.3～Vcc+0.3	V
DC voltage on the RXD pin	V_{RXD}			
DC voltage on the STB pins	V_{STB}			
Electrostatic discharge voltage	V_{ESD}	Human Model,Note 1	-8～8	kV
		Machine Model,Note 2	-300～300	V
		Model of Electrical Components	-2～2	kV
Storage Temperature	T_{STG}		-55～150	℃
Actual fusion temperature	T_{VJ}	Note 3	-40～150	℃

NOTE:

1. Equivalent to a 100pF capacitor discharging through a 1.5 kΩ resistor.
2. Equivalent to a 200pF capacitor discharging through a 0.75μH inductor and a 10Ω resistor.
3. According to the junction temperature of "IEC-6077-1", another definition of T_{VJ} is: T_{VJ}= T_{amb} P*R_{th}($_{VJ-amb}$), where R_{th}($_{VJ-amb}$) is a fixed used to calculate T_{VJ}, and the rated value of T_{VJ} limits the allowable combination of power dissipation (P) and ambient temperature (T_{amb}).
4. If the operating conditions the device exceed the maximum ratings mentioned above, permanent damage may be caused to the device. The above parameters are only the maximum values of the operating conditions, and we do not recommend the device outside this specification range. If the device operates under absolute maximum limit conditions for a long time, its stability may be affected.

Electrical characteristics

Unless otherwise specified, all typical values are measured under the conditions of T_A=25℃, V_{CC}=5V, T_{VJ}= -40~50℃, and R_L=60Ω. All voltages are referenced to ground, and the positive current direction is flowing into the IC.

Parameter declaration	Symbol	Test condition	Least value	Representative value	Crest value	Unit
Current Characteristics						
Dominant power supply current	$I_{cc(dom)}$	Normal mode:Dominant V_{TxD}=0V	30	50	70	mA
Implicit power supply current	$I_{cCreces)}$	Normal mode,recessive V_{TxD}=Vcc	2.5	5	10	mA
Standby power current	$I_{cc(stb)}$	Standby mode	5	10	20	μA
Short-circuit output current at pin CANH	$I_{o(CANH)(sc)}$	Normal mode V_{TXD}=0V,V_{CANH}=0V	-40	-70	-95	mA
Short-circuit output current at pin CANL	$I_{o(CANL)(sc)}$	Normal mode V_{TXD}=0V,V_{CANL}=40V	40	70	100	mA
Standby pin high-level input current	$I_{STB(H)}$	V_{STB}=Vcc	—	0	—	μA
Standby pin low-level input current	$I_{STB(L)}$	V_{STB}=0V	-1	-4	-10	μA
TXD Pin High-Level Input Current	$I_{TXD(H)}$	V_{TXD}=Vcc	-5	0	5	μA
Pin TXD low-level input current	$I_{TXD(L)}$	Normal mode:V_{TXD}=0V	-100	-200	-300	μA
Pin RXD high-level output current	$I_{RXDCH)}$	Normal mode V_{RXD}=Vcc-0.4V	-0.1	-0.4	-1	mA
Pin RXD low-level output current	$I_{RXD(L)}$	V_{RXD}=0.4V	2	6	12	mA
Implicit output current	$I_{o(reces)}$	-27V<VCAN<32V	-2.5	—	2.5	mA
CANH,CANL leakage current	$I_{leak(CAN)}$	Vcc=0V V_{CANH}=V_{CANL}=5V	-5	0	5	μA
SPLIT Pin Leakage Current	$\lvert I_L \rvert$	Standby mode -22V<V_{SPLIT}<35V	—	0	5	μA
Input Threshold Voltage						
High-level input voltage for the standby pin	$V_{STB(H)}$		2	—	Vcc+0.3	V
Standby pin low-level input voltage	$V_{STB(L)}$		-0.3	—	0.8	V
Pin TXD high-level input voltage	$V_{TXD(H)}$		2	—	Vcc+0.3	V
Pin TXD low-level input voltage	$V_{TXD(L)}$		-0.3	—	0.8	V
Differential receiver threshold voltage	$V_{dif(th)}$	Normal mode -12V<VCAN<12V	0.5	0.7	0.9	V
Differential receiver threshold hysteresis	$V_{ifhys)}$		50	70	100	mV
Standby mode differential receiver threshold voltage	$V_{dif(th)(stb)}$	Standby mode-12V<VCAN<12V	0.4	0.7	1.15	V
Output voltage						
Pin CANH dominant output voltage	$V_{O(CANH)(dom)}$	V_{TXD}=0V 45Ω<R_L<65Ω	3	3.6	4.25	V
Pin CANL output voltage (dominant)	$V_{O(CANL)(dom)}$		0.5	1.4	1.75	V
Differential bus explicit output voltage	$V_{O(dif)(dom)}$		1.5	—	3	V
Dominant output voltage matching	$V_{O(dom)(m)}$	Vcc-Vo(CANH))(dom) -Vo(CANL)(dom)	-100	0	150	mV
Implicit bus output voltage	$V_{O(reces)}$	Normal mode V_{TXD}=Vcc,no load	2	0.5Vcc	3	V
Differential bus implicit output voltage	$V_{O(dif)(reces)}$		-50	—	50	mV
Standby Mode Bus Output Voltage	$V_{O(stb)}$	Standby mode,no load	-0.1	0	0.1	V
Pin RXD high-level output voltage	$V_{RXD(H)}$	Standby mode I_{rxD}=-100μA	Vcc-1.1	Vcc-0.7	Vcc-0.4	V
Pin SPLIT Output Voltage	V_{SPLIT}	Normal mode -500μA<ISPLIT<500μA	0.3Vcc	0.5Vcc	0.7Vcc	V

Electrical characteristics （Continue）

Unless otherwise specified, all typical values are measured under the conditions of T_A=25°C, V_{CC}=5V, T_{VJ}= -40~50°C, and R_L=60Ω. All voltages are referenced to ground, and the positive current direction is flowing into the IC.

Parameter declaration	Symbol	Test condition	Least value	Representative value	Crest value	Unit
Transfer characteristic						
TXD-induced explicit delay in the bus communication	$t_{a(TXD-BUSon)}$	Normal mode	25	70	110	ns
Bus visibility to RXD latency	$t_{a(BUSon-RXD)}$		15	65	115	ns
TXD to bus implicit latency	$t_{a(TXD-BUSoff)}$		10	50	95	ns
Bus latency to RXD delay	$t_{d(BUSoff-RXD)}$		35	100	160	ns
Transmission delay from TXD to RXD	$t_{PD(TXD-RXD)}$	V_{STB}=0V	40	—	255	ns
Bus Wake Time	t_{BUS}	Standby mode	0.75	1.75	5	μs
Defencive function						
Enabling time from standby mode to normal mode	$t_{a(stb-norm)}$		5	7.5	10	μs
TXD Dominant Timeout	$t_{dom(TXD)}$	V_{TXD}=0V	300	600	1000	μs
Turn-off junction temperature	$T_{j(sd)}$		155	165	180	℃
Input resistance						
Common-mode input impedance	$R_{icm)}$	Normal/Standby Mode	15	25	35	kΩ
Common-mode input impedance matching	$R_{icm)(m)}$	V_{CANH}=V_{CANL}	-3	0	3	%
Differential input impedance	$R_{i(dif)}$	Normal/Standby Mode	25	50	75	kΩ
Input capacitance						
TXD Pin Input Capacitor	$C_{i(TXD)}$		—	5	10	pF
Common-mode input capacitance	$C_{i(cm)}$	V_{TXD}=Vcc	—	—	20	pF
Differential input capacitor	$C_{i(dif)}$		—	—	10	pF

Functional Description

Work Pattern

The TJA1050 has two operating modes, which can be selected via the STB pin. Table 1 provides detailed descriptions of these operating modes.

Pattern	Pin STB	Pin RXD	
		Low	Gao
Normal mode	Low	Bus Visibility	Bus Implicitity
Standby mode	Gao	Wake request detected	No wake-up request detected

The STB control pin allows selection of two operating modes: normal mode and standby mode. Normal mode is selected by connecting pin STB to ground. Both the CAN driver and receiver operate fully normally, and CAN communication proceeds bidirectionally. t_{BUS} Standby mode can be selected by setting the STB to a high level. Both the CAN driver and receiver are turned off to reduce system power consumption. The high level on pin STB activates the low-power receiver and wake-up filter; when the low-power differential comparator detects an explicit bus level exceeding , pin RXD transitions to a low level.

Common-Mode Voltage Regulation Function

The SPLIT pin provides a 0.5VCC DC voltage regulator. It is only connected in normal mode. In standby mode, the SPL pin is floating. By connecting the SPLIT pin to the midpoint of the terminal load, the recessive common-mode voltage is stabilized. Due to the presence of unpowered transce on the bus, they have significant leakage current between the bus and ground, making the recessive bus voltage < $0.5V_{CC}$. The common-mode voltage regulation function will this recessive voltage to $0.5V_{CC}$. Therefore, no step will be generated on the common-mode signal when starting transmission, thereby ensuring the electromagnetic emission (EME).

Wake Up Function

In standby mode, the bus is monitored by a low-power differential comparator. Once the low-power differential comparator detects a persistent bus voltage level lasting longer than t_{BUS} , pin RXD becomes low (low-level).

Overheating Detection

The output driver is protected against overheating. If the temperature exceeds 165°C, the output driver will be disabled until the temperature drops below the typical threshold of 165°C and TXD becomes inactive, at which point it resumes operation. Thus, the output driver does not oscillate due to temperature fluctuations.

TXD Explicit Timeout Function

When the TXD pin is continuously held low (level) due to a hardware or software error, the " TXD dominant timeout" timer circuit prevents bus from entering a continuous dominant state (blocking all network communication). This timer is triggered by the falling edge of the TXD pin. If the low level of the TXD lasts longer than the internal timer value (tdom), the transceiver will be disabled, forcing the bus into a recessive state. The timer is reset by the rising edge of the TX pin. The TXD dominant timeout time (tdom) defines the minimum allowed bit rate as 40kBaud.

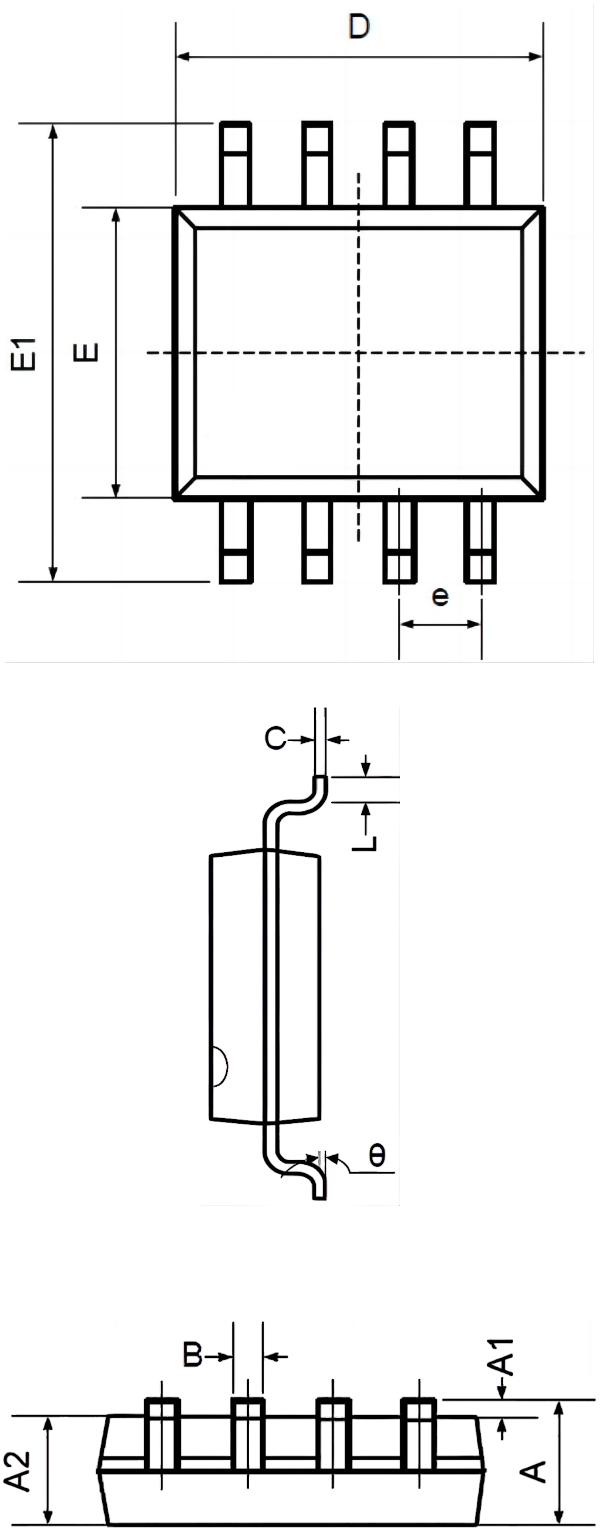
Failure Protection Function

Pin TXD provides a pull-up to Vcc, keeping it at a low level when not in use. Pin STB provides a pull-up to Vcc; when not used, it puts the transceiver into standby mode. If Vcc is powered down , pins TXD, STB, and RXD remain floating to prevent reverse current flow through them.

Order information

Order Number	Package	Package Quantity	Marking On The park	Temperature
TJA1050T/CM-TUDI	SOP8	Tape,Reel,2500	A1050/C	-40℃ to 150℃

Package SOP8



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
B	0.330	0.510	0.013	0.020
C	0.190	0.250	0.007	0.010
D	4.780	5.000	0.188	0.197
E	3.800	4.000	0.150	0.157
E1	5.800	6.300	0.228	0.248
e	1.270TYP		0.050TYP	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

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