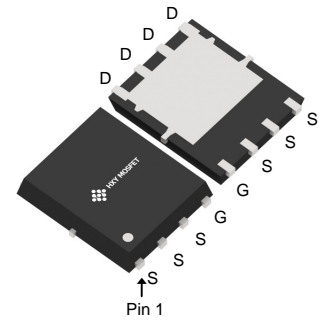




General Description

The DMTH6005LPS-13 use advanced SGT MOSFET technology to provide low RDS(ON), low gate charge, fast switching and excellent avalanche characteristics.

This device is specially designed to get better ruggedness and suitable.



DFN5X6-8L

General Features

$V_{DS} = 60V$ $I_D = 100A$

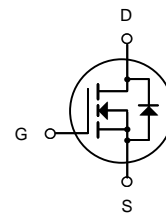
$R_{DS(ON)} < 5m\Omega$ @ $V_{GS}=10V$

Applications

Consumer electronic power supply Motor control

Synchronous-rectification Isolated DC

Synchronous-rectification applications



N-Channel MOSFET

Ordering Information

Product ID	Pack	Brand	Qty(PCS)
DMTH6005LPS-13	DFN5X6-8L	HXY MOSFET	5000

Absolute Maximum Ratings ($T_c = 25^\circ C$ unless otherwise noted)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	60	V
V_{GS}	Gate-Source Voltage	± 20	V
$I_D @ T_c = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	100	A
$I_D @ T_c = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	64	A
I_{DM}	Pulsed Drain Current ²	385	A
EAS	Single Pulse Avalanche Energy ³	80	mJ
$P_D @ T_c = 25^\circ C$	Total Power Dissipation ⁴	73.5	W
T_{STG}	Storage Temperature Range	-55 to 150	$^\circ C$
T_J	Operating Junction Temperature Range	-55 to 150	$^\circ C$
$R_{\theta JC}$	Thermal Resistance from Junction-to-Ambient ³	1.7	$^\circ C/W$
$R_{\theta JA}$	Thermal Resistance Junction-Ambient ¹	51	$^\circ C/W$



Electrical Characteristics ($T_J = 25^\circ\text{C}$, unless otherwise noted)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit	
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	60	-	-	V	
Gate-body Leakage Current	I_{GSS}	$V_{DS} = 0V, V_{GS} = \pm 20V$	-	-	± 100	nA	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 60V, V_{GS} = 0V$	$T_J = 25^\circ\text{C}$	-	-	1	μA
			$T_J = 100^\circ\text{C}$	-	-	100	
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	2	2.9	4	V	
Drain-Source On-Resistance ⁴	$R_{DS(on)}$	$V_{GS} = 10V, I_D = 21A$	-	3.7	5	m Ω	
Forward Transconductance ⁴	g_{fs}	$V_{DS} = 10V, I_D = 21A$	-	89	-	S	
Input Capacitance	C_{iss}	$V_{DS} = 30V, V_{GS} = 0V, f = 1\text{MHz}$	-	1673	-	pF	
Output Capacitance	C_{oss}		-	773	-		
Reverse Transfer Capacitance	C_{rss}		-	46.8	-		
Gate Resistance	R_g	$f = 1\text{MHz}$	-	1.8	-	Ω	
Total Gate Charge	Q_g	$V_{GS} = 10V, V_{DS} = 30V, I_D = 21A$	-	28.5	-	nC	
Gate-Source Charge	Q_{gs}		-	7.8	-		
Gate-Drain Charge	Q_{gd}		-	8.4	-		
Turn-On Delay Time	$t_{d(on)}$	$V_{GS} = 10V, V_{DD} = 30V, R_G = 3\Omega, I_D = 21A$	-	11.2	-	ns	
Rise Time	t_r		-	8.2	-		
Turn-Off Delay Time	$t_{d(off)}$		-	19.6	-		
Fall Time	t_f		-	6.2	-		
Body Diode Reverse Recovery Time	t_{rr}	$I_F = 21A, dI/dt = 100A/\mu s$	-	50	-	ns	
Body Diode Reverse Recovery Charge	Q_{rr}		-	20	-	nC	
Diode Forward Voltage ⁴	V_{SD}	$I_S = 21A, V_{GS} = 0V$	-	-	1.2	V	
Continuous Source Current	I_S	$T_C = 25^\circ\text{C}$	-	-	100	A	

Notes:

1. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)} = 150^\circ\text{C}$
2. The EAS data shows Max. rating . The test condition is $V_{DD} = 25V, V_{GS} = 10V, L = 0.1\text{mH}, I_{AS} = 40A$.
3. The data tested by surface mounted on a 1 inch2 FR-4 board with 2OZ copper, The value in any given application depends on the user's specific board design.
4. The data tested by pulsed , pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$.
5. This value is guaranteed by design hence it is not included in the production test.



Typical Characteristics

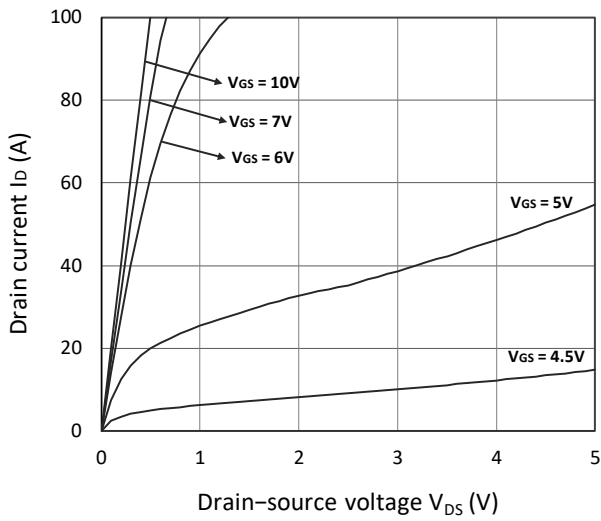


Figure 1. Output Characteristics

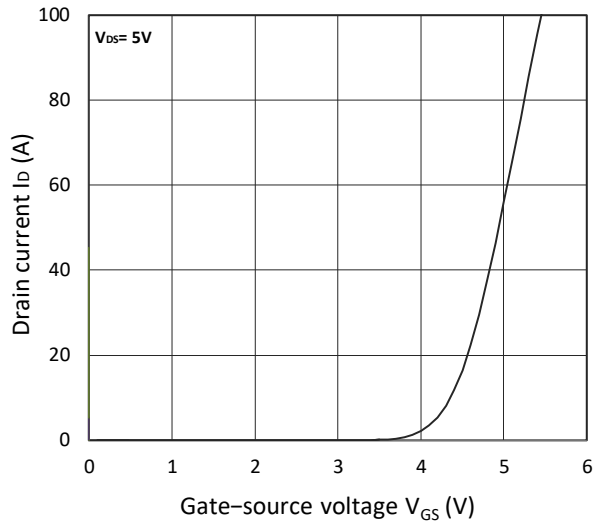


Figure 2. Transfer Characteristics

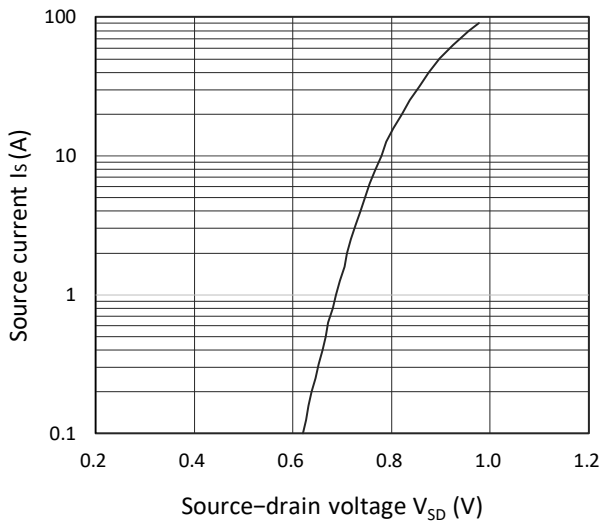


Figure 3. Forward Characteristics of Reverse

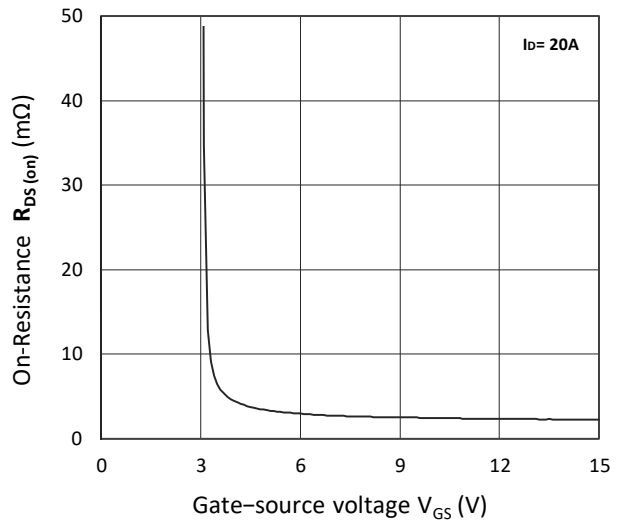


Figure 4. $R_{DS(ON)}$ vs. V_{GS}

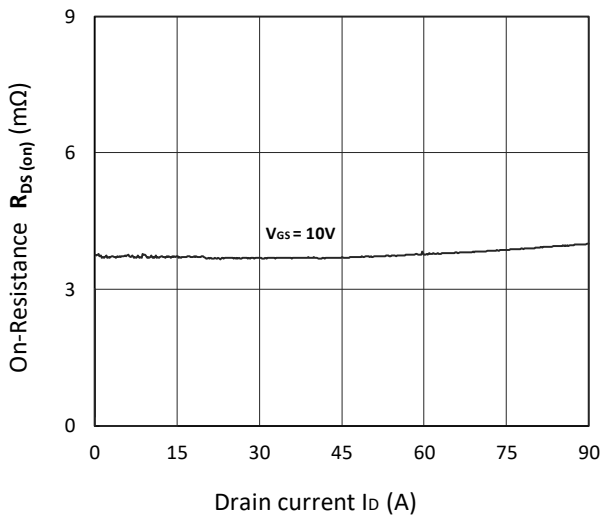


Figure 5. $R_{DS(ON)}$ vs. I_D

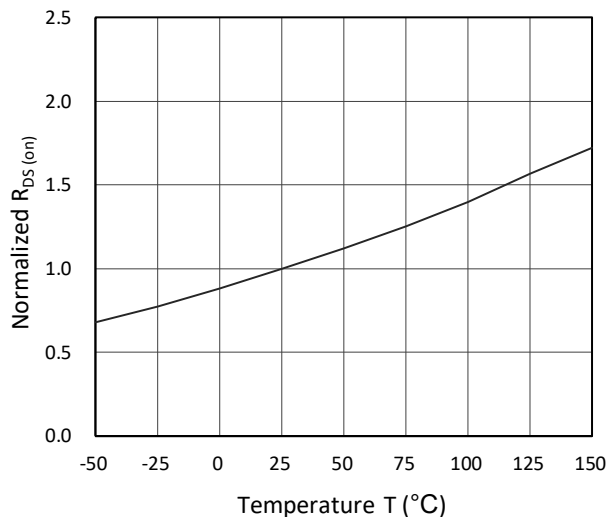


Figure 6. Normalized $R_{DS(ON)}$ vs. Temperature

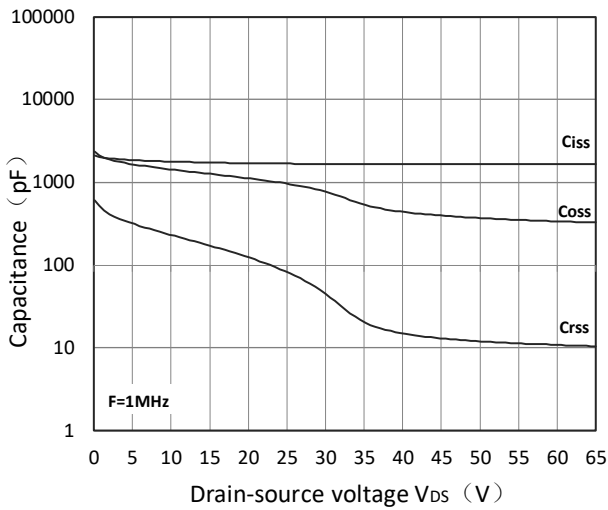


Figure 7. Capacitance Characteristics

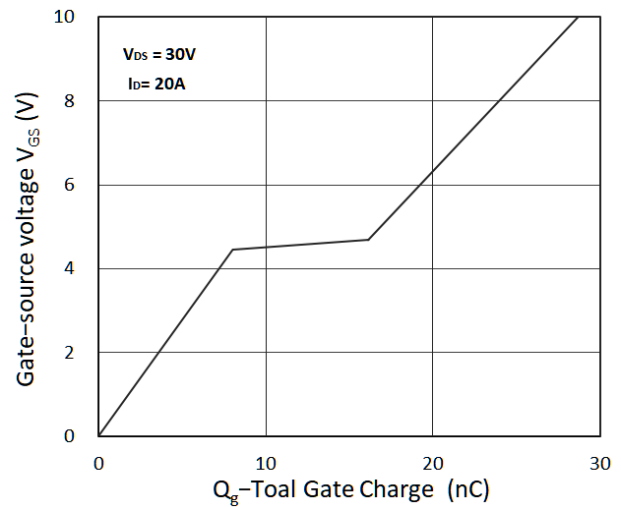


Figure 8. Gate Charge Characteristics

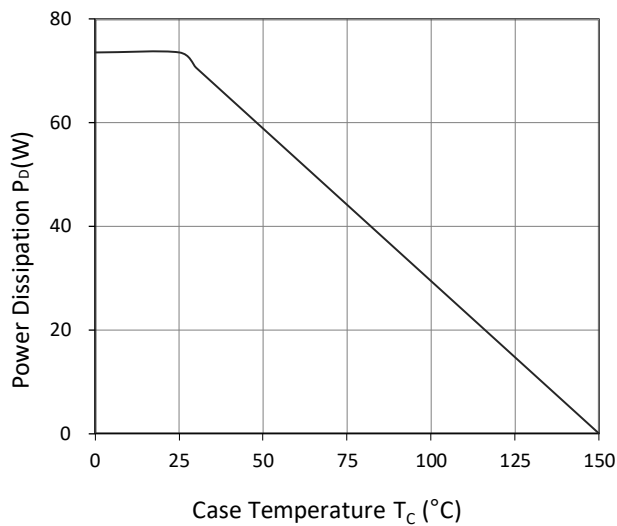


Figure 9. Power Dissipation

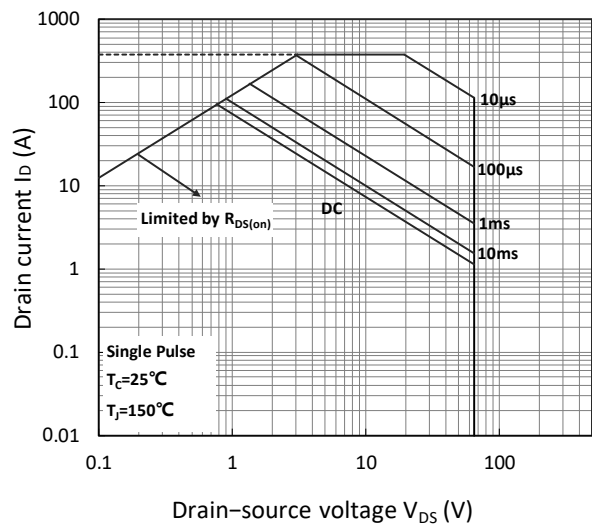


Figure 10. Safe Operating Area

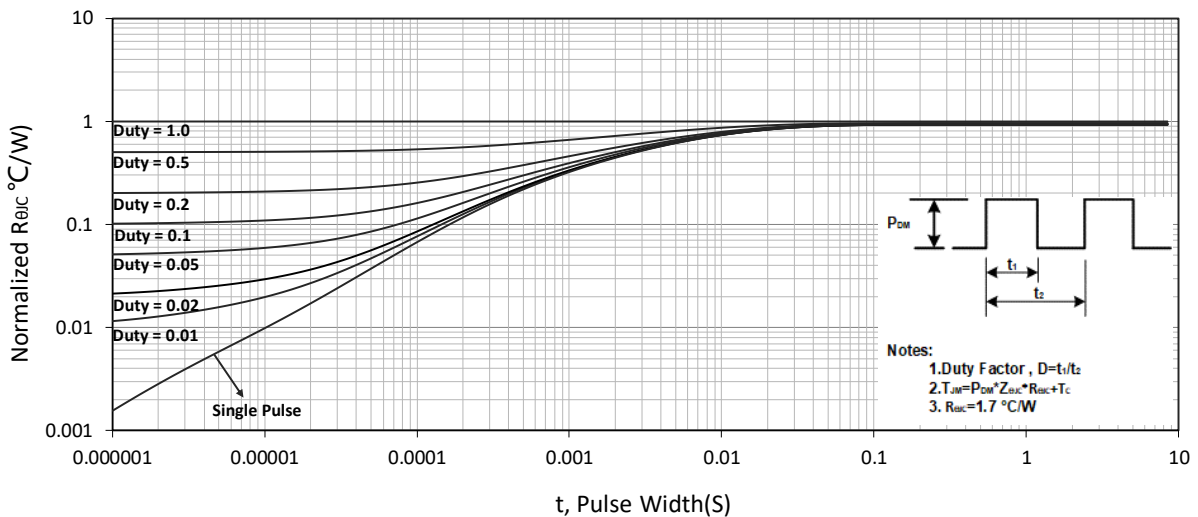


Figure 11. Normalized Maximum Transient Thermal Impedance



Test Circuit

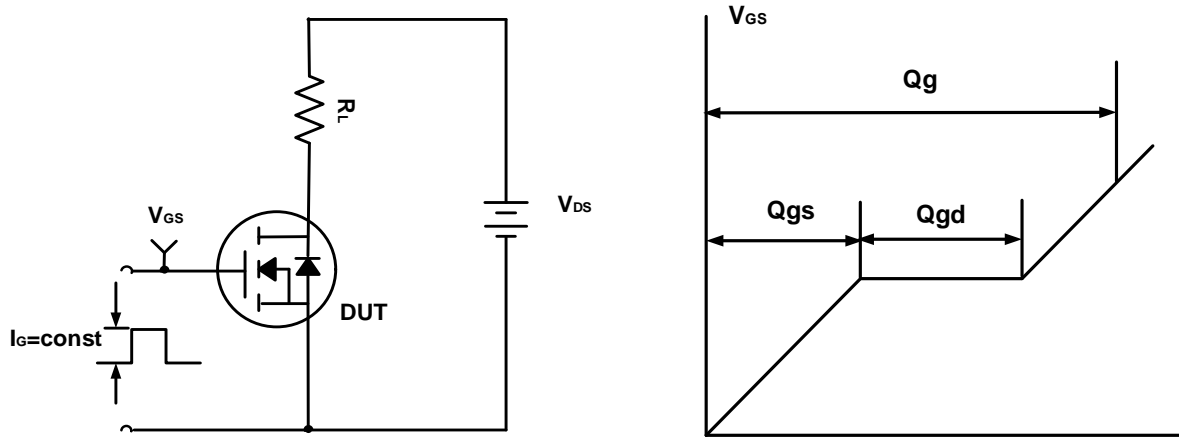


Figure A. Gate Charge Test Circuit & Waveforms

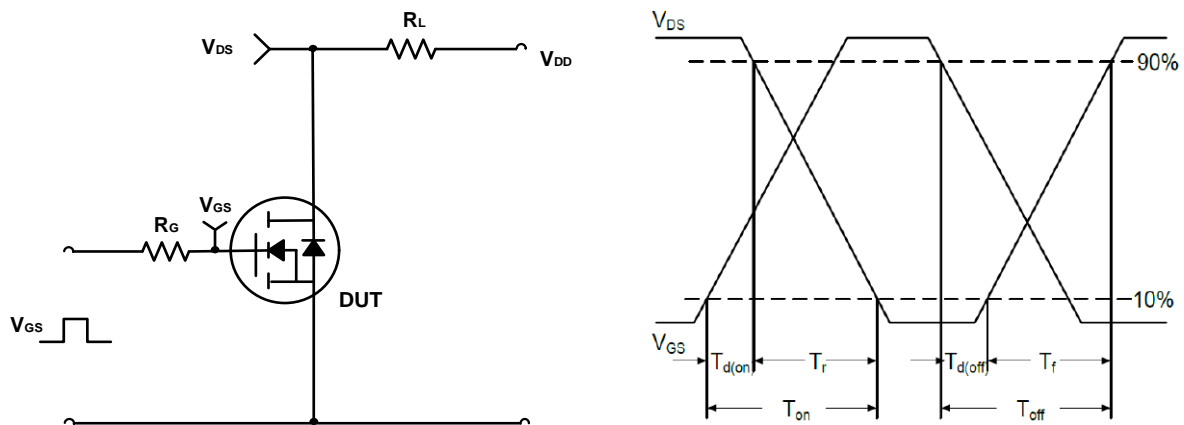


Figure B. Switching Test Circuit & Waveforms

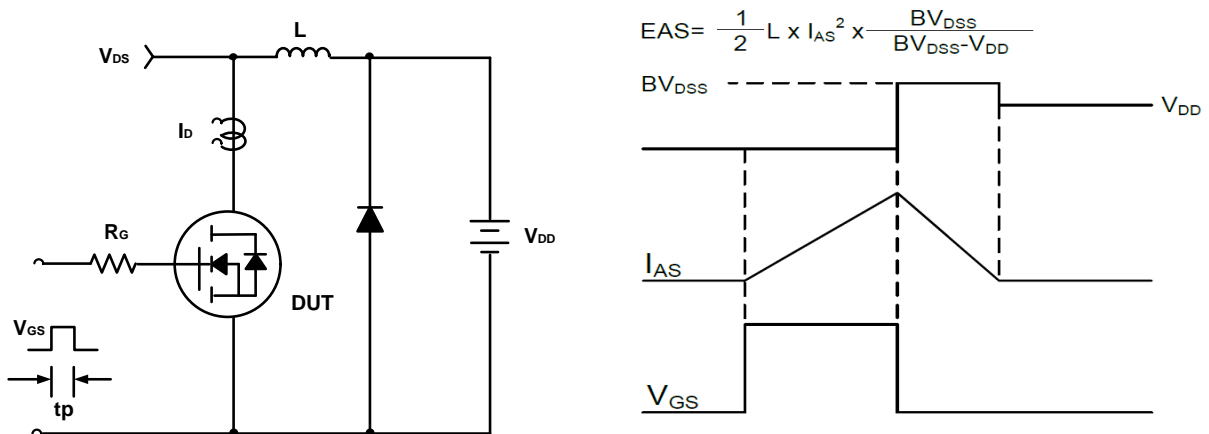
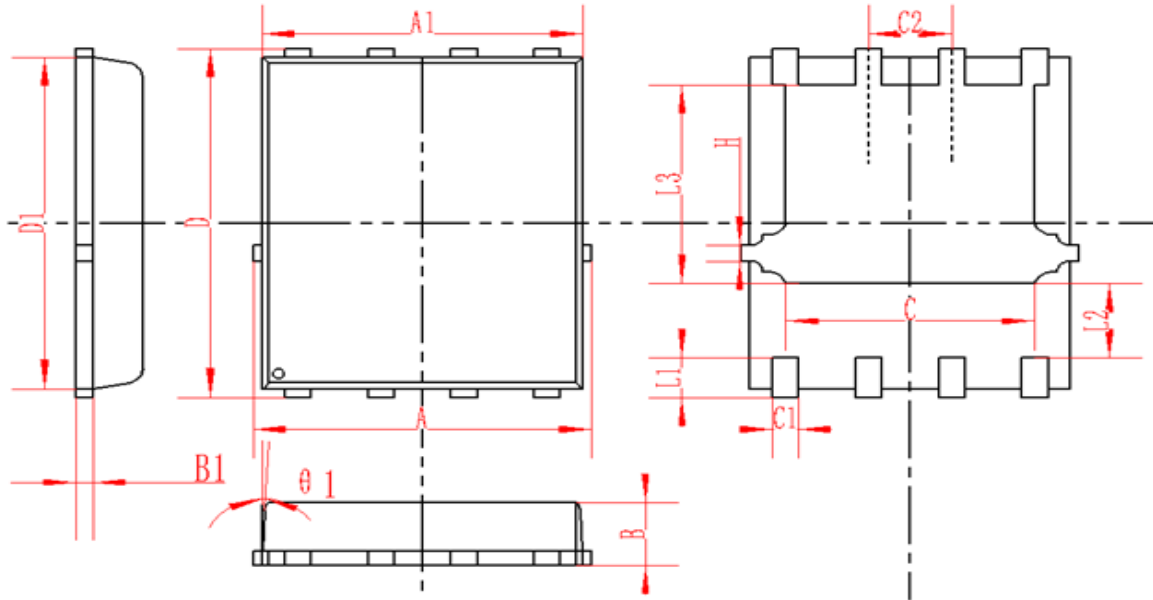


Figure C. Unclamped Inductive Switching Circuit & Waveforms



DFN5X6-8L Package Information



SYMBOL	MM			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	4.95	5	5.05	0.195	0.197	0.199
A1	4.82	4.9	4.98	0.190	0.193	0.196
D	5.98	6	6.02	0.235	0.236	0.237
D1	5.67	5.75	5.83	0.223	0.226	0.230
B	0.9	0.95	1	0.035	0.037	0.039
B1	0.254REF			0.010REF		
C	3.95	4	4.05	0.156	0.157	0.159
C1	0.35	0.4	0.45	0.014	0.016	0.018
C2	1.27TYP			0.5TYP		
$\theta 1$	8°	10°	12°	8°	10°	12°
L1	0.63	0.64	0.65	0.025	0.025	0.026
L2	1.2	1.3	1.4	0.047	0.051	0.055
L3	3.415	3.42	3.425	0.134	0.135	0.135
H	0.24	0.25	0.26	0.009	0.010	0.010



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