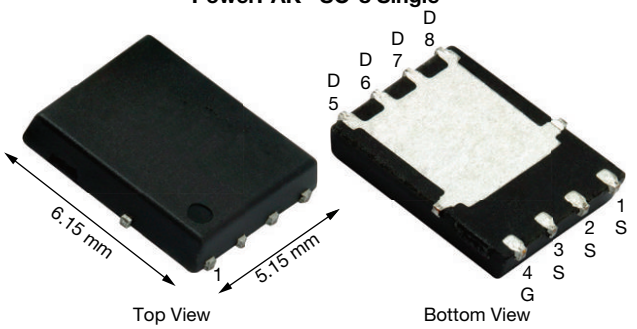
# N-Channel 40 V (D-S) MOSFET

| PRODUCT SUMMARY | | | |
|---|---|---|---|
| $V_{DS}$ (V) | $R_{DS(on)}$ (Ω) (MAX.) | $I_D$ (A) [a, g] | $Q_g$ (TYP.) |
| 40 | 0.00088 at $V_{GS}$ = 10 V | 100 | 63 nC |
| | 0.00116 at $V_{GS}$ = 4.5 V | 100 | |

**PowerPAK® SO-8 Single**




Top View Bottom View

**Ordering Information**:
SiR638DP-T1-GE3 (lead (Pb)-free and halogen-free)

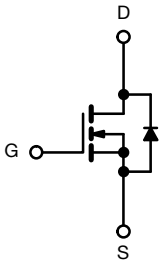
## FEATURES

- TrenchFET® Gen IV power MOSFET
- 100 % $R_g$ and UIS tested
- $Q_{gd}$ / $Q_{gs}$ ratio < 1 optimizes switching characteristics
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

RoHS COMPLIANT
HALOGEN FREE

## APPLICATIONS

- Synchronous rectification
- ORing
- High power density DC/DC
- VRMs and embedded DC/DC
- DC/AC inverters
- Load switch




N-Channel MOSFET

| ABSOLUTE MAXIMUM RATINGS ($T_A$ = 25 °C, unless otherwise noted) | | | | |
|---|---|---|---|---|
| PARAMETER | | SYMBOL | LIMIT | UNIT |
| Drain-Source Voltage | | $V_{DS}$ | 40 | V |
| Gate-Source Voltage | | $V_{GS}$ | +20, -16 | |
| Continuous Drain Current ($T_J$ = 150 °C) | $T_C$ = 25 °C | $I_D$ | 100 [g] | A |
| | $T_C$ = 70 °C | | 100 [g] | |
| | $T_A$ = 25 °C | | 62.8 [b, c] | |
| | $T_A$ = 70 °C | | 50.2 [b, c] | |
| Pulsed Drain Current (t = 100 µs) | | $I_{DM}$ | 400 | |
| Continuous Source-Drain Diode Current | $T_C$ = 25 °C | $I_S$ | 94.5 | |
| | $T_A$ = 25 °C | | 5.6 [b, c] | |
| Single Pulse Avalanche Current | L = 0.1 mH | $I_{AS}$ | 50 | |
| Single Pulse Avalanche Energy | | $E_{AS}$ | 125 | mJ |
| Maximum Power Dissipation | $T_C$ = 25 °C | $P_D$ | 104 | W |
| | $T_C$ = 70 °C | | 66.6 | |
| | $T_A$ = 25 °C | | 6.25 [b, c] | |
| | $T_A$ = 70 °C | | 4 [b, c] | |
| Operating Junction and Storage Temperature Range | | $T_J$, $T_{stg}$ | -55 to +150 | °C |
| Soldering Recommendations (Peak Temperature) [d, e] | | | 260 | |

| THERMAL RESISTANCE RATINGS | | | | | |
|---|---|---|---|---|---|
| PARAMETER | | SYMBOL | TYPICAL | MAXIMUM | UNIT |
| Maximum Junction-to-Ambient [b, f] | t ≤ 10 s | $R_{thJA}$ | 15 | 20 | °C/W |
| Maximum Junction-to-Case (Drain) | Steady State | $R_{thJC}$ | 0.9 | 1.2 | |

**Notes**

a. Based on $T_C$ = 25 °C.
b. Surface mounted on 1" x 1" FR4 board.
c. t = 10 s.
d. See solder profile (www.vishay.com/doc?73257). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.
f. Maximum under steady state conditions is 54 °C/W.
g. Package limited.



For technical questions, contact: pmostechsupport@vishay.com

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| **SPECIFICATIONS** ($T_J$ = 25 °C, unless otherwise noted) | | | | | | |
|---|---|---|---|---|---|---|
| **PARAMETER** | **SYMBOL** | **TEST CONDITIONS** | **MIN.** | **TYP.** | **MAX.** | **UNIT** |
| **Static** | | | | | | |
| Drain-Source Breakdown Voltage | $V_{DS}$ | $V_{GS}$ = 0 V, $I_D$ = 250 µA | 40 | - | - | V |
| $V_{DS}$ Temperature Coefficient | $\Delta V_{DS}/T_J$ | $I_D$ = 250 µA | - | 24 | - | mV/°C |
| $V_{GS(th)}$ Temperature Coefficient | $\Delta V_{GS(th)}/T_J$ | | - | -5.4 | - | |
| Gate-Source Threshold Voltage | $V_{GS(th)}$ | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 µA | 1.1 | - | 2.3 | V |
| Gate-Source Leakage | $I_{GSS}$ | $V_{DS}$ = 0 V, $V_{GS}$ = +20, -16 V | - | - | ± 100 | nA |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS}$ = 40 V, $V_{GS}$ = 0 V | - | - | 1 | µA |
| | | $V_{DS}$ = 40 V, $V_{GS}$ = 0 V, $T_J$ = 55 °C | - | - | 10 | |
| On-State Drain Current [a] | $I_{D(on)}$ | $V_{DS} \geq$ 5 V, $V_{GS}$ = 10 V | 50 | - | - | A |
| Drain-Source On-State Resistance [a] | $R_{DS(on)}$ | $V_{GS}$ = 10 V, $I_D$ = 20 A | - | 0.00073 | 0.00088 | Ω |
| | | $V_{GS}$ = 4.5 V, $I_D$ = 15 A | - | 0.00096 | 0.00116 | |
| Forward Transconductance [a] | $g_{fs}$ | $V_{DS}$ = 10 V, $I_D$ = 20 A | - | 147 | - | S |
| **Dynamic [b]** | | | | | | |
| Input Capacitance | $C_{iss}$ | $V_{DS}$ = 20 V, $V_{GS}$ = 0 V, f = 1 MHz | - | 10 500 | - | pF |
| Output Capacitance | $C_{oss}$ | | - | 1530 | - | |
| Reverse Transfer Capacitance | $C_{rss}$ | | - | 250 | - | |
| $C_{rss}/C_{iss}$ Ratio | | | - | 0.024 | 0.048 | |
| Total Gate Charge | $Q_g$ | $V_{DS}$ = 20 V, $V_{GS}$ = 10 V, $I_D$ = 20 A | - | 136 | 204 | nC |
| | | $V_{DS}$ = 20 V, $V_{GS}$ = 4.5 V, $I_D$ = 20 A | - | 63 | 95 | |
| Gate-Source Charge | $Q_{gs}$ | | - | 30.5 | - | |
| Gate-Drain Charge | $Q_{gd}$ | | - | 10.6 | - | |
| Output Charge | $Q_{oss}$ | $V_{DS}$ = 20 V, $V_{GS}$ = 0 V | - | 75 | - | |
| Gate Resistance | $R_g$ | f = 1 MHz | 0.3 | 0.88 | 1.5 | Ω |
| Turn-On Delay Time | $t_{d(on)}$ | $V_{DD}$ = 20 V, $R_L$ = 1 Ω<br>$I_D \cong$ 20 A, $V_{GEN}$ = 10 V, $R_g$ = 1 Ω | - | 20 | 40 | ns |
| Rise Time | $t_r$ | | - | 21 | 42 | |
| Turn-Off Delay Time | $t_{d(off)}$ | | - | 52 | 100 | |
| Fall Time | $t_f$ | | - | 10 | 20 | |
| Turn-On Delay Time | $t_{d(on)}$ | $V_{DD}$ = 20 V, $R_L$ = 1 Ω<br>$I_D \cong$ 20 A, $V_{GEN}$ = 4.5 V, $R_g$ = 1 Ω | - | 70 | 140 | |
| Rise Time | $t_r$ | | - | 16 | 32 | |
| Turn-Off Delay Time | $t_{d(off)}$ | | - | 43 | 86 | |
| Fall Time | $t_f$ | | - | 19 | 38 | |
| **Drain-Source Body Diode Characteristics** | | | | | | |
| Continuous Source-Drain Diode Current | $I_S$ | $T_C$ = 25 °C | - | - | 100 | A |
| Pulse Diode Forward Current ($t_p$ = 100 µs) | $I_{SM}$ | | - | - | 400 | |
| Body Diode Voltage | $V_{SD}$ | $I_S$ = 10 A | - | 0.73 | 1.1 | V |
| Body Diode Reverse Recovery Time | $t_{rr}$ | $I_F$ = 20 A, dI/dt = 100 A/µs,<br>$T_J$ = 25 °C | - | 59 | 118 | ns |
| Body Diode Reverse Recovery Charge | $Q_{rr}$ | | - | 85 | 170 | nC |
| Reverse Recovery Fall Time | $t_a$ | | - | 34 | - | ns |
| Reverse Recovery Rise Time | $t_b$ | | - | 25 | - | |

**Notes**

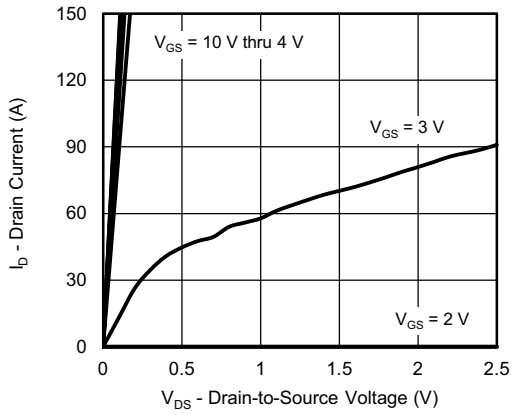
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.

b. Guaranteed by design, not subject to production testing.

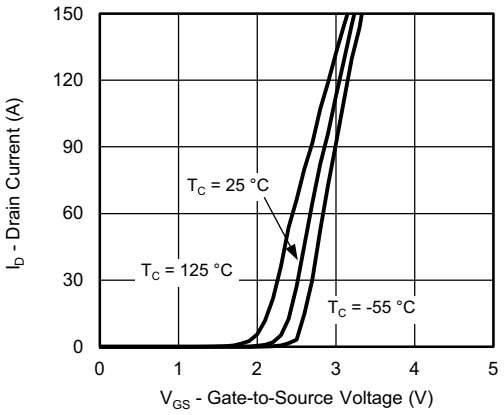
*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*


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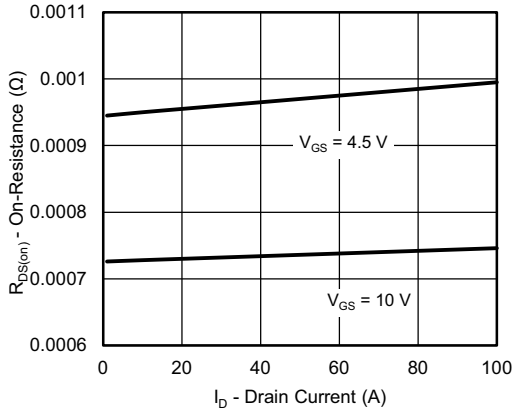
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



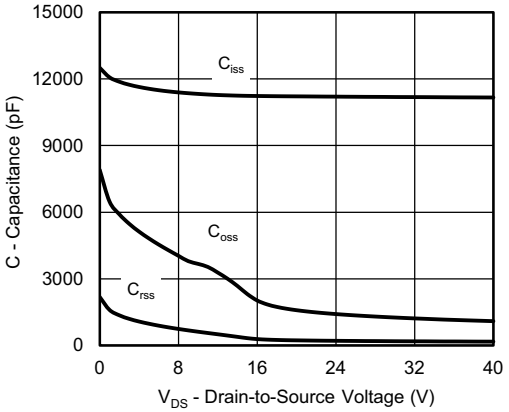

**Output Characteristics**



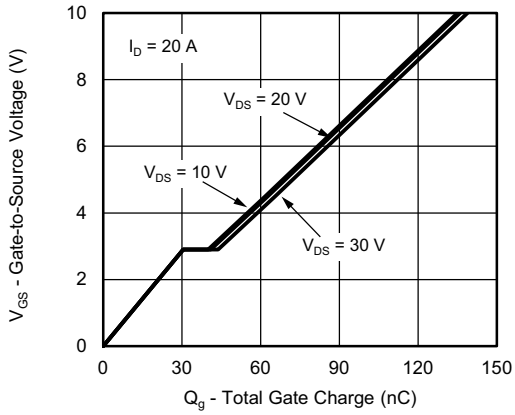

**Transfer Characteristics**



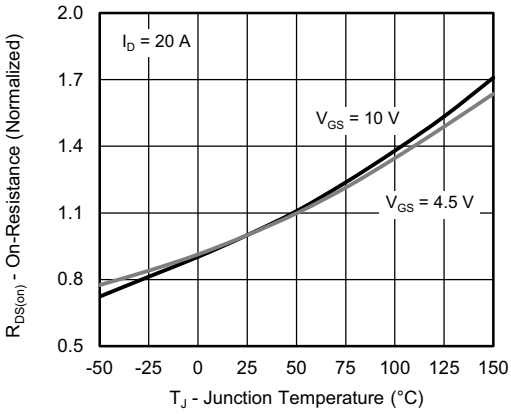

**On-Resistance vs. Drain Current**




**Capacitance**



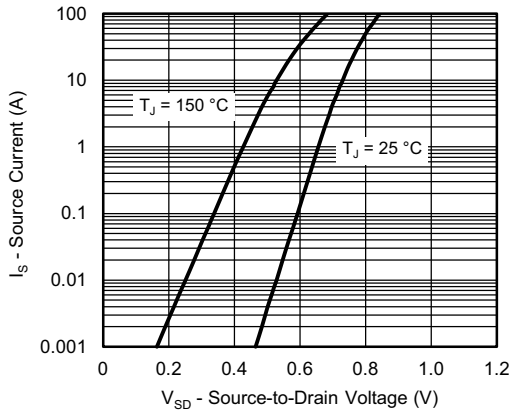

**Gate Charge**



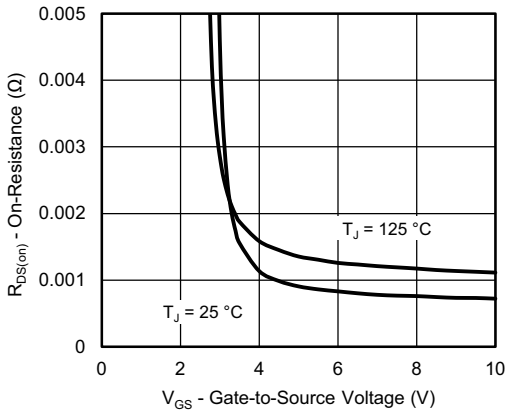

**On-Resistance vs. Junction Temperature**


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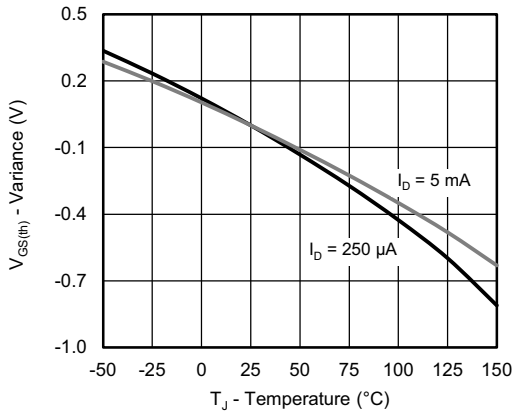
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



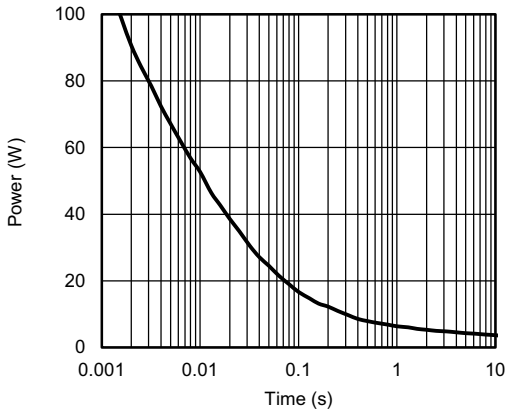

**Source-Drain Diode Forward Voltage**



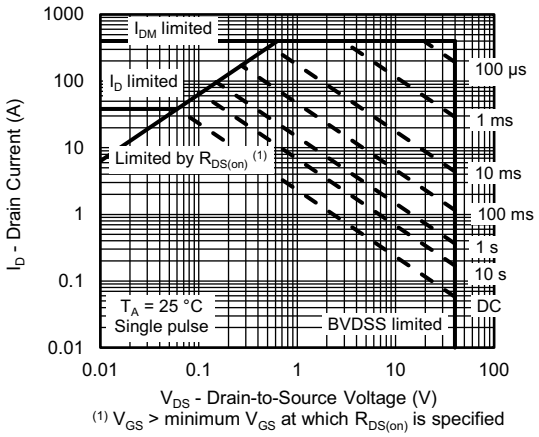

**On-Resistance vs. Gate-to-Source Voltage**




**Threshold Voltage**



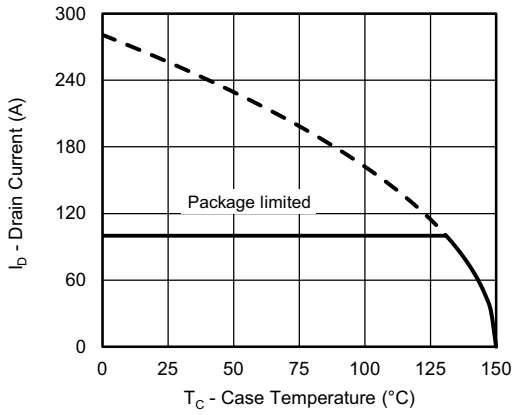

**Single Pulse Power, Junction-to-Ambient**



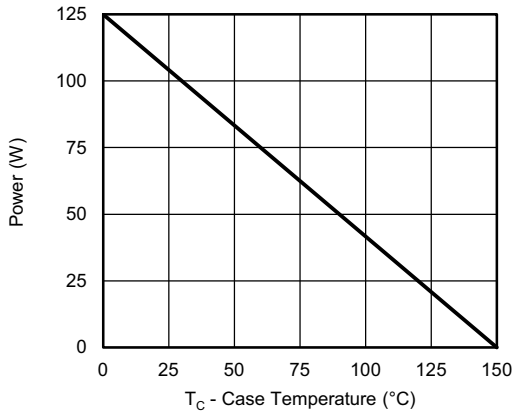

**Safe Operating Area**


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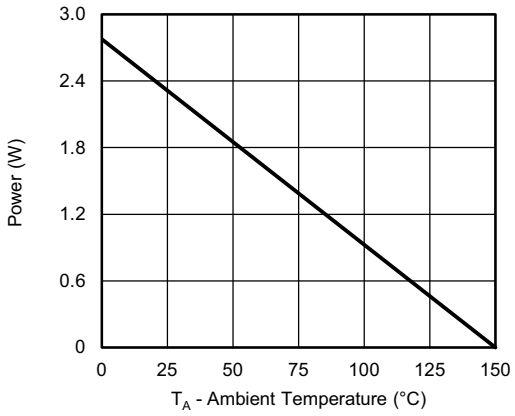
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)




**Current Derating** [a]




**Power, Junction-to-Case**



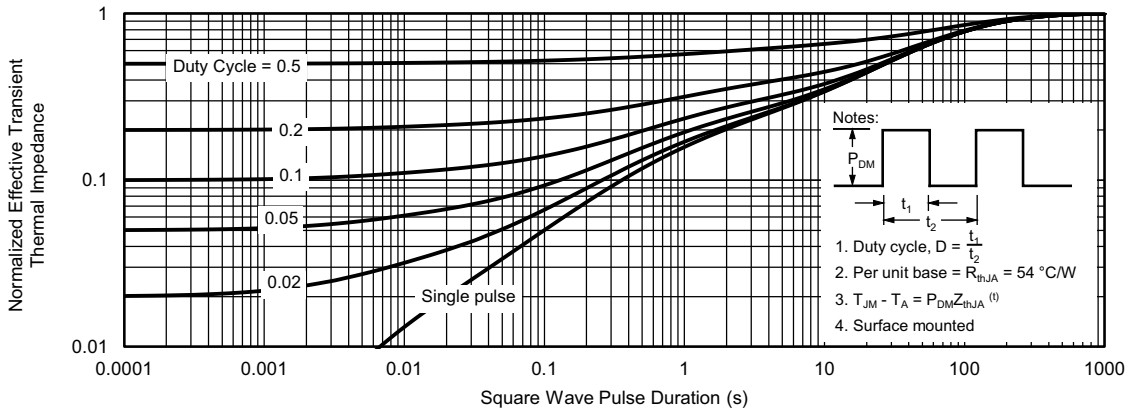

**Power, Junction-to-Ambient**

**Note**

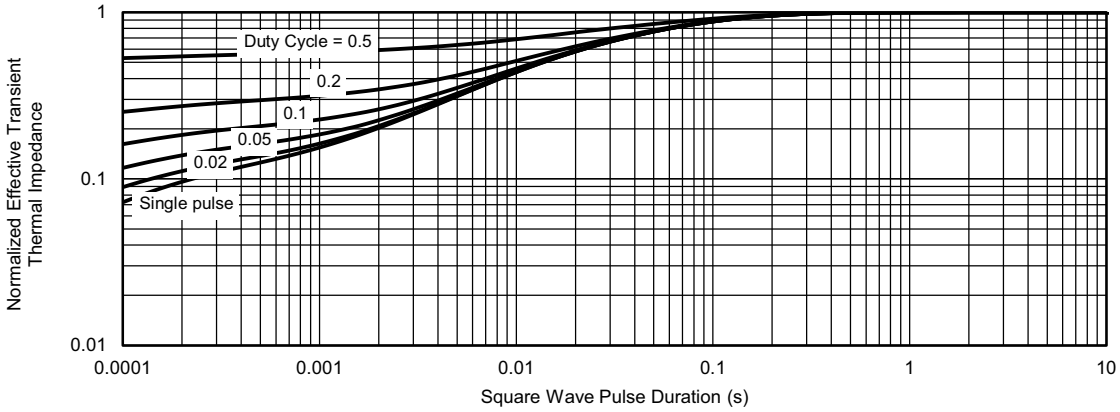
a. The power dissipation $P_D$ is based on $T_J$ (max.) = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.


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**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)




**Normalized Thermal Transient Impedance, Junction-to-Ambient**

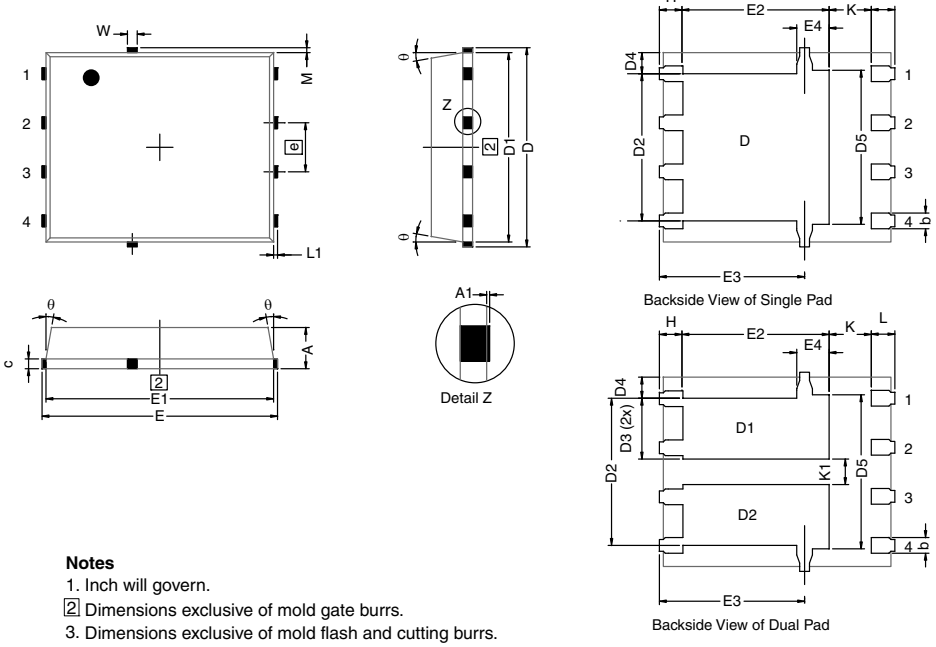



**Normalized Thermal Transient Impedance, Junction-to-Case**

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# PowerPAK® SO-8, (Single/Dual)




**Notes**

1. Inch will govern.
2. Dimensions exclusive of mold gate burrs.
3. Dimensions exclusive of mold flash and cutting burrs.

| DIM. | MILLIMETERS | | | INCHES | | |
|---|---|---|---|---|---|---|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | 0.97 | 1.04 | 1.12 | 0.038 | 0.041 | 0.044 |
| A1 | | - | 0.05 | 0 | - | 0.002 |
| b | 0.33 | 0.41 | 0.51 | 0.013 | 0.016 | 0.020 |
| c | 0.23 | 0.28 | 0.33 | 0.009 | 0.011 | 0.013 |
| D | 5.05 | 5.15 | 5.26 | 0.199 | 0.203 | 0.207 |
| D1 | 4.80 | 4.90 | 5.00 | 0.189 | 0.193 | 0.197 |
| D2 | 3.56 | 3.76 | 3.91 | 0.140 | 0.148 | 0.154 |
| D3 | 1.32 | 1.50 | 1.68 | 0.052 | 0.059 | 0.066 |
| D4 | 0.57 typ. | | | 0.0225 typ. | | |
| D5 | 3.98 typ. | | | 0.157 typ. | | |
| E | 6.05 | 6.15 | 6.25 | 0.238 | 0.242 | 0.246 |
| E1 | 5.79 | 5.89 | 5.99 | 0.228 | 0.232 | 0.236 |
| E2 | 3.48 | 3.66 | 3.84 | 0.137 | 0.144 | 0.151 |
| E3 | 3.68 | 3.78 | 3.91 | 0.145 | 0.149 | 0.154 |
| E4 | 0.75 typ. | | | 0.030 typ. | | |
| e | 1.27 BSC | | | 0.050 BSC | | |
| K | 1.27 typ. | | | 0.050 typ. | | |
| K1 | 0.56 | - | - | 0.022 | - | - |
| H | 0.51 | 0.61 | 0.71 | 0.020 | 0.024 | 0.028 |
| L | 0.51 | 0.61 | 0.71 | 0.020 | 0.024 | 0.028 |
| L1 | 0.06 | 0.13 | 0.20 | 0.002 | 0.005 | 0.008 |
| θ | 0° | - | 12° | 0° | - | 12° |
| W | 0.15 | 0.25 | 0.36 | 0.006 | 0.010 | 0.014 |
| M | 0.125 typ. | | | 0.005 typ. | | |
| ECN: S17-0173-Rev. L, 13-Feb-17<br>DWG: 5881 | | | | | | |



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# PowerPAK® SO-8 Mounting and Thermal Considerations

**by Wharton McDaniel**

MOSFETs for switching applications are now available with die on resistances around 1 mΩ and with the capability to handle 85 A. While these die capabilities represent a major advance over what was available just a few years ago, it is important for power MOSFET packaging technology to keep pace. It should be obvious that degradation of a high performance die by the package is undesirable. PowerPAK is a new package technology that addresses these issues. In this application note, PowerPAK's construction is described. Following this mounting information is presented including land patterns and soldering profiles for maximum reliability. Finally, thermal and electrical performance is discussed.

## THE PowerPAK PACKAGE

The PowerPAK package was developed around the SO-8 package (figure 1). The PowerPAK SO-8 utilizes the same footprint and the same pin-outs as the standard SO-8. This allows PowerPAK to be substituted directly for a standard SO-8 package. Being a leadless package, PowerPAK SO-8 utilizes the entire SO-8 footprint, freeing space normally occupied by the leads, and thus allowing it to hold a larger die than a standard SO-8. In fact, this larger die is slightly larger than a full sized DPAK die. The bottom of the die attach pad is exposed for the purpose of providing a direct, low resistance thermal path to the substrate the device is mounted on. Finally, the package height is lower than the standard SO-8, making it an excellent choice for applications with space constraints.

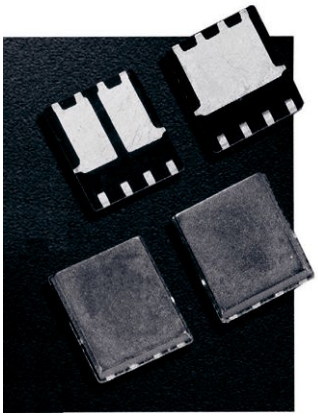
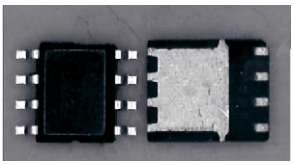


Fig. 1 PowerPAK 1212 Devices

## PowerPAK SO-8 SINGLE MOUNTING

The PowerPAK single is simple to use. The pin arrangement (drain, source, gate pins) and the pin dimensions are the same as standard SO-8 devices (see figure 2). Therefore, the PowerPAK connection pads match directly to those of the SO-8. The only difference is the extended drain connection area. To take immediate advantage of the PowerPAK SO-8 single devices, they can be mounted to existing SO-8 land patterns.



Standard SO-8 PowerPAK SO-8

Fig. 2

The minimum land pattern recommended to take full advantage of the PowerPAK thermal performance see Application Note 826, *Recommended Minimum Pad Patterns With Outline Drawing Access for Vishay Siliconix MOSFETs*. Click on the PowerPAK SO-8 single in the index of this document.

In this figure, the drain land pattern is given to make full contact to the drain pad on the PowerPAK package.

This land pattern can be extended to the left, right, and top of the drawn pattern. This extension will serve to increase the heat dissipation by decreasing the thermal resistance from the foot of the PowerPAK to the PC board and therefore to the ambient. Note that increasing the drain land area beyond a certain point will yield little decrease in foot-to-board and foot-to-ambient thermal resistance. Under specific conditions of board configuration, copper weight and layer stack, experiments have found that more than about 0.25 $in^2$ to 0.5 $in^2$ of additional copper (in addition to the drain land) will yield little improvement in thermal performance.

APPLICATION NOTE



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# PowerPAK® SO-8 Mounting and Thermal Considerations

## PowerPAK SO-8 DUAL

The pin arrangement (drain, source, gate pins) and the pin dimensions of the PowerPAK SO-8 dual are the same as standard SO-8 dual devices. Therefore, the PowerPAK device connection pads match directly to those of the SO-8. As in the single-channel package, the only exception is the extended drain connection area. Manufacturers can likewise take immediate advantage of the PowerPAK SO-8 dual devices by mounting them to existing SO-8 dual land patterns.

To take the advantage of the dual PowerPAK SO-8's thermal performance, the minimum recommended land pattern can be found in Application Note 826, *Recommended Minimum Pad Patterns With Outline Drawing Access for Vishay Siliconix MOSFETs*. Click on the PowerPAK 1212-8 dual in the index of this document.

The gap between the two drain pads is 24 mils. This matches the spacing of the two drain pads on the PowerPAK SO-8 dual package.

## REFLOW SOLDERING

Vishay Siliconix surface-mount packages meet solder reflow reliability requirements. Devices are subjected to solder reflow as a test preconditioning and are then reliability-tested using temperature cycle, bias humidity, HAST, or pressure pot. The solder reflow temperature profile used, and the temperatures and time duration, are shown in figures 3 and 4.

For the lead (Pb)-free solder profile, see www.vishay.com/doc?73257.

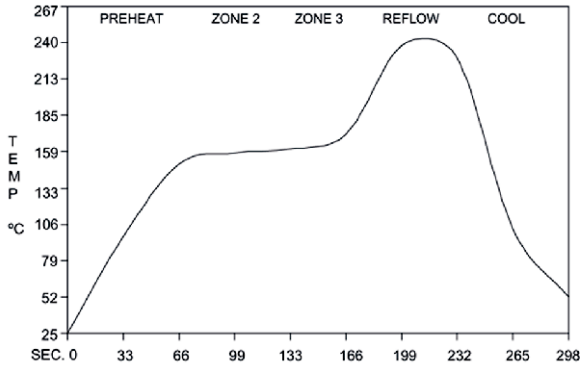



Fig. 3 Solder Reflow Temperature Profile

| | |
|---|---|
| Ramp-Up Rate | + 3 °C /s max. |
| Temperature at 150 - 200 °C | 120 s max. |
| Temperature Above 217 °C | 60 - 150 s |
| Maximum Temperature | 255 + 5/- 0 °C |
| Time at Maximum Temperature | 30 s |
| Ramp-Down Rate | + 6 °C/s max. |

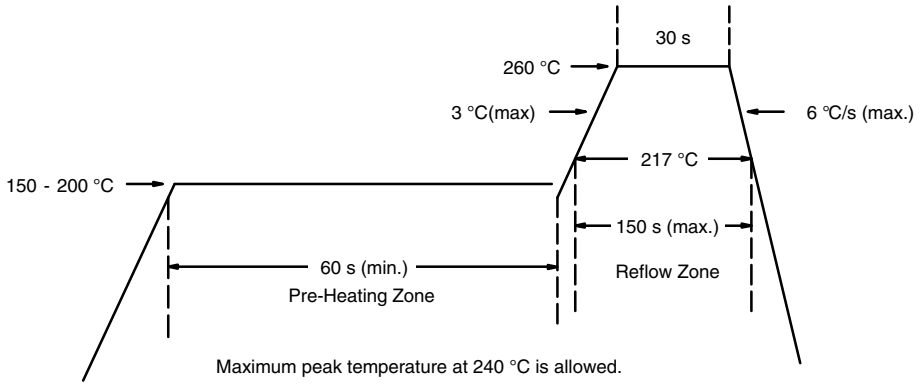



Fig. 4 Solder Reflow Temperatures and Time Durations

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# PowerPAK® SO-8 Mounting and Thermal Considerations

## THERMAL PERFORMANCE

### Introduction

A basic measure of a device's thermal performance is the junction-to-case thermal resistance, $R_{thJC}$, or the junction-to-foot thermal resistance, $R_{thJF}$ This parameter is measured for the device mounted to an infinite heat sink and is therefore a characterization of the device only, in other words, independent of the properties of the object to which the device is mounted. Table 1 shows a comparison of the DPAK, PowerPAK SO-8, and standard SO-8. The PowerPAK has thermal performance equivalent to the DPAK, while having an order of magnitude better thermal performance over the SO-8.

**TABLE 1 - DPAK AND POWERPAK SO-8 EQUIVALENT STEADY STATE PERFORMANCE**

| | DPAK | PowerPAK SO-8 | Standard SO-8 |
|---|---|---|---|
| Thermal Resistance $R_{thJC}$ | 1.2 °C/W | 1 °C/W | 16 °C/W |

### Thermal Performance on Standard SO-8 Pad Pattern

Because of the common footprint, a PowerPAK SO-8 can be mounted on an existing standard SO-8 pad pattern. The question then arises as to the thermal performance of the PowerPAK device under these conditions. A characterization was made comparing a standard SO-8 and a PowerPAK device on a board with a trough cut out underneath the PowerPAK drain pad. This configuration restricted the heat flow to the SO-8 land pads. The results are shown in figure 5.

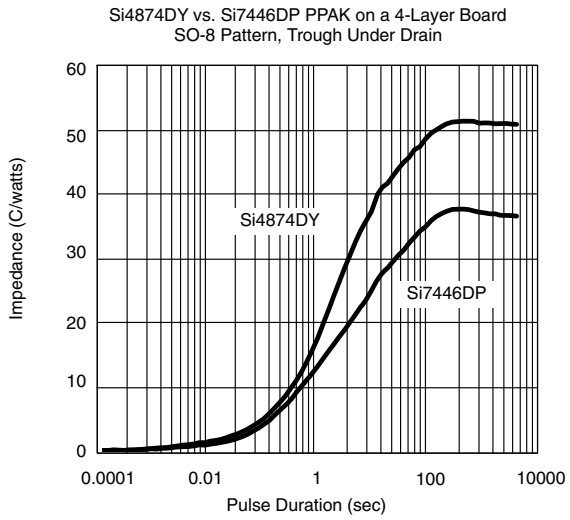



Fig. 5 PowerPAK SO-8 and Standard SO-0 Land Pad Thermal Path

Because of the presence of the trough, this result suggests a minimum performance improvement of 10 °C/W by using a PowerPAK SO-8 in a standard SO-8 PC board mount.

The only concern when mounting a PowerPAK on a standard SO-8 pad pattern is that there should be no traces running between the body of the MOSFET. Where the standard SO-8 body is spaced away from the pc board, allowing traces to run underneath, the PowerPAK sits directly on the pc board.

### Thermal Performance - Spreading Copper

Designers may add additional copper, spreading copper, to the drain pad to aid in conducting heat from a device. It is helpful to have some information about the thermal performance for a given area of spreading copper.

Figure 6 shows the thermal resistance of a PowerPAK SO-8 device mounted on a 2-in. 2-in., four-layer FR-4 PC board. The two internal layers and the backside layer are solid copper. The internal layers were chosen as solid copper to model the large power and ground planes common in many applications. The top layer was cut back to a smaller area and at each step junction-to-ambient thermal resistance measurements were taken. The results indicate that an area above 0.3 to 0.4 square inches of spreading copper gives no additional thermal performance improvement. A subsequent experiment was run where the copper on the back-side was reduced, first to 50 % in stripes to mimic circuit traces, and then totally removed. No significant effect was observed.

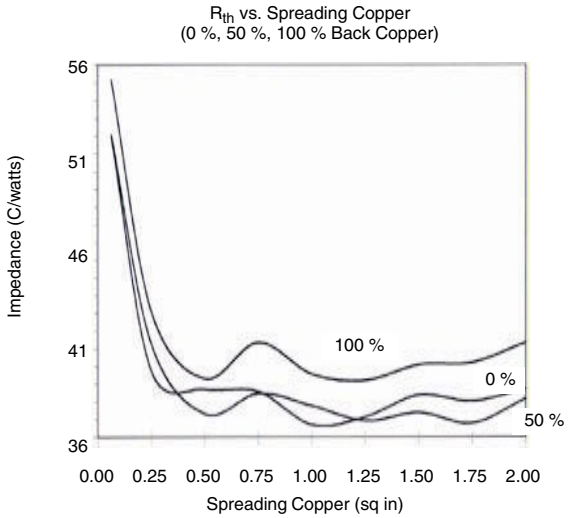



Fig. 6 Spreading Copper Junction-to-Ambient Performance

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# PowerPAK® SO-8 Mounting and Thermal Considerations

## SYSTEM AND ELECTRICAL IMPACT OF PowerPAK SO-8

In any design, one must take into account the change in MOSFET $R_{DS(on)}$ with temperature (figure 7).

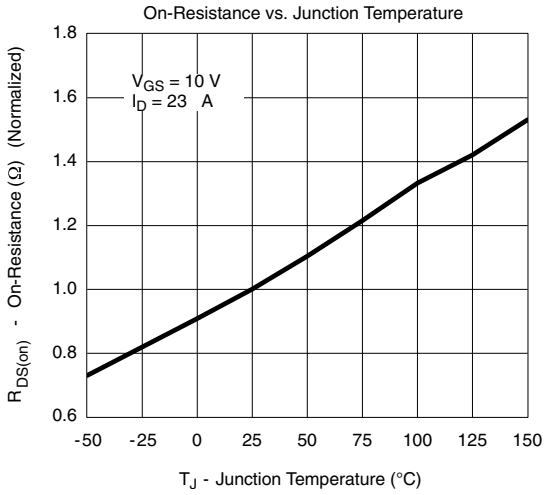



Fig. 7 MOSFET $R_{DS(on)}$ vs. Temperature

A MOSFET generates internal heat due to the current passing through the channel. This self-heating raises the junction temperature of the device above that of the PC board to which it is mounted, causing increased power dissipation in the device. A major source of this problem lies in the large values of the junction-to-foot thermal resistance of the SO-8 package.

PowerPAK SO-8 minimizes the junction-to-board thermal resistance to where the MOSFET die temperature is very close to the temperature of the PC board. Consider two devices mounted on a PC board heated to 105 °C by other components on the board (figure 8).

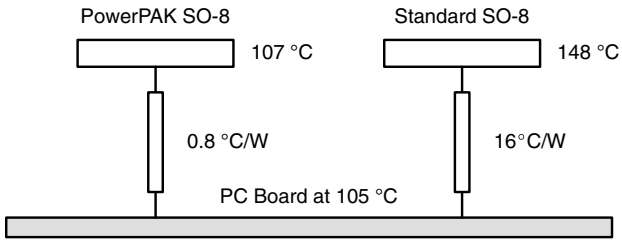



Fig. 8 Temperature of Devices on a PC Board

Suppose each device is dissipating 2.7 W. Using the junction-to-foot thermal resistance characteristics of the PowerPAK SO-8 and the standard SO-8, the die temperature is determined to be 107 °C for the PowerPAK (and for DPAK) and 148 °C for the standard SO-8. This is a 2 °C rise above the board temperature for the PowerPAK and a 43 °C rise for the standard SO-8. Referring to figure 7, a 2 °C difference has minimal effect on $R_{DS(on)}$ whereas a 43 °C difference has a significant effect on $R_{DS(on)}$.

Minimizing the thermal rise above the board temperature by using PowerPAK has not only eased the thermal design but it has allowed the device to run cooler, keep $r_{DS(on)}$ low, and permits the device to handle more current than the same MOSFET die in the standard SO-8 package.

## CONCLUSIONS

PowerPAK SO-8 has been shown to have the same thermal performance as the DPAK package while having the same footprint as the standard SO-8 package. The PowerPAK SO-8 can hold larger die approximately equal in size to the maximum that the DPAK can accommodate implying no sacrifice in performance because of package limitations.

Recommended PowerPAK SO-8 land patterns are provided to aid in PC board layout for designs using this new package.

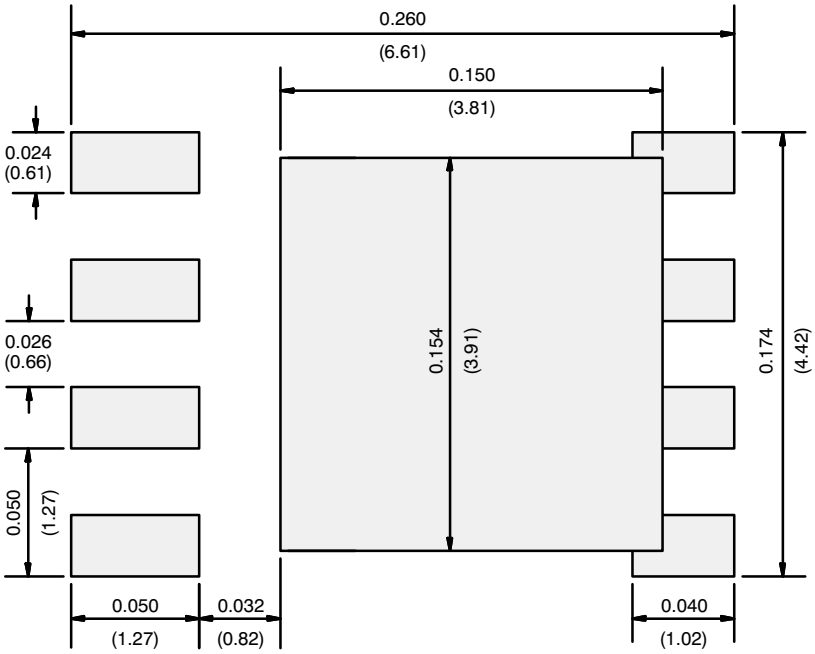
Thermal considerations have indicated that significant advantages can be gained by using PowerPAK SO-8 devices in designs where the PC board was laid out for the standard SO-8. Applications experimental data gave thermal performance data showing minimum and typical thermal performance in a SO-8 environment, plus information on the optimum thermal performance obtainable including spreading copper. This further emphasized the DPAK equivalency.

PowerPAK SO-8 therefore has the desired small size characteristics of the SO-8 combined with the attractive thermal characteristics of the DPAK package.

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## RECOMMENDED MINIMUM PADS FOR PowerPAK® SO-8 Single




Recommended Minimum Pads
Dimensions in Inches/(mm)

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