60V boost, buck and buck-boost LED constant current driver

Check for Samples: LGS6304X

Character

- All ports are protected with ±2000V(HBM)ESD
- Wide input/output voltage range:3.0V-60V
- Support PWM dimming and analog dimming
- Built-in 350mΩ low side MOSFET
- 1.2MHz fixed operating frequency
- Cycle peak current limiting protection
- SKIP mode provides extremely high light load efficiency
- Provide ultra-small SOT23-5 package and enhanced heat dissipation ESOP8 package
- Built-in soft start circuit to prevent current overshoot
- Thermal turn-off protection
- Input undervoltage protection
- Overvoltage protection can provide LED circuit breaker protection
- Internal loop compensation helps reduce solution size, cost and design complexity
- Operating junction temperature range: -40℃ to +125℃

Applications

- Intelligent dimming LED lights
- Wide range LED drive

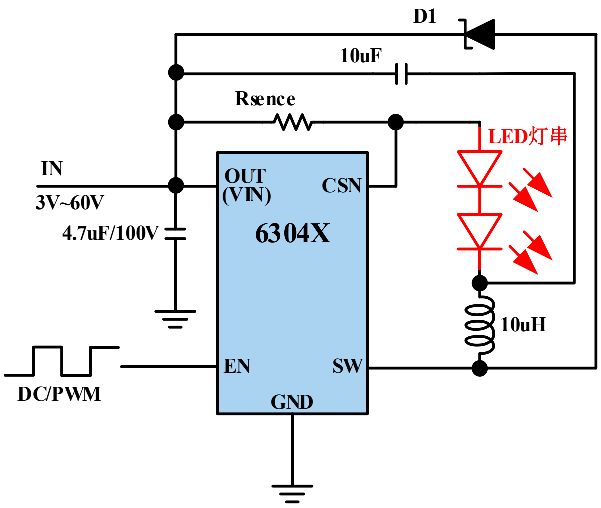

Figure 1. Typical step-down topology in multimode

Description

The LGS6304X is a driver chip with integrated power switching multi-operating modes, wide input/output DC-DC LED, and a wide input voltage range of 3V to 60V.

LGS6304X with integrated 350mΩ power switch; Can provide at least 1.5A peak input current capacity; And its' output current can be adjusted by external sampling resistance.

LGS6304X uses current mode control for excellent response speed and easy loop compensation. It also has SKIP control mode; Combining low static currents with high switching frequencies enables high efficiency over a wide range of load currents.

Additional features include: soft-start, thermal shutdown, Input undervoltage protection, output overvoltage protection and periodic current limiting protection.

To LGS6304X select different resistance sampling resistance R_{Sence} to achieve high precision digital and analog output current regulation, including two specific number LGS63040 and LGS63042:

- LGS63040 supports DC dimming with analog input (0.6V~1.2V)
- LGS63042 supports PWM dimming with digital input (100Hz~100KHz), no screen flash under high-frequency PWM input. The dimming ratio is as high as 25,000:1 when the PWM frequency is 100Hz.

Ordering Information

LGS6304□(□□) **Package**
B5:SOT23-5
EP:ESOP8
Dimming version
0:Analog dimming
2:Only digital dimming

Part	Package
LGS63040B5	SOT23-5
LGS63040EP	ESOP8
LGS63042B5	SOT23-5
LGS63042EP	ESOP8

Historical revision record (†)

RevA V0.1 16.Aug.2021	**page number**
※A version of the original	
The parameters in this manual only describe and acknowledge the indicators in version A	ALL

RevA V0.2 4.Jan.2022	**page number**
※A version of the modified	
Modify related parameters of version A, optimize the chart section	ALL

RevA V0.3 10.Jun.2022	**page number**
※A version of the modified	
Added information about ESOP8 and SOT23-6 package	ALL

RevA V0.4 21.Jul.2022	**page number**
※A version of the modified	
Add ordering information, modify some page header information	ALL

†NOTE: Page numbers of previous editions may differ from those of the current edition.

Absolute Maximum Ratings (†)

Table 1

Parameter	Range
Pin to GND Voltage（VIN,SW）	-0.3V~60V
Pin to GND Voltage（EN,OVP）	-0.3V~6V
Pin to GND Voltage（CSN）	VIN-6~VIN+0.3V
Maximum current of switch tube	3A
Storage temperature	-65℃ to 150℃
Operating junction temperature	-40℃ to 125℃
ESD Value（HBM）	±2KV
ESD Value（CDM）	±500V

† NOTE：If the operating conditions of the device exceed the absolute maximum, the device may be permanently damaged. This is only a limit parameter and it is not recommended that the device operate at or above the limit value. The reliability of devices may be affected by long time operation in limiting conditions.

Pin arrangement

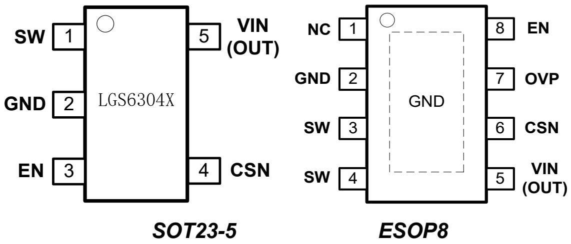

Figure 2. Encapsulation and pin arrangement

ESD warning

ESD (Electrostatic discharge) Sensitive devices.

Electric devices and circuit boards can be electrically charged without being noticed. Though this product has a patented or proprietary protection circuit, the device may be damaged in the event of high energy ESD. Therefore, appropriate ESD preventive measures should be taken to avoid device performance degradation or function loss.

Table 2 Description of pin function

Pin number		pin name	instructions
SOT23-5	ESOP-8		
1	3,4	SW	Internal power switch node. Externally connected to power inductor and Schottky diode.
2	2	GND	Ground pin.
3	8	EN	Dimming input pin, can input DC and PWM square wave for dimming, see "dimming Settings" for details.
4	6	CSN	LED current detection pin. Connect to external LED current sampling resistor R_{Sence}. The output current is determined by $V_{OUT(VIN)} - V_{CSN}$ and R_{Sence}, which can be set by this formula: $I_{OUT} = (V_{OUT(VIN)} - V_{CSN}) / R_{Sence}\ (A)$。
5	5	VIN (OUT)	Output voltage detection point or input voltage connection point，connects the LED current sampling resistor to the CSN end. It is used as an input voltage detection point in buck circuit and as an output voltage connection point in boost and lift applications.
-	1	NC	No external component is required. Ground the pin
-	7	OVP	Overvoltage protection pin，is connected to the output pin and the partial voltage resistor at ground.

Technical specifications

Limits apply to operating junction temperatures (T_J) ranging from -40℃ to +125℃ unless otherwise specified. Minimum and maximum limits are specified by test, design or statistical correlation. Typical values represent the most likely parameter specifications when T_J=25℃, for reference only. All voltages are relative to GND.

Table3.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Characteristics						
V_{IN}	Operating Input Voltage Range		3.0		60	V
V_{UVLO}	VIN undervoltage lock	Rising		3.0		V
	VIN undervoltage lock	Falling		2.6		V
I_Q	Operating quiescent current	No load， No switch, IN=12V		180		uA
I_S	Shutdown quiescent current	EN=0,IN=12V		10		uA
Switching Characteristics						
R_{DSON}	MOSFET R_{DSON}	TJ= 25℃	330	350	410	mΩ
V_{OUT}-V_{CSN}	LED Current sampling voltage		0.195	0.2	0.205	V
F_{SW}	Switching frequency	PWM Operation	1.05	1.2	1.35	MHZ
F_{SW_FB}	Switching frequency during soft start	IN=12V，EN=1		1/4F_{SW}		MHZ
T_{onmin}	Minimum on-off time			120		ns
$I_{LIMIT.SW(Peak)}$	Peak Current Limit		1.5	1.7	2.1	A
$I_{SW.LKG}$	Input leakage current at SW pin				4	uA
EN pin /Dimming(3V≤VIN≤60V)						
V_{EN_min}	Analog dimming lower limit voltage 63040	3V≤IN≤60V	0.6	0.62	0.65	V
V_{EN_max}	Analog dimming upper limit voltage 63040	3V≤IN≤60V	1.2	1.22	1.25	V
V_{EN_H}	Digital dimming rising edge 63042	EN=0 ↑ EN=1	0.31	0.5	0.54	V
V_{EN_L}	Digital dimming falling edge 63042	EN=1 ↓ EN=0	0.25	0.35	0.38	V
I_{EN}	EN Input current	V_{EN}=5V	5		10	uA
f_{EN}	PWM dimming frequency range 63042		100		100K	HZ
Thermal protection characteristic						
T_{OTP-R}	Over temperature protection	TJ Rising		150		℃
T_{OTP-F}	The overtemperature protection is removed	TJ Falling		120		℃
Thermal resistivity						
θ_{JA}	The thermal resistance coefficient from the silicon core to the surrounding air	0 LFPM Air Flow		173		℃/W
θ_{JB}	Thermal resistance coefficient between silicon core and PCB surface			33.2		℃/W
θ_{JCtop}	Thermal resistance coefficient of silicon core to upper surface of package			116		℃/W
Ψ_{JB}	Thermal resistance coefficient between silicon core and PCB surface			30		℃/W

Functional block diagram

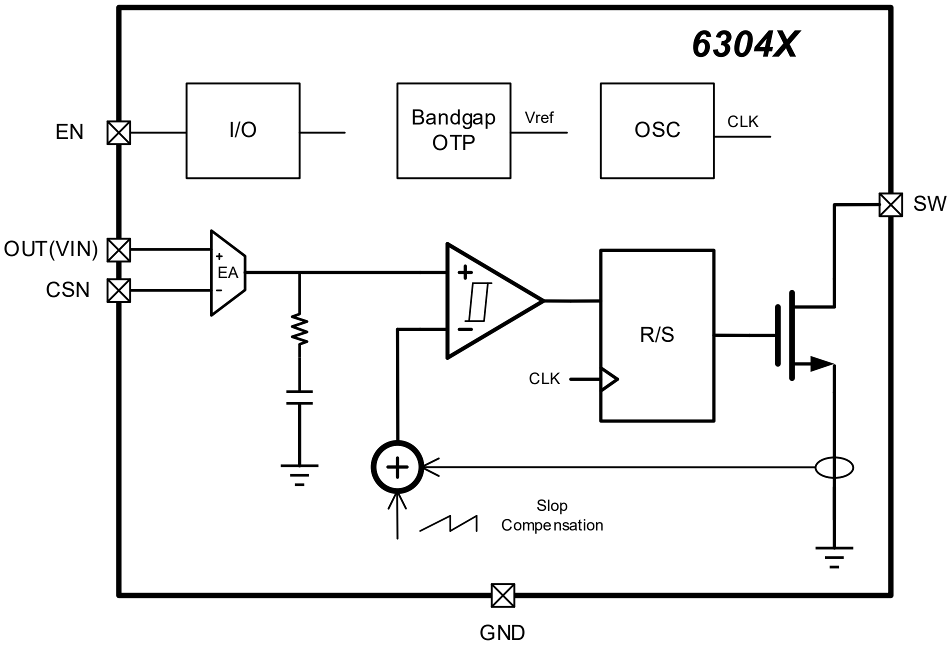

Figure3. Internal function block diagram

Application information: Typical application circuit

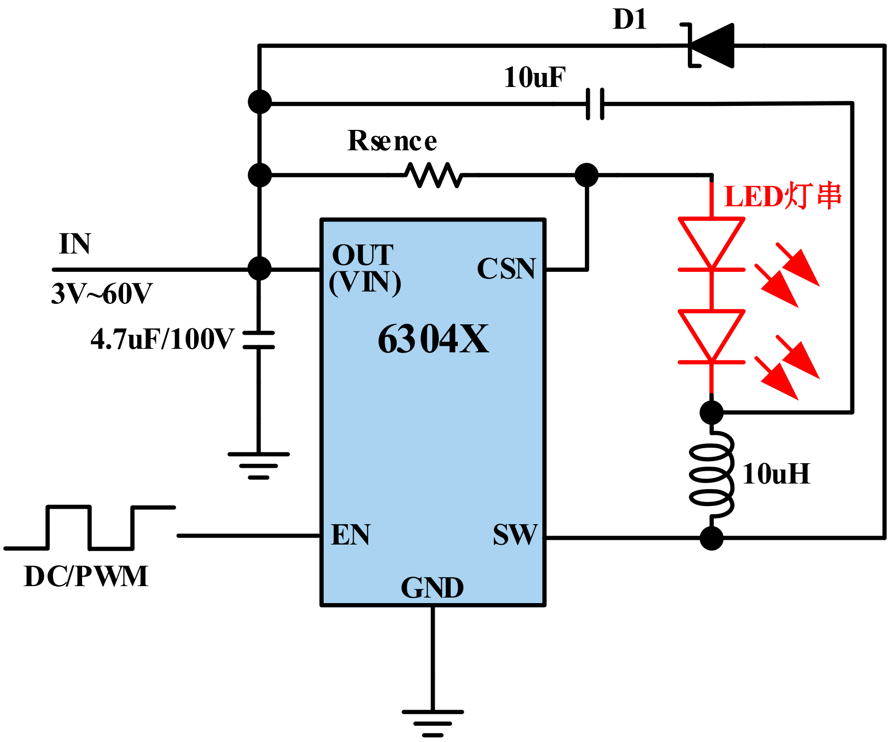

Figure 4.a Typical application topology of LGS6304X buck mode (VIN>VLED)

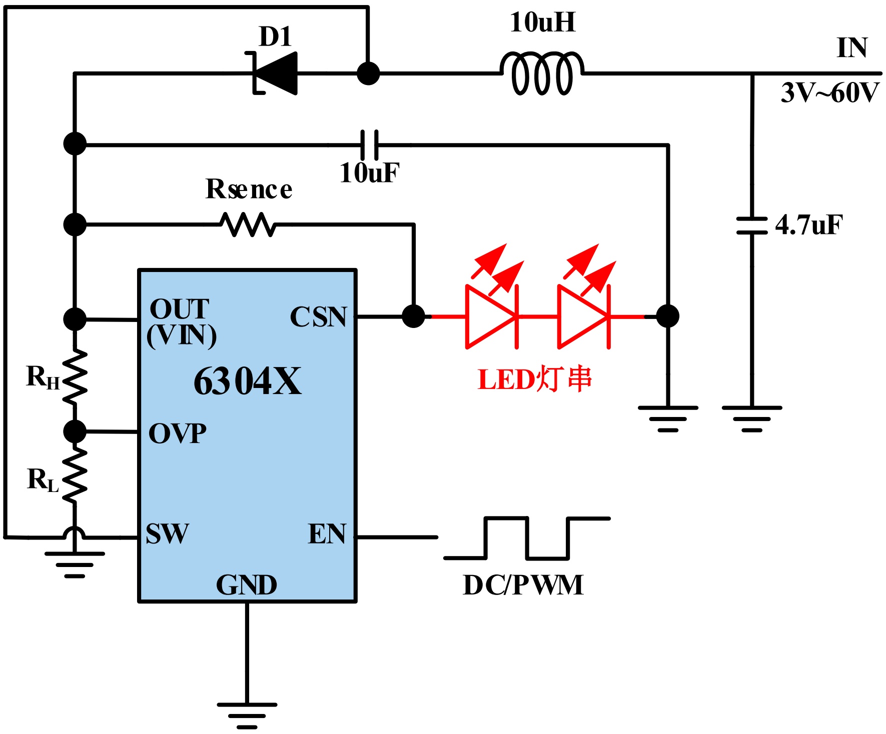

Figure 4. b Typical application topology of LGS6304X boost mode (VIN<VLED)

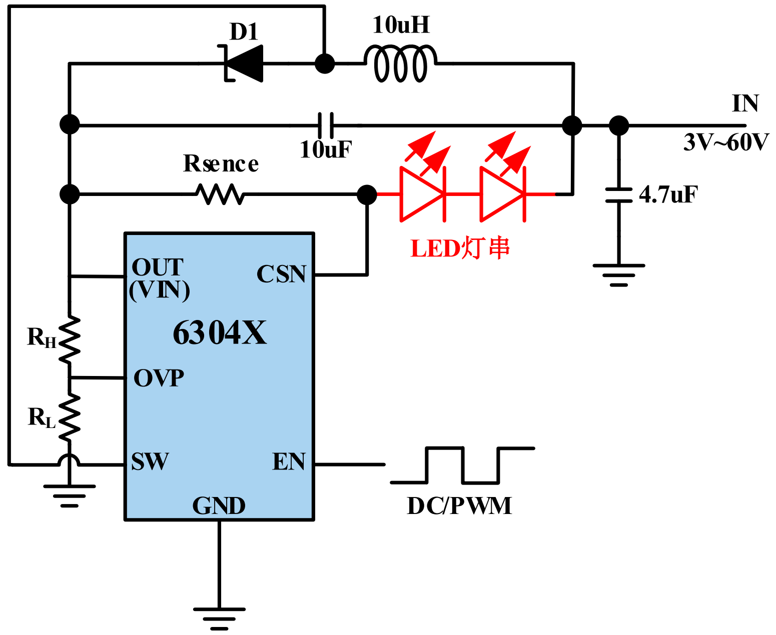

Figure 4. c Typical application topology of LGS6304X boost/buck mode (V_{IN}<V_{LED} 或 V_{IN}>V_{LED})

NOTE:

- CSN pin, connected to external LED sampling resistor. The output constant current value can be set by R_{Sence} , and the output current is determined by $V_{OUT(VIN)} - V_{CSN}$ and R_{Sence} , which can be set by this formula:

  $I_{OUT} = (V_{OUT(VIN)} - V_{CSN}) / R_{Sence} (A)$。
- The input capacitor is recommended to be X7R or X5R ceramic capacitor of 10uF, and should be placed as close as possible to the VIN pin of the power input and GND pin.
- LGS6304X in ESOP8 package is recommended for boost and lift applications. The package chip has OVP pins to protect the circuit in the case of LED ball break.

Application information: Feature Description

Overview

LGS6304X is a driver chip with integrated power switching multi-operating modes, wide input/output DC-DC LED, and a wide input voltage range of 3V to 60V. LGS6304X with integrated 350mΩ power switch; Can provide at least 1.5A peak input current capacity; And its' output current can be adjusted by external sampling resistance. LGS6304X uses current mode control for excellent response speed and easy loop compensation. It also has SKIP control mode; Combining low static currents with high switching frequencies enables high efficiency over a wide range of load currents.

Additional features include: soft-start, thermal shutdown, Input undervoltage protection, output overvoltage protection periodic current limiting protection.

Set output current

LGS6304X output current can be adjusted by external sampling resistance divider. The output current can be calculated according to $V_{OUT(VIN)} - V_{CSN}$ and $\mathrm{R_{Sence}}$. The typical value of $V_{OUT(VIN)} - V_{CSN}$ is 0.2V. The recommended value of output current is shown in the following table:

$$I_{OUT} = \frac{V_{OUT(VIN)} - V_{CSN}}{R_{Sence}} \quad (A)$$

Table 4. Output current setting quick configuration

I_{OUT}	R_{SENCE}	Error precision (1)
10mA	20Ω	10mA
20mA	10Ω	20mA
100mA	2Ω	100mA
200mA	1Ω	200mA
400mA	0.5Ω	400mA
800mA	0.25Ω	800mA

(1) Other sampling resistors and high precision resistors can also be selected to achieve higher setting accuracy.

SKIP pulse mode

LGS6304X built-in jump pulse circuit; In light load, the circuit is closed; Switch only when necessary to keep the output voltage within the specified range. This reduces switching losses and allows the converter to maintain high efficiency under light load conditions.

In SKIP pulse mode, when the output voltage falls below the specified value, LGS6304X enters the PWM mode, and stays for several oscillator cycles, so that the output voltage rises to the specified range. During the waiting time between burst pulses, the power switch is disconnected and all load currents are supplied by the output capacitor. The output voltage ripple in this mode is larger than that in PWM mode because the output voltage will drop and recover irregularly.

Input undervoltage protection (VULO)

An internal undervoltage locking circuit is included on the VIN pin of the device. When the VIN voltage falls below the UVLO drop threshold, UVLO protection will be triggered and the regulator output will be turned off. The UVLO rise threshold is about 3.0V. After VIN reaches this voltage and removes the UVLO, the controller will enter the soft start process.

Soft-Start

Soft Start of LGS6304X can prevent underdamped overshoot of converter input power during start up. When the chip is started, the internal circuit generates a Soft Start voltage (SS), while the switching frequency drops to 1/4 of the maximum switching frequency, and the current rises at a fixed rate of rise. During soft start, the output voltage will track the internal node voltage ramp proportionally.

When it is less than the internal reference voltage (REF), SS replaces REF, so the error amplifier uses SS as the reference. When SS exceeds REF, REF restores control. The switching current limit is still in effect throughout the startup phase, and can be very reliable to avoid the situation of short-circuit on power-on.

When the output has a very large capacitance (e.g., 2200uF or greater), the output voltage will rise more slowly than the SS, and the time to start up to the target voltage set point will be prolonged due to the maximum switching current limi

Application information: Feature Description

Thermal shutdown protection

The thermal overload protection circuit limits the junction temperature below 150℃(typical value). Under extreme conditions (high ambient Temperature and/or high power consumption), when the junction Temperature begins to rise above 150℃ Over Temperature Protection (OTP) is activated and the regulator output (if EN is enabled) will be forcibly shut down. When the junction temperature drops below 130°C, the OTP state is unlocked, the voltage regulator output is restarted, and the output current is restored to its normal operating value.

The guaranteed junction temperature range of this device is -40°C to 125°C. High junction temperature will reduce the working life; The device lifetime is shortened when the junction temperature is higher than 125°C for a long time. Please note that the maximum ambient temperature consistent with these specifications depends on the specific operating conditions as well as circuit board layout, rated package thermal resistance, and other environmental factors.

Current limiting protection switch

cycle overcurrent limit. When SW current is triggered $I_{LIMIT.SW(Peak)}$, LGS6304X output will enter the periodic limit current state.

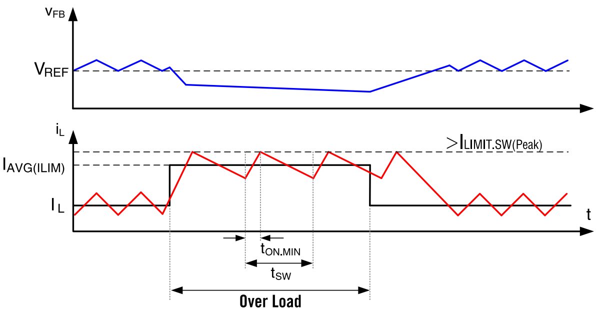

Figure 5. LGS6304X output overcurrent with M_{top} behavior

$I_{LIMIT.SW(Peak)}$ is related to inductance size and input pressure difference, and $I_{LIMIT.SW(Peak)}$ is only the reference minimum. Global OTP protection may be triggered in case of prolonged overcurrent or short circuit.

EN Dimming instructions

EN is the enabled input pin of the chip. The pin has two independent thresholds, a rise threshold greater than 0.5V enables the output, and a fall below 0.4V turns off the voltage regulator output to enter the low-power sleep mode. An 800K pull-down is provided inside this pin. External logic signal can be used to drive EN inputs for system sorting and protection. As the internal pull-down is weak, the external pull-down resistor can be turned off if necessary. It is not recommended to leave this pin hanging empty.

Table5. EN working state

Pin	Port type	Pin state	Function
EN	input	High level	Chip Output open
		Low level	Chip Output shut down

LGS63040 Analog dimming

LGS63040 supports analog dimming (0.6V~1.2V). DC voltage VEN can be added to the EN terminal to reduce the LED output current. The maximum output LED current is determined by the sampling resistance. The formula for calculating the real-time average output current of LED simulation dimming is as follows:

$$I_{OUT} = \frac{0.2 \times (V_{EN} - 0.6)}{0.6 \times R_{Sence}} (0.6V \le V_{EN} \le 1.2V)$$

When V_{EN} is greater than 1.2V and less than 6V, the LED current shall be 100% equal to the set LED maximum average current.

LGS63042 PWM dimming

LGS63042 support PWM dimming, with PWM dimming, LED output current can be changed from 0% to 100%. The LED brightness is determined by the duty cycle of the PWM signal. For example, the PWM signal is 25% duty cycle, and the average LED current is $(0.2/R_{Sence})$ 25%. It is recommended to set the PWM dimming frequency above 120Hz to prevent human eyes from seeing the LED flicker. Compared with analog

Application information: Feature Description

dimming, PWM dimming has the advantage of not changing the chroma of LED.

- LGS63042 supports digital input (100Hz~ 100KHz) PWM dimming, no screen flash under high-frequency PWM input. The dimming ratio is as high as 25,000:1 when the PWM frequency is 100Hz.

In contrast, we can see that LGS63042 dimming frequency support range will be wider, up to 100KHZ, dimming ratio is also higher, have PWM dimming needs more recommended to choose LGS63042.

The calculation formula of real-time average output current of PWM dimming of LGS63042 is:

$$I_{OUT}=\frac{0.2\times D}{R_{Sence}}\left(0\%\le D\le 100\%,\ 0.6V\le V_{EN}\le 6V\right)$$

Among them： D is the duty cycle of PWM.

Output overvoltage protection

The output overvoltage protection circuit can prevent the LED lamp beads from breaking and damaging the chip. According to the actual number of LED beads, set the overvoltage protection threshold through the proportion of external circuit. The typical value of OVP trigger voltage is 1V, and the recovery voltage is 0.9V

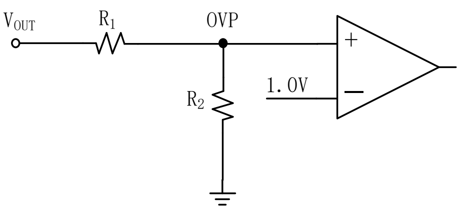

Figure 6. Setting OVP voltage

The overvoltage protection threshold can be calculated according to the following formula:

$$V_{OUT\_OVP}=\left(1+\frac{R_1}{R_2}\right)\times 1.0\ \ (V)$$

You are advised to set the overvoltage protection threshold to 1.3 to 1.5 times of the normal output voltage.

Input capacitance C_{IN}

The typical input capacitance is 4.7μF, and larger capacitance can be used if further input/output ripple reduction is required. The capacitive reactance of the input capacitor should be as small as possible at the switching frequency. Ceramic capacitors X5R or X7R are recommended. To minimize potential input noise problems, place the ceramic capacitor near the IN and GND pins to reduce the loop area formed by CIN and IN/GND pins.

Output capacitance C_{OUT}

Output capacitors are selected to handle output current ripple noise. For best performance, ceramic capacitors with capacity of 10μF and material X5R or X7R are recommended. If it is necessary to use the PWM dimming mode of the chip, in order to solve the noise problem caused by the piezoelectric effect of the output capacitor in this case, there are two ways to reduce the problem:

(1) It is recommended to use tantalum capacitors, thin film capacitors and other capacitors without piezoelectric effect or ceramic chip plug-in capacitors instead of ceramic capacitors. This method abandons the advantages of light and thin MLCC, so it is necessary to consider the volume space, reliability and cost in practical application.

(2) It is recommended to use LGS63042 when PWM dimming is needed. The high dimming frequency of the chip can avoid the range of human ear recognition, so as to achieve the purpose of eliminating the capacitor noise.

Application information: Feature Description

Output diode D

The LGS6304X requires an external continuation diode between the SW pin and the output point. The reverse voltage rating of the selected diode must be greater than V_{OUTMAX} and the peak current rating of the diode must be greater than the maximum inductor current. Schottky diodes are recommended for optimal efficiency due to their low forward voltage drop and fast switching speed.

Output inductance L

Inductor selection needs to consider the following aspects:

Select the inductor to provide the required current ripple. It is recommended that the current ripple be about 40% of the maximum output current. The inductance calculation formula is as follows:

$$L = \frac{V_{OUT} \times \left(1 - V_{OUT}/V_{IN,MAX}\right)}{f_{SW} \times I_{OUT(MAX)} \times K}$$

f_{SW} is the switching frequency, $I_{OUT(MAX)}$ is the LED current, and the constant K is the percentage of the inductor current ripple.

For LGS6304X, the optimal inductance range for the BUCK topology in typical application circuits is 10μH to 47μH. The recommended inductance value is 10μH for optimal loop stability and efficiency.

(2) In order to ensure the safety of the circuit, the saturation current rating of the inductor must be greater than the peak current under full load condition. It is recommended that the saturation current of the inductor exceed the peak current of the normal operation by 30%-40%. The peak current of the inductor can be calculated according to the following formula:

$$I_{L(PEAK)} = I_{OUT(MAX)} + \frac{V_{OUT} \times \left(1 - V_{OUT}/V_{IN,MAX}\right)}{2 \times f_{SW} \times L}$$

Application Information: Typical application feature

unless otherwise specified，L=10μH，C_{OUT}=10μF，T_A=25℃，Buck Application Circuit

Figure 7.1 Efficiency vs Input Voltage

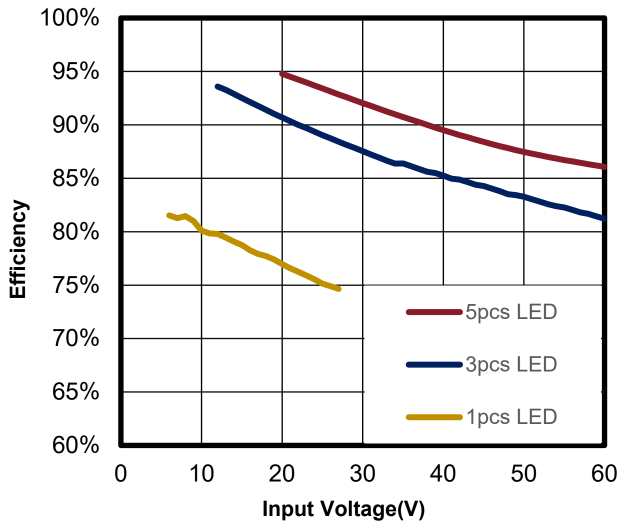

Figure 7.1.a I_{OUT}=400mA

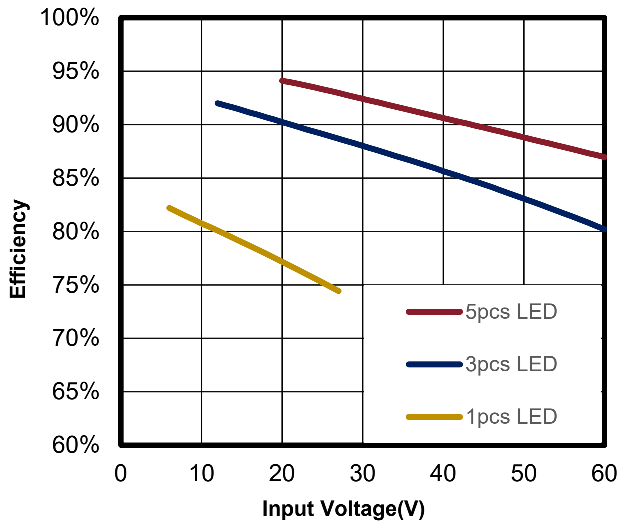

Figure 7.1.b I_{OUT}=800mA

Figure 11.2LED Current vs Input Voltage

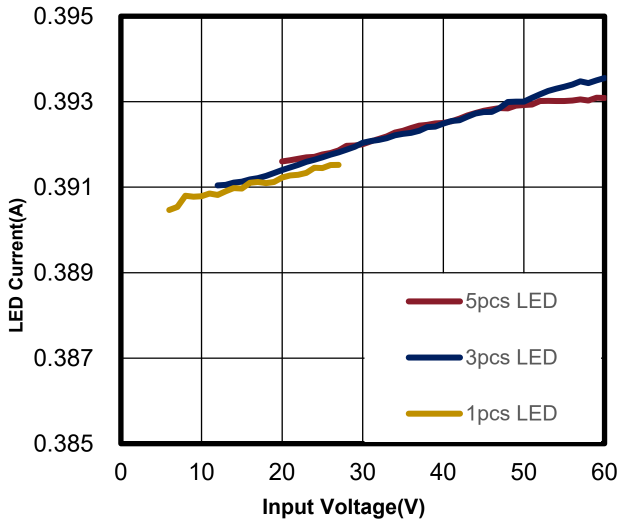

Figure 7.2.a I_{OUT}=400mA

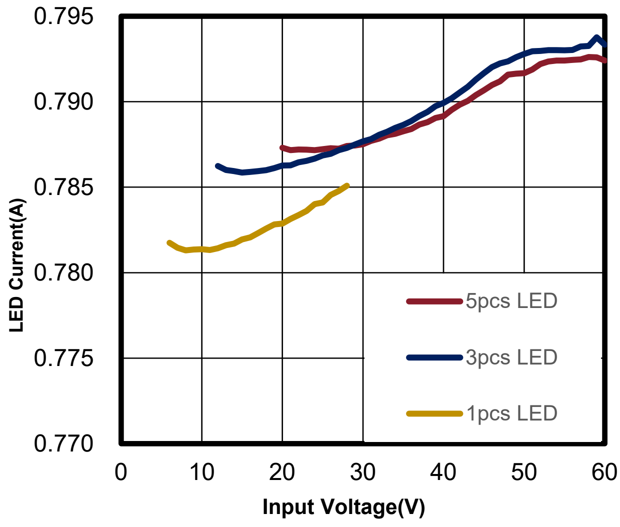

Figure 7.2.a I_{OUT}=800mA

Application Information: Typical application feature

unless otherwise specified, L=10μH, C_{OUT}=10μF, T_A=25℃, Buck Application Circuit

Figure 8.1Analog Dimming Curve

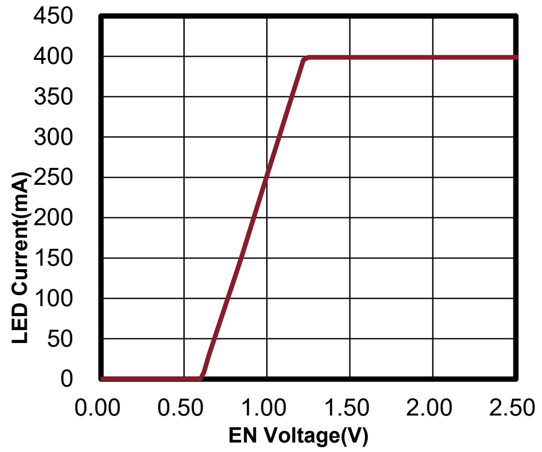

Figure 8.1.a LGS63040, V_{IN}=30V,3pcs LED Series

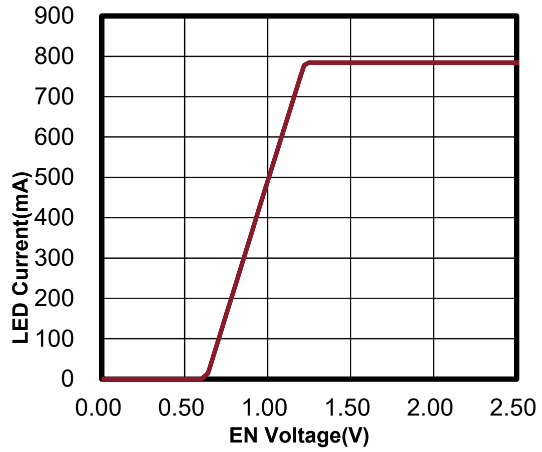

Figure 8.1.b LGS63040, V_{IN}=30V,3pcs LED Series

Figure 12.2PWM Dimming Curve

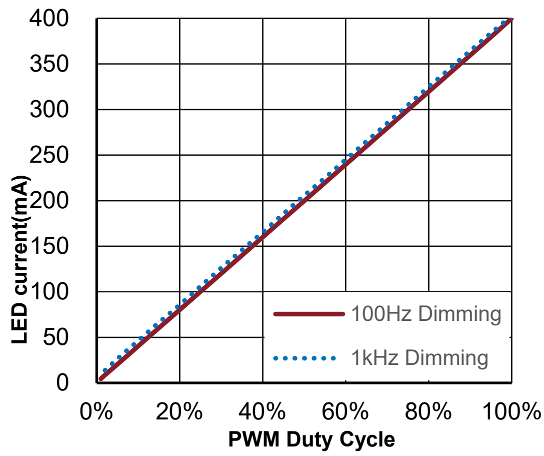

Figure 8.2.a LGS63040, V_{IN}=30V,3pcs LED Series

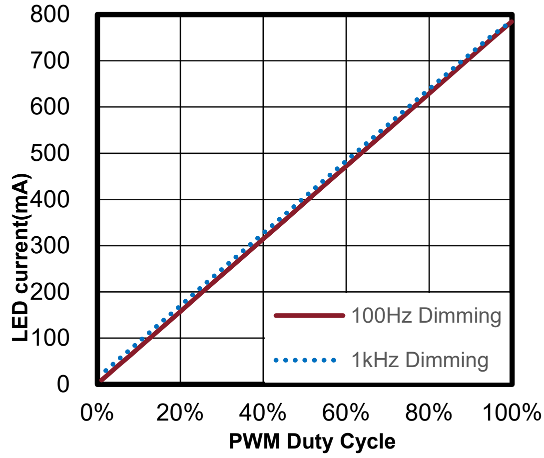

Figure 8.2.b LGS63040, V_{IN}=30V,3pcs LED Series

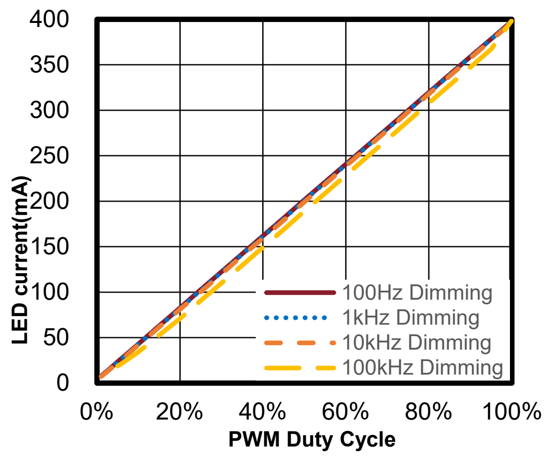

Figure 8.2.c LGS63042, V_{IN}=30V,3pcs LED Series

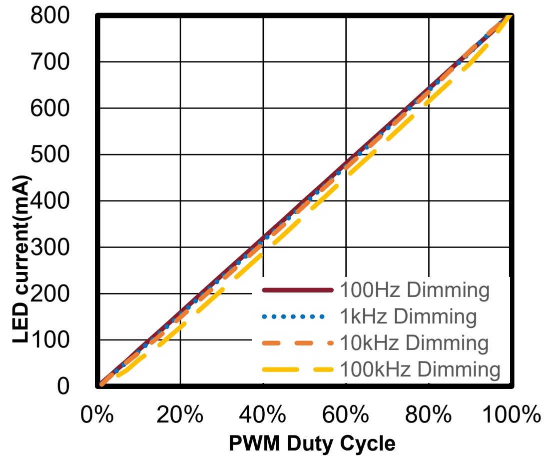

Figure 8.2.d LGS63042, V_{IN}=30V,3pcs LED Series

Application Information: Typical application feature

unless otherwise specified, L=10μH, C_{OUT}=10μF, T_A=25℃, Buck Application Circuit

Figure 9.1 Start-Up/Shut-down Waveforms

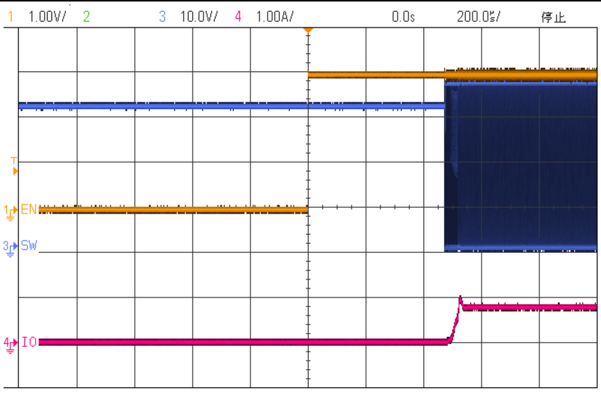

Figure 9.1.a V_{IN}=36V, I_{OUT}=800mA,3pcs LED Series

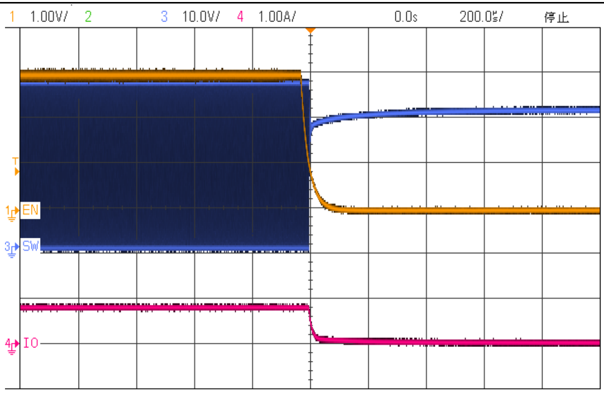

Figure 9.1.b V_{IN}=36V, I_{OUT}=800mA,3pcs LED Series

Figure 9.2PWM Dimming Transient

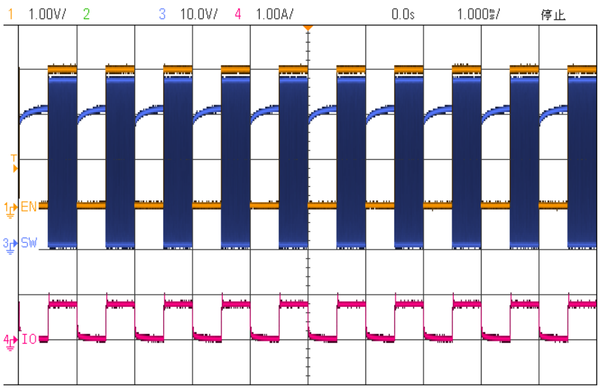

Figure 9.2.a LGS63040, V_{IN}=36V, I_{OUT}=800mA,3pcs LED Series

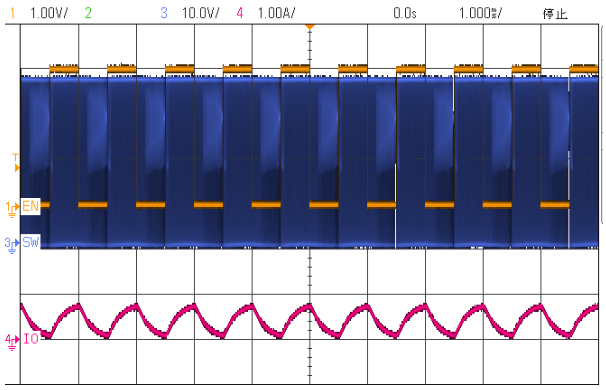

Figure 9.2.b LGS63042, V_{IN}=36V, I_{OUT}=800mA,3pcs LED Series

Figure 9.3OTP Waveforms

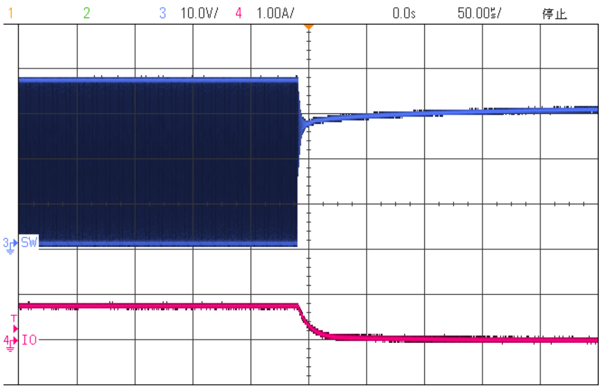

Figure 9.3.a V_{IN}=36V, I_{OUT}=800mA, 3pcs LED Series

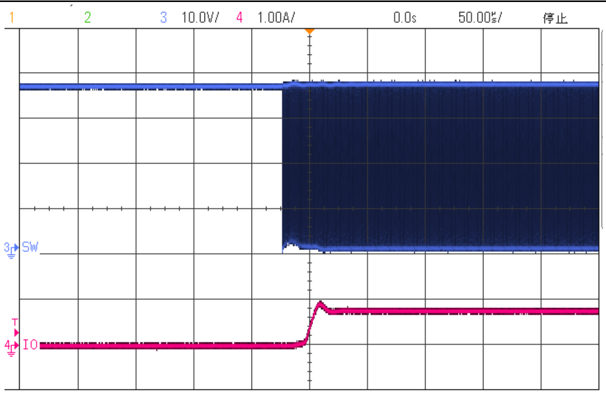

Figure 9.3.b V_{IN}=36V, I_{OUT}=800mA, 3pcs LED Series

Application Information: Typical application feature

unless otherwise specified， L=10μH， C_{OUT}=10μF， T_A=25℃， Buck Application Circuit

Figure 10.1 Start-Up/Shut-down Waveforms

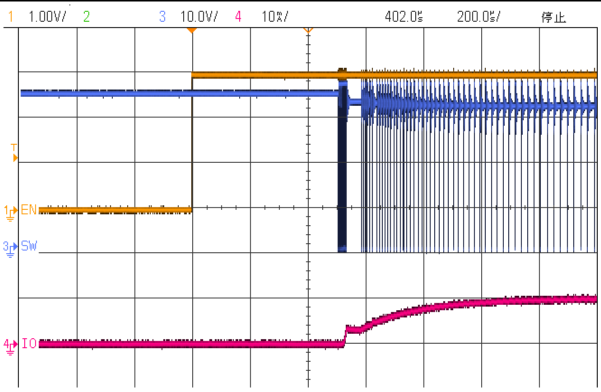

Figure 10.1.a V_{IN}=36V, I_{OUT}=10mA, 3pcs LED Series

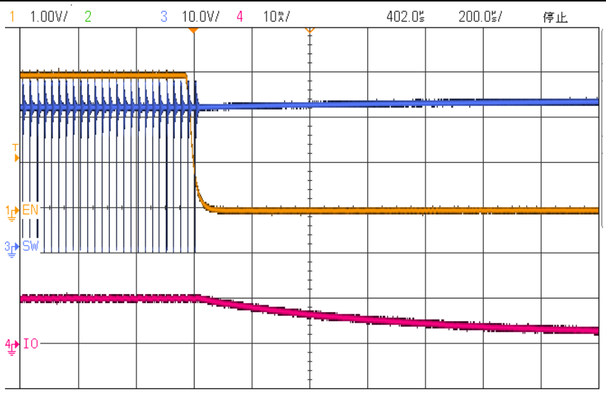

Figure 10.1.b V_{IN}=36V, I_{OUT}=10mA, 3pcs LED Series

Figure 10.2 PWM Dimming Transient

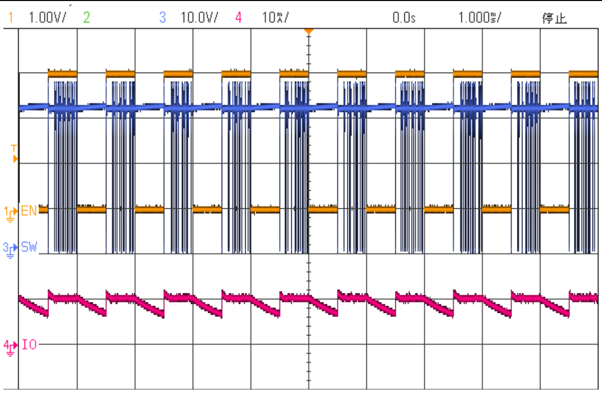

Figure 10.2.a LGS63040, V_{IN}=36V, I_{OUT}=10mA, 3pcs LED Series

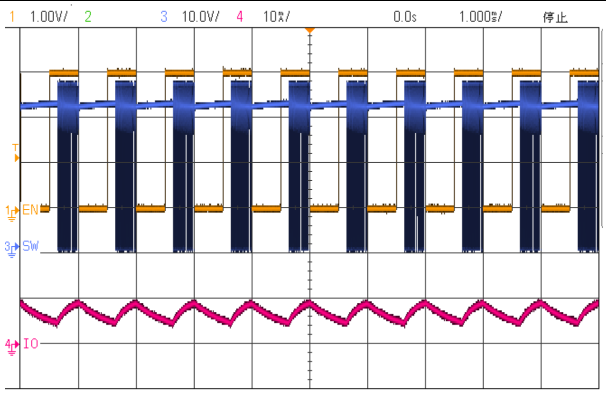

Figure 10.2.b LGS63042, V_{IN}=36V, I_{OUT}=10mA, 3pcs LED Series

Figure 10.3 Switching Waveforms

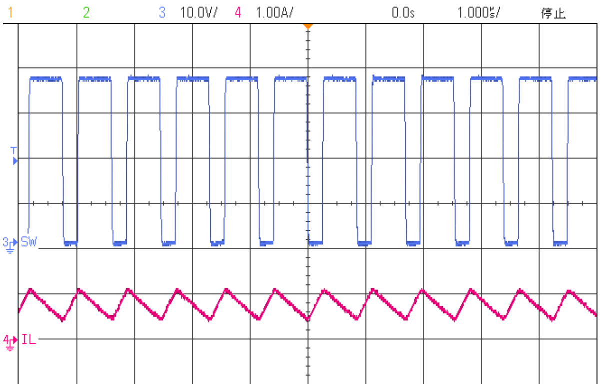

Figure 10.3.a V_{IN}=36V, I_{OUT}=800mA, 3pcs LED Series, CCM Mode

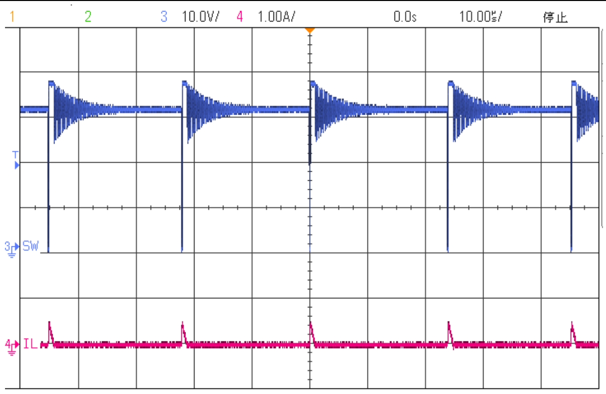

Figure 10.3.b V_{IN}=36V, I_{OUT}=10mA, 3pcs LED Series, Pulse Skip Mode

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Application information: Layout reference

Overview

LGS6304X high integration makes PCB layout very simple and easy. Poor layout will affect the performance of LGS6304X, resulting in electromagnetic interference (EMI), electromagnetic compatibility (EMC) poor, ground hopping and voltage loss, and then affect voltage regulation and stability. In order to optimize its electrical and thermal performance, the following rules should be applied to achieve good PCB layout and wiring to ensure the best performance:

- The high frequency ceramic input capacitor CIN must be placed near the VIN and GND pins as close as possible to reduce the high frequency noise.
- Use large PCB copper-clad areas including GND pins for high current paths. This helps minimize PCB conduction losses and thermal stress.
- The PCB copper area associated with the SW pin must be reduced to avoid potential noise interference problems.
- To minimize through-hole conduction losses and reduce module thermal stress, multiple through-holes should be used for interconnection between the top layer and other power layers or formations.
- CSN pin impedance is high, the lead track should be as short as possible and away from the high noise SW node or shielded.
- Add through-holes and Windows to the heat sink pad at the bottom of ESOP8 package chip to help heat dissipation and improve efficiency.

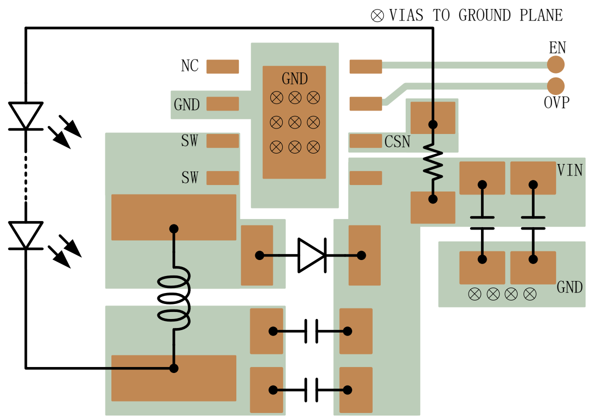


Figure 11.1 Typical application PCB layout of BUCK ESOP8 package

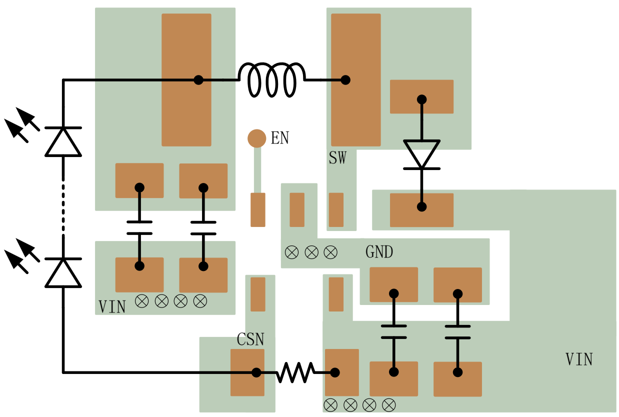
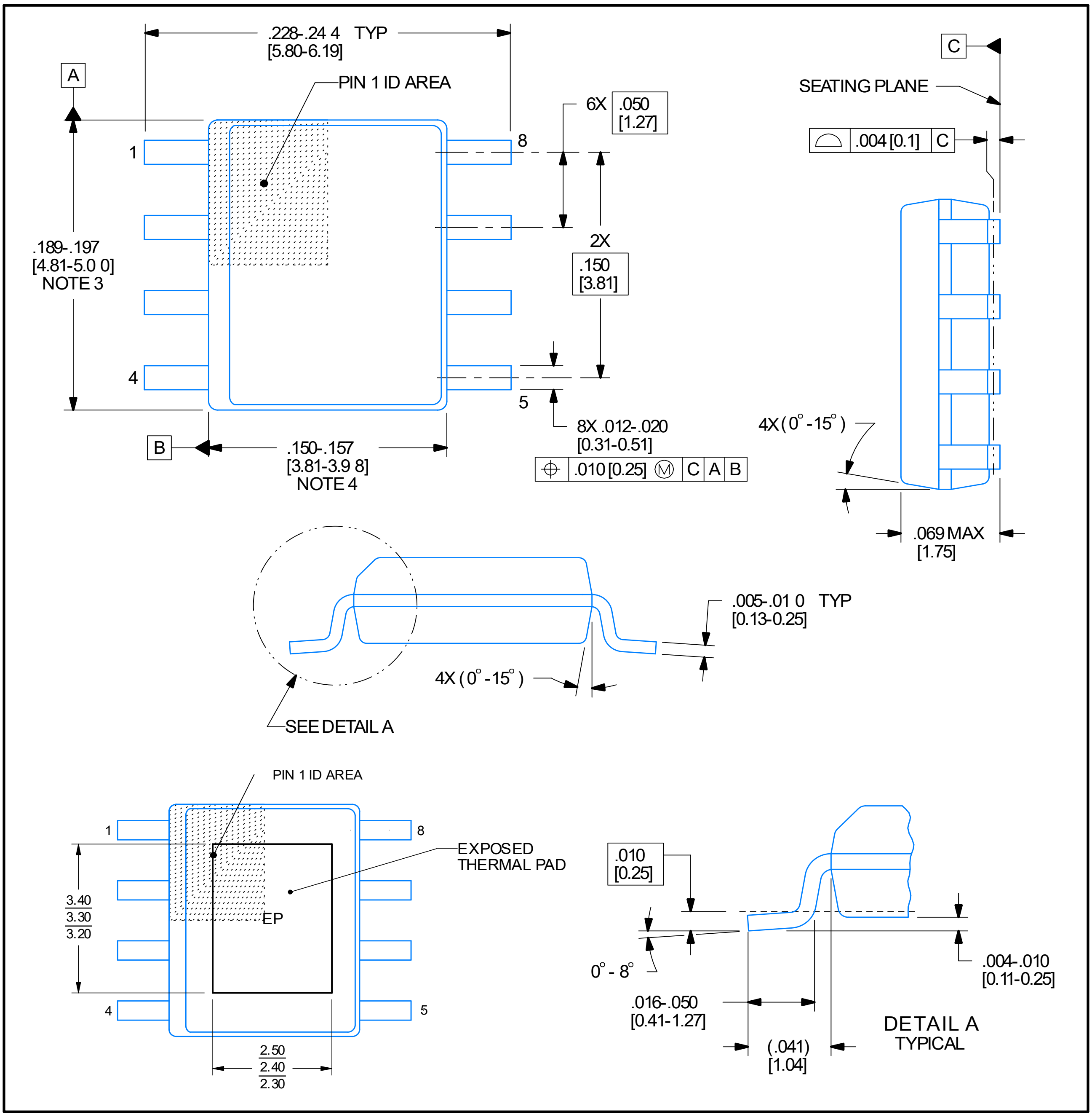


Figure 11.2 Typical application PCB layout of BUCK SOT23-5 package

Package Outline Description (ESOP8)

8-pin plastic seal SOIC with bottom EPAD



NOTE:

(1) All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

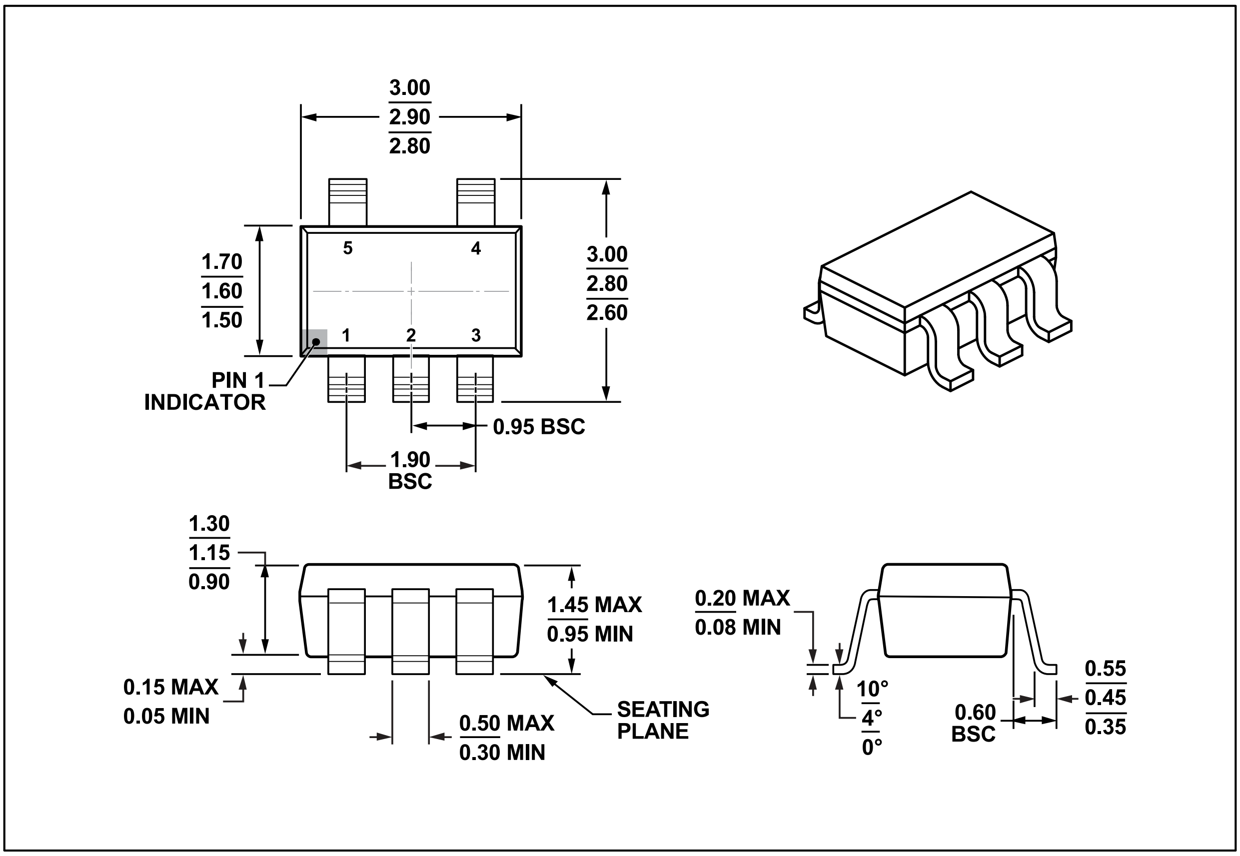
(2) This drawing is subject to change without notice.

(3) This dimension does not include mold burrs, protrusions, or nozzle burrs. The burrs or protrusions on each side of the mold shall not exceed 0.15mm.

(4) This dimension does not include mold burrs, and the burrs or protrusions on each side of the mold do not exceed 0.25 mm.

Package Outline Description (SOT23-5)

1.45mm height 5-pin SOT-23 plastic SOIC



NOTE：

(5) All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

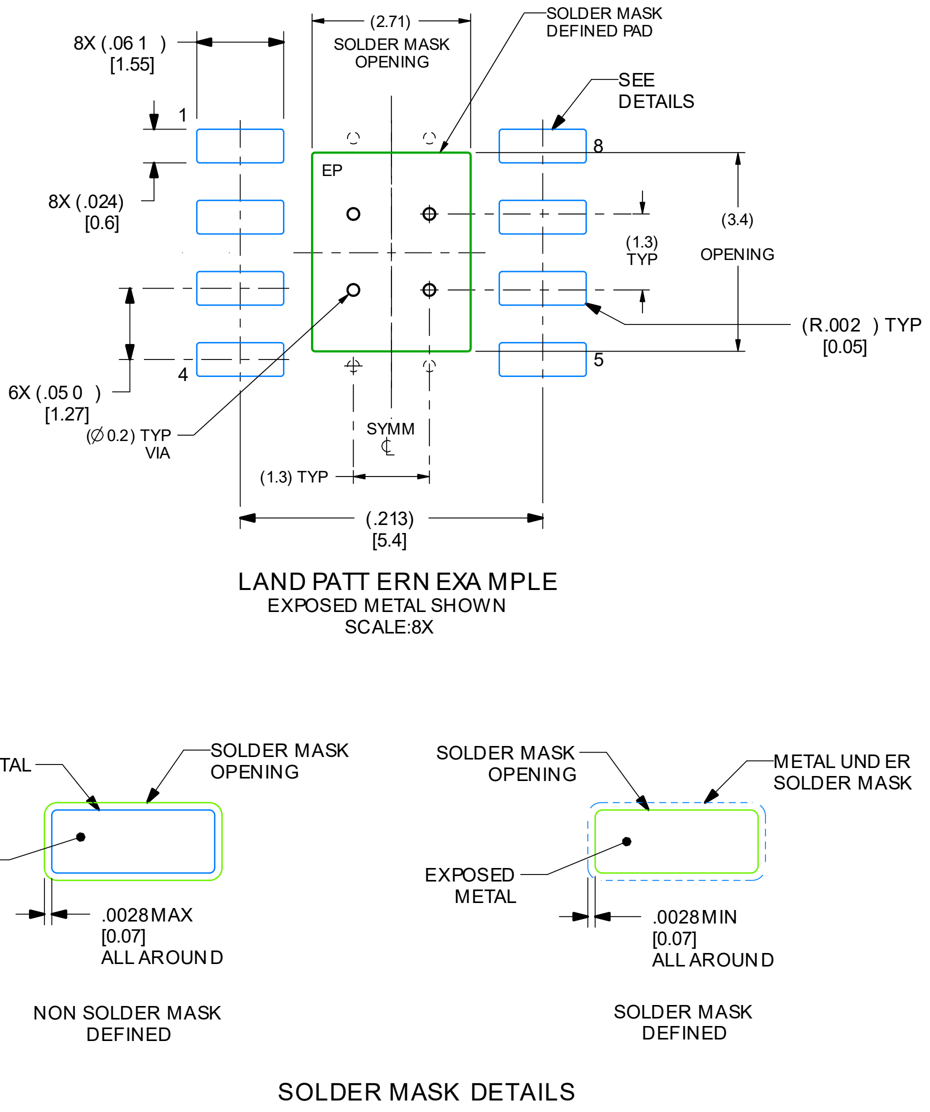
(6) This drawing is subject to change without notice.

(7) This dimension does not include mold burrs, protrusions, or nozzle burrs. The burrs or protrusions on each side of the mold shall not exceed 0.15mm.

(8) This dimension does not include mold burrs, and the burrs or protrusions on each side of the mold do not exceed 0.25 mm.

Component package pad layout (ESOP8)

8-pin plastic seal SOIC with bottom EPAD



NOTE:

(1) Based on IPC-7351, which relies on proven mathematical algorithms, and comprehensively considers manufacturing, assembly, and component tolerances, the pad pattern is accurately calculated.

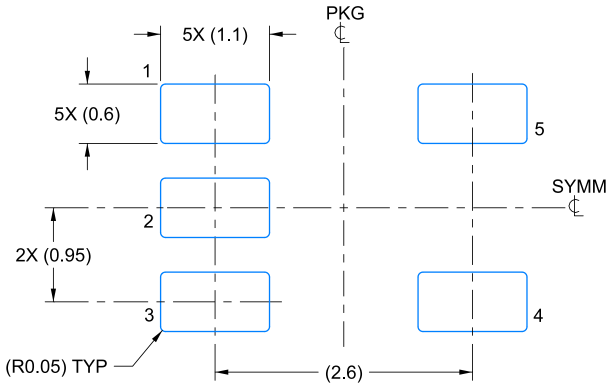
(2) Solder mask tolerances between and around signal pads may vary due to board fabrication.

(3) The size of the metal pad may vary due to creepage requirements.

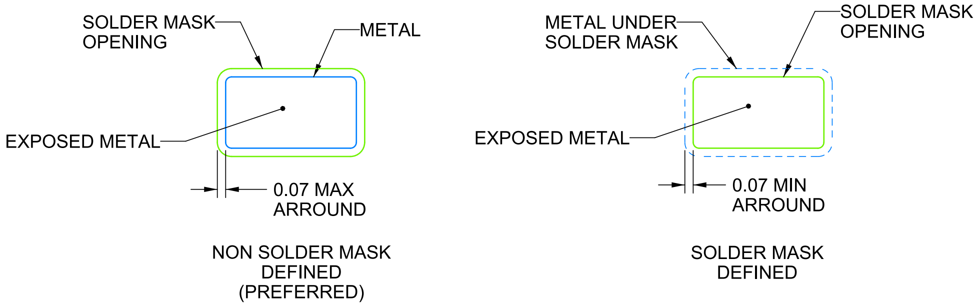
(4) Through holes are optional, depending on application, see device data sheet. If vias are used, refer to the via locations shown in this view. It is recommended to fill or cover the vias under the pads with solder paste.

Component package pad layout (SOT23-5)

1.45mm height 5-pin SOT-23 plastic SOIC



器件封装焊盘布局举例
SCALE:15X



焊盘阻焊部详解
PADS 1-6

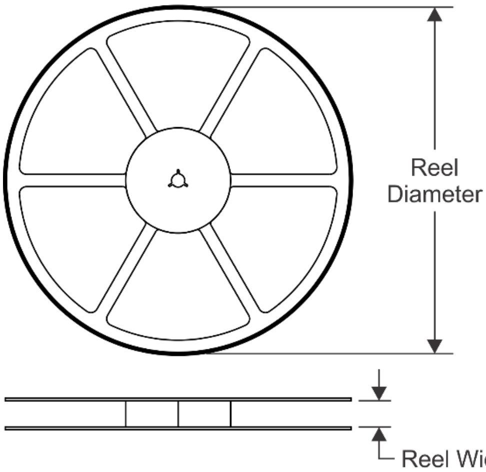
NOTE：

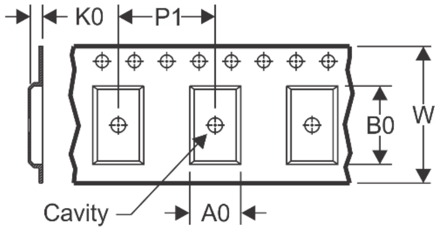
(1) Based on IPC-7351, which relies on proven mathematical algorithms, and comprehensively considers manufacturing, assembly, and component tolerances, the pad pattern is accurately calculated.

(2) Solder mask tolerances between and around signal pads may vary due to board fabrication.

(3) The size of the metal pad may vary due to creepage requirements.

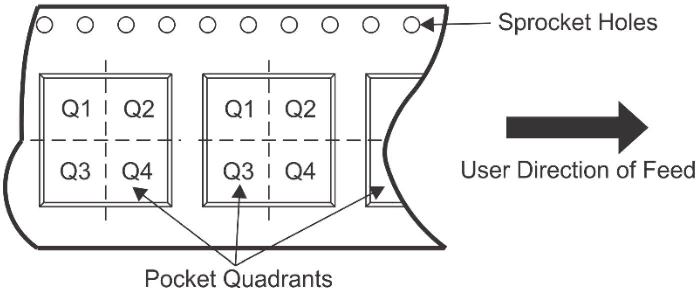
TAPE AND REEL INFORMALEGEND-SION





A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*ALL dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Width W1(mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LGS63040	SOT23-5	B5	5	3000	180.0	8.4	3.2	3.2	1.4	1.4	Q3
LGS63042	SOT23-5	B5	5	3000	180.0	8.4	3.2	3.2	1.4	1.4	Q3
LGS63040	ESOP8	EP	8	4000	330	6.5	5.3	2.1	TBD	12	TBD
LGS63042	ESOP8	EP	8	4000	330	6.5	5.3	2.1	TBD	12	TBD

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