20MHz -4GHz GaAs SPDT Switch

Chip Overview

Chip Introduction

AS179-92LF is a single pole double throw switch designed by pHEMT GaAs technology. The circuit structure of the chip is simple, and the recommended operating frequency of the chip is 20MHz-4GHz. The chip is controlled by a single power supply and has very low current consumption. When the switch is turned on, there is very low insertion loss.

The functional block diagram of the chip is shown in Figure 1.1, which includes two control ports and three RF ports. The voltage of the two control ports V1 and V2 is in opposite phase, and different switching paths correspond to different states.

Main features

- IP1dB=+30dBm@VC=3V
- IIP3=+43dBm@VC=3V
- Low insertion loss: 0.3dB@0.9GHz
- Ultralow DC power consumption
- Small packaging, low cost

Chip Applications

- Conventional medium power switch applications
- Industrial radio
- smart home
- Applications with a transmitting and receiving system that require switching

Chip Packaging

SOT363

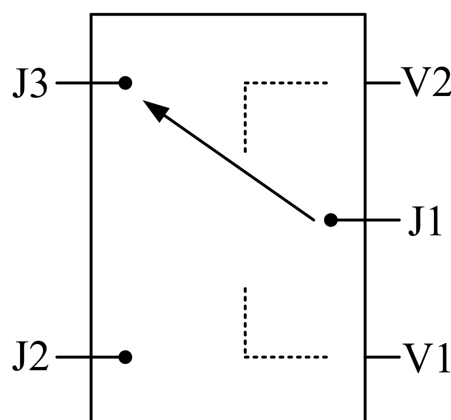


Figure 1.1 Block Diagram

Pin description

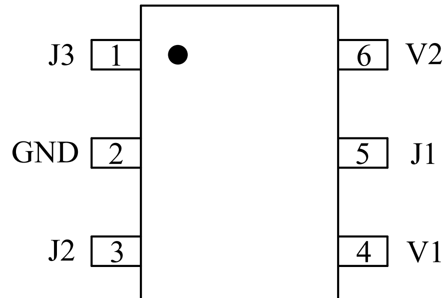


Figure 2.1 Pin diagram

Pin Description

pin number	Pin name	Pin description
1	J3	RF port, requires external DC blocking capacitor
2	GND	ground
3	J2	RF port, requires external DC blocking capacitor
4	V1	DC control voltage
5	J1	RF port, requires external DC blocking capacitor
6	V2	DC control voltage

Electrical characteristics

Absolute maximum ratings

parameter	unit	minimum	maximum	condition
DC control voltage	V	-1.2	+8	
RF port power >500MHz <500MHz	 W mW		 6 500	
Chip operating temperature	℃	-40	+85	

Chip storage temperature range	℃	-65	+150	

Note: Exceeding one or several absolute maximum ratings mentioned above may result in permanent damage to the device. It is recommended to use within the range listed in the table. The maximum signal strength at the RF input corresponds to an RF input impedance of 50 Ohm.

Typical performance characteristics

Control voltage Vctrl=0-3V, operating temperature is 25 ℃.

parameter	unit	minimum	typical	maximum	test conditions
Insertion loss (IL)	dB		0.3	0.4	0.02-1.0GHz
			0.3	0.5	1.0-2.0GHz
			0.4	0.6	2.0-3.0GHz
			0.5	0.7	3.0-4.0GHz
Isolation (ISO)	dB	22	25		0.02-1.0GHz
		22	25		1.0-2.0GHz
		20	23		2.0-3.0GHz
Input Return Loss	dB	15		20	0.02-1.0GHz
		15		20	1.0-2.0GHz
		14		17	2.0-3.0GHz
		13		15	3.0-4.0GHz
Switching time					
Rise/fall	ns		10		10% to 90% or 90% to 10%
On/off	ns		100		50% to 90% or 10%
Input 1dB compression point (IP1dB)	dBm				@0.5-3.0GHz
			+26		Vctrl=0-2V
			+30		Vctrl=0-3V
			+34		Vctrl=0-5V
					@48MHz
			+28.9		Vctrl=0-3V

			+29.5 +29 +32		Vctrl=0-5V @3.0-4.0GHz Vctrl=0-3V Vctrl=0-5V
Input third-order intercept point (IIP3)	dBm		+43 +43 +50 +45		The power of the dual tone input is 5dBm @0.5-3.0GHz Vctrl=0-2V Vctrl=0-3V Vctrl=0-5V @3.0-4.0GHz Vctrl=0-5V
thermal resistance	°C/W		25		
control voltage Low (20uA) High (100uA) High (200uA)	V	0		0.2 2.0 5.0	Vctrl_L Vctrl_H Vctrl_H

Truth table

V1	V2	J1-J2	J1-J3
1	0	Isolation	Insertion loss
0	1	Insertion loss	Isolation

Note:

1 "represents the high-level state of the control pin (2-5V)

'0' represents the low-level state of the control pin (0-0.2V)

Logic states not listed in the table will cause the switch to operate abnormally, but will not damage the device

Application circuit

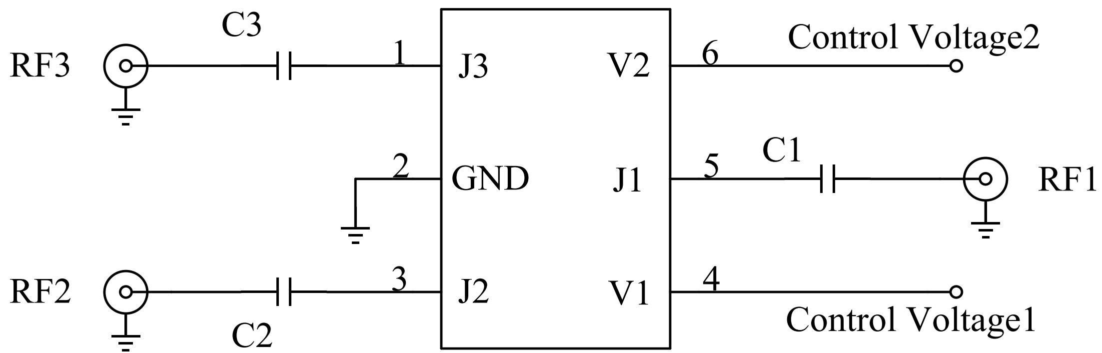


Figure 4.1 Application Circuit

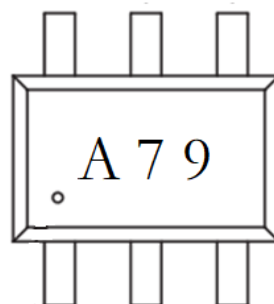
Note:

When the operating frequency is higher than 500MHz, 100pF can be used for capacitors of C1, C2, and C3, but as the operating frequency decreases, larger capacitors need to be used as DC blocking capacitors.

When the operating frequency is below 50MHz, 10nF are required for capacitors of C1, C2, and C3.

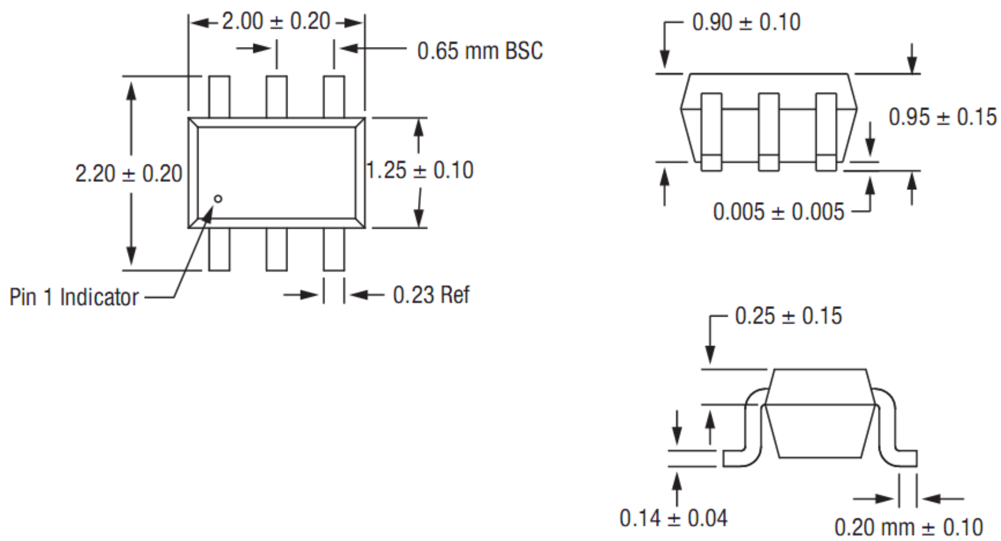
Package information

Package marking



Package dimensions

The chip is packaged in SOT363, and the following are the package dimensions.



Chip soldering and storage

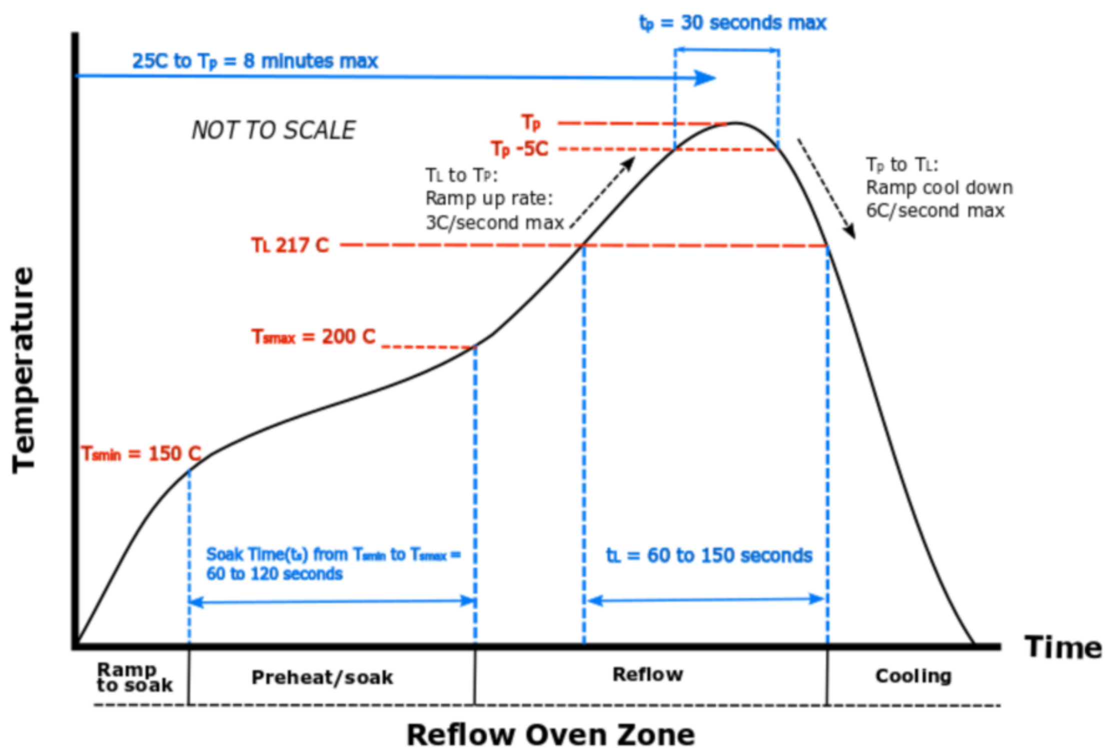
Moisture sensitivity level:

Moisture Sensitivity Level (MSL): Level 3

MSL, please refer to the IPC/JEDEC J-STD-020 standard.

Reflow soldering curve:

Refer to IPC/JEDEC J-STD-020 standard



Lead-free soldering process:

1. Preheat the temperature zone to 150℃-200℃ and maintain it for 60s-120s;

2. Reflow temperature > 217℃, duration 60s-150s;

Temperature rise slope: from the reflux temperature (217℃) to the peak temperature range, the temperature rise slope is ≤3℃/S;

Cooling rate: Within the range from peak temperature to reflow temperature of 217℃, the cooling rate is ≤6℃/S;

3. The peak set temperature should not exceed 260℃, and the actual temperature should also not exceed 260℃. The total time from the highest temperature to a decrease of 5℃ should not exceed 30 seconds

4. Time from normal temperature (25℃) to peak temperature: ≤8 minutes;

5. The number of reflow soldering cycles for the chip shall be no more than 3;

The reflow soldering time can be set based on various factors such as equipment model, equipment lifespan, number of temperature zones, heating method, PCB board thickness, solder paste model, heat resistance of electronic components, solder paste glossiness after soldering, and stencil condition. Proper adjustments to temperature and chain speed can be made within the conditions specified in Table 5-2 of J-STD-020. The temperature process parameters set for each product and its corresponding equipment should be unique.

- Furnace temperature testing frequency: Furnace temperature testing is required when switching products, and it should be conducted at least every 24 hours during continuous production;
- The reflow oven should undergo a temperature stability verification assessment at least once a year;
- The lifespan of the temperature measurement board is recommended to be 50-100 uses;
- The temperature measuring instrument needs to be calibrated regularly;
- When considering the slope of temperature rise and fall, it is important to ensure that the chain speed and statistical time interval are reasonable.

Key points of temperature measurement:

1. Perform operations at 3-7 locations on the substrate;
2. In areas with high/low component loading density;

3. At or near the location of components with large heat capacity;

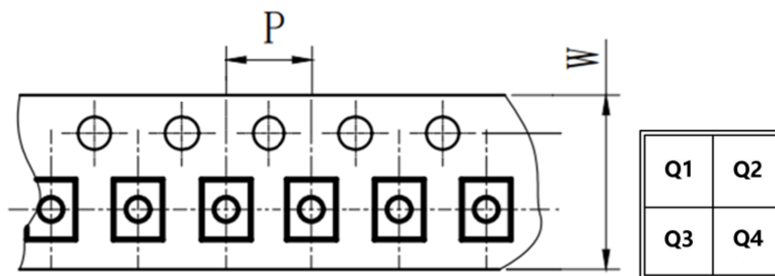
4. For component leads and physical surfaces with weaker heat resistance (IC/electrolytic capacitors);

5. To accurately measure the peak temperature of the package, refer to the thermocouples recommended in JEP140.

Packaging and transportation

Packaging

The chip is packaged with vacuum tape, which has moisture-proof, anti-static and other characteristics. The usage process is compatible with major surface mount machines in the industry. The minimum packaging is 3000 pieces per tray.



W=8.0mm, P=4.0mm, PIN1 orientation: Q3

ESD protection

Please take precautions against static electricity and moisture during the transportation and production of chips.

Please pay attention to electrostatic protection during use, packaging, and transportation!