1.General Description

The 74HC4094; 74HCT4094 is an 8-bit serial-in/serial or parallel-out shift register with a storage register and 3-state outputs. Both the shift and storage register have separate clocks. The device features a serial input (D) and two serial outputs (QS1 and QS2) to enable cascading. Data is shifted on the LOW-to-HIGH transitions of the CP input. Data is available at QS1 on the LOW-to-HIGH transitions of the CP input to allow cascading when clock edges are fast. The same data is available at QS2 on the next HIGH-to-LOW transition of the CP input to allow cascading when clock edges are slow. The data in the shift register is transferred to the storage register when the STR input is HIGH. Data in the storage register appears at the outputs whenever the output enable input (OE) is HIGH. A LOW on OE causes the outputs to assume a high-impedance OFF-state. Operation of the OE input does not affect the state of the registers. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.

2.Features and Benefits

- Complies with JEDEC standard JESD7A
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

3.Applications

- Serial-to-parallel data conversion
- Remote control holding register

4. Ordering Information

Table 1. Ordering information

Type number	Package		
	Name	Description	Quantity
74HC4094D	SOP-16L	plastic small outline package; 16 leads; body width 3.9 mm	2500
74HCT4094D			
74HC4094PW	TSSOP-16L	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	2500
74HCT4094PW			

5. Function Diagram

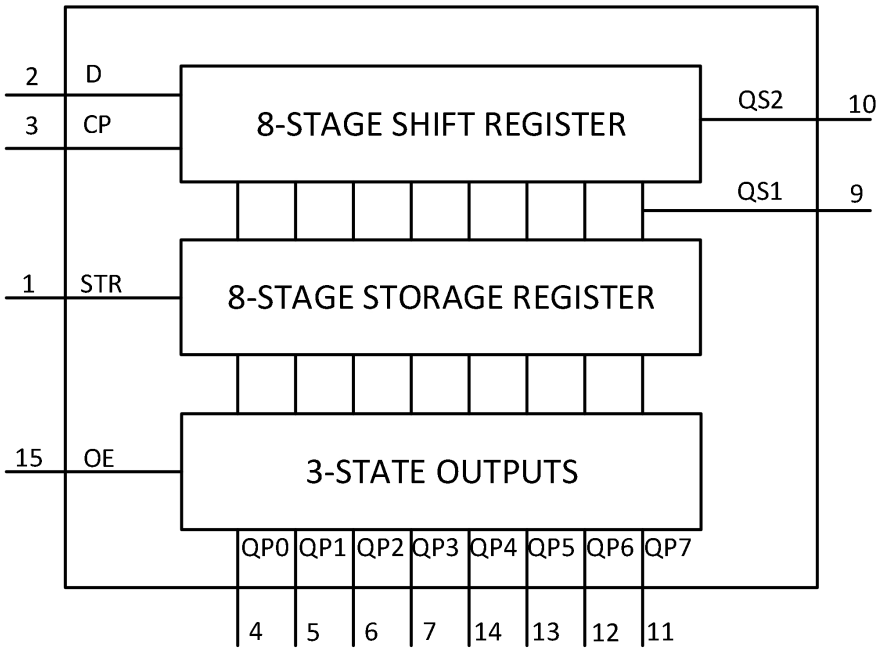


Fig. 1. Functional diagram

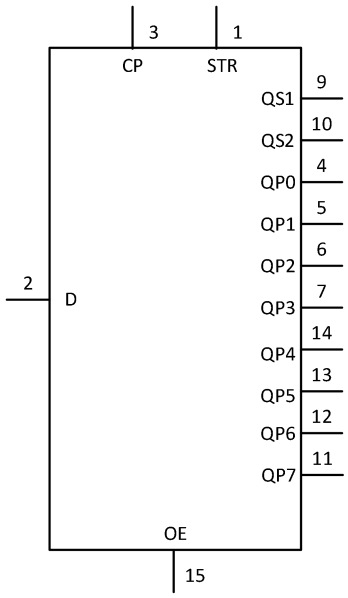


Fig. 2. Logic symbol

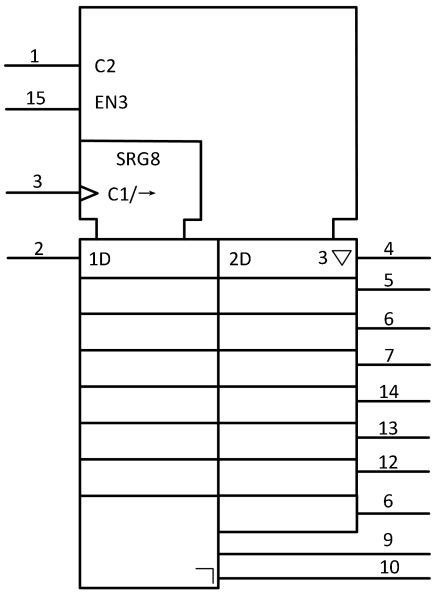


Fig. 3. IEC logic symbol

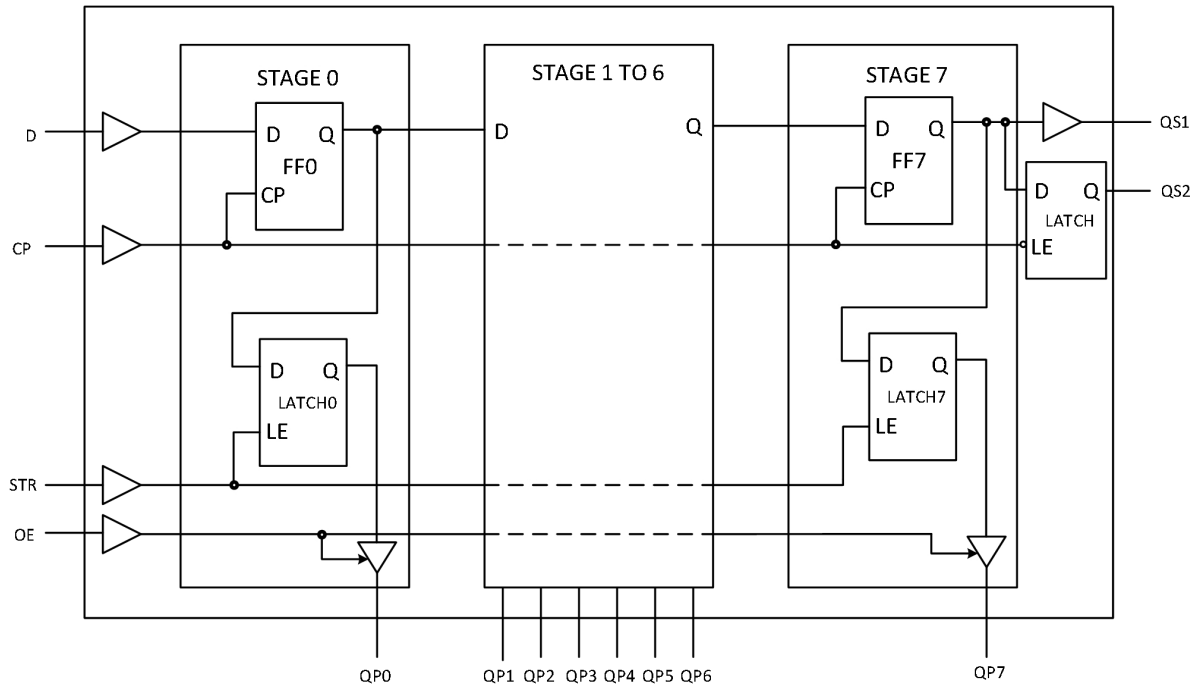


Fig. 4. Logic diagram

6. Pinning Information

6.1. Pinning

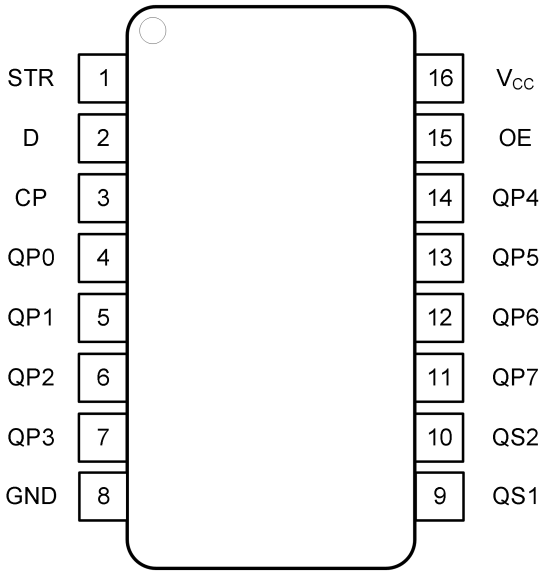


Fig. 5. Top view pin configuration SOP and TSSOP

6.2. Pin description

Table 2. Pin description

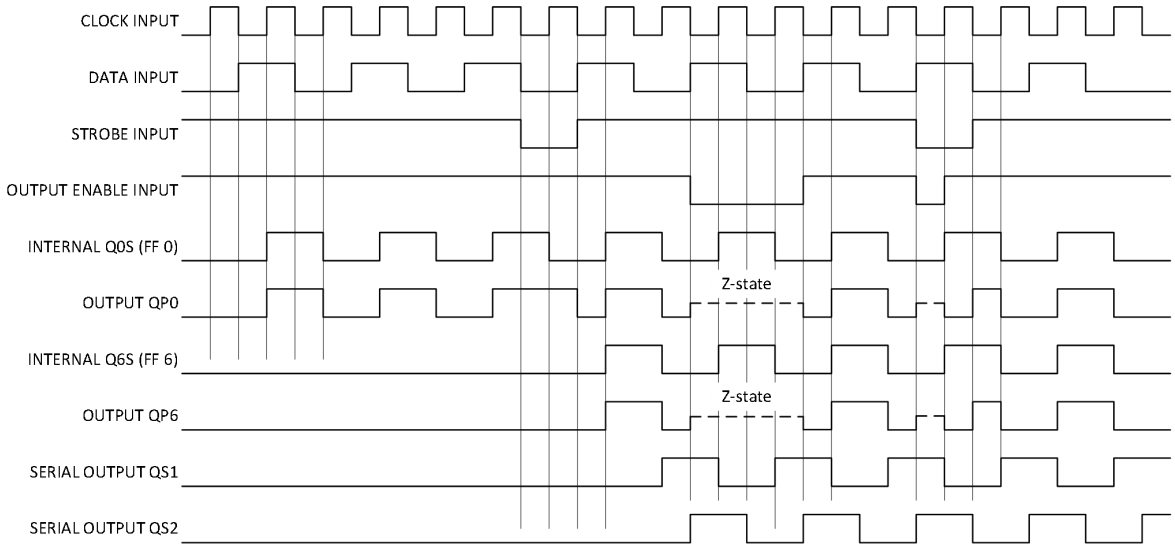
Symbol	Pin	Description
STR	1	Strobe input
D	2	Data input
CP	3	Clock input
QP0, QP1, QP2, QP3, QP4, QP5, QP6, QP7	4, 5, 6, 7, 14, 13, 12, 11	Parallel output
GND	8	Ground supply voltage
QS1, QS2	9, 10	Serial output
OE	15	Output enable input
V_{CC}	16	Supply voltage

7.Functional Description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = HIGH-impedance OFF-state;
NC = no change; ↑ = positive-going transition; ↓ = negative-going transition;
Q6S = the data in register stage 6 before the LOW to HIGH clock transition;
Q7S = the data in register stage 7 before the HIGH to LOW clock transition.

Inputs				Parallel outputs		Serial outputs	
CP	**OE**	**STR**	**D**	**QP0**	**QPn**	**QS1**	**QS2**
↑	L	X	X	Z	Z	Q6S	NC
↓	L	X	X	Z	Z	NC	Q7S
↑	H	L	X	NC	NC	Q6S	NC
↑	H	H	L	L	QPn-1	Q6S	NC
↑	H	H	H	H	QPn-1	Q6S	NC
↓	H	H	H	NC	NC	NC	Q7S



At the positive clock edge, the information in the 7th register stage is transferred to the 8th register stage and the QSn outputs.

Fig. 6. Timing diagram

8.Absolute Maximum Ratings

Stresses exceeding the absolut`e maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Table 4. Absolute Maximum Ratings

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	7	V
I_{IK}	input clamping current	$V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V		±20	mA
I_{OK}	output clamping current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V		±20	mA
I_O	output current	$V_O = -0.5$ V to $(V_{CC} + 0.5$ V)		±25	mA
I_{CC}	supply current			50	mA
I_{GND}	ground current		-50		mA
P_{tot}	total power dissipation	$T_{amb} = -40$ °C to + 125 °C		500	mW
T_{stg}	storage temperature		-65	150	°C

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

9.Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. EnergyMath does not recommend exceeding them or designing to Absolute Maximum Ratings.

Table 5. Recommended Operating Conditions

Symbol	Parameter	Conditions	74HC4094			74HCT4094			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	supply voltage		2.5	5.0	6.0	4.5	5.0	5.5	V
V_I	input voltage		0		V_{CC}	0		V_{CC}	V
V_O	output voltage		0		V_{CC}	0		V_{CC}	V
T_{amb}	ambient temperature		-40	25	125	-40	25	125	°C
Δt/ΔV	Input transition rise and fall rate	$V_{CC} = 2.5$ V			625				ns/V
		$V_{CC} = 4.5$ V		1.67	139		1.67	139	ns/V
		$V_{CC} = 6.0$ V			83				ns/V

10. Static Characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	
74HC4094								
V_{IH}	HIGH-level input voltage	V_{CC} = 2.5 V	1.5			1.5		V
		V_{CC} = 4.5 V	3.15			3.15		V
		V_{CC} = 6.0 V	4.2			4.2		V
V_{IL}	LOW-level input voltage	V_{CC} = 2.5 V			0.5		0.5	V
		V_{CC} = 4.5 V			1.35		1.35	V
		V_{CC} = 6.0 V			1.8		1.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}						
		I_O = -20 µA; V_{CC} = 2.5 V	2.4			2.4		V
		I_O = -20 µA; V_{CC} = 4.5 V	4.4			4.4		V
		I_O = -20 µA; V_{CC} = 6.0 V	5.9			5.9		V
		I_O = -4.0 mA; V_{CC} = 4.5 V	3.84			3.7		V
		I_O = -5.2 mA; V_{CC} = 6.0 V	5.34			5.2		V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}						
		I_O = -20 µA; V_{CC} = 2.5 V			0.1		0.1	V
		I_O = -20 µA; V_{CC} = 4.5 V			0.1		0.1	V
		I_O = -20 µA; V_{CC} = 6.0 V			0.1		0.1	V
		I_O = -4.0 mA; V_{CC} = 4.5 V			0.33		0.4	V
		I_O = -5.2 mA; V_{CC} = 6.0 V			0.33		0.4	V
I_I	input leakage current	V_I = V_{CC} or GND ; V_{CC} = 6.0 V			±1		±1	µA
I_{OZ}	OFF-state output current	V_I = V_{IH} or V_{IL} ; V_{CC} =6.0 V ; V_O = V_{CC} or GND			±5		±10	µA
I_{CC}	supply current	V_I = V_{CC} or GND ; I_O = 0 A ; V_{CC} = 6.0 V			20		40	µA
C_I	input capacitance			4				pF

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	
74HCT4094								
V_{IH}	HIGH-level input voltage	V_{CC} = 4.5 V to 5.5 V	2.0			2.0		V
V_{IL}	LOW-level input voltage	V_{CC} = 4.5 V to 5.5 V			0.8		0.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}; V_{CC} = 4.5 V						
		I_O = -20 µA	4.4			4.4		V
		I_O = -4.0 mA	3.84			3.7		V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}; V_{CC} = 4.5 V						
		I_O = 20 µA			0.1		0.1	V
		I_O = 4.0 mA			0.33		0.4	V
I_I	input leakage current	$V_I = V_{CC}$ or GND ; V_{CC} = 5.5 V			±1		±1	µA
I_{OZ}	OFF-state output current	$V_I = V_{IH}$ or V_{IL} ; V_{CC} =5.5 V ; $V_O = V_{CC}$ or GND			±5		±10	µA
I_{CC}	supply current	$V_I = V_{CC}$ or GND ; I_O = 0 A ; V_{CC} = 5.5 V			20		40	µA
ΔI_{CC}	additional supply current	$V_I = V_{CC}$ - 2.1 V; other inputs at V_{CC} or GND; V_{CC} = 4.5 V to 5.5 V; I_O = 0 A						
		per input pin; STR input			450		490	µA
		per input pin; OE input			675		735	µA
		per input pin; CP input			675		735	µA
		per input pin; D input			180		196	µA
C_I	input capacitance			4				pF

11. Dynamic Characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 11.

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	
74HC4094								
t_{pd}	propagation delay	CP to QS1; see Fig. 7 [1]						
		V_{CC} = 2.5 V			190		225	ns
		V_{CC} = 4.5 V			38		45	ns
		V_{CC} = 6.0 V			33		38	ns
		CP to QS2; see Fig. 7 [1]						
		V_{CC} = 2.5 V			170		205	ns
		V_{CC} = 4.5 V			34		41	ns
		V_{CC} = 6.0 V			29		35	ns
		CP to QPn; see Fig. 7 [1]						
		V_{CC} = 2.5 V			245		295	ns
		V_{CC} = 4.5 V			49		59	ns
		V_{CC} = 6.0 V			42		50	ns
		STR to QPn; see Fig. 8 [1]						
		V_{CC} = 2.5 V			225		270	ns
		V_{CC} = 4.5 V			45		54	ns
		V_{CC} = 6.0 V			38		46	ns
t_{en}	enable time	OE to QPn; see Fig. 9 [1]						
		V_{CC} = 2.5 V			220		265	ns
		V_{CC} = 4.5 V			44		53	ns
		V_{CC} = 6.0 V			37		45	ns
t_{dis}	disable time	OE to QPn; see Fig. 9 [1]						
		V_{CC} = 2.5 V			155		190	ns
		V_{CC} = 4.5 V			31		38	ns
		V_{CC} = 6.0 V			26		32	ns

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	
t_t	transition time	QPn and QSn; see Fig. 7 [1]						
		V_{CC} = 2.5 V			95		110	ns
		V_{CC} = 4.5 V			19		22	ns
		V_{CC} = 6.0 V			16		19	ns
t_W	pulse width	CP HIGH or LOW; see Fig. 7						
		V_{CC} = 2.5 V			100		120	ns
		V_{CC} = 4.5 V			20		24	ns
		V_{CC} = 6.0 V			17		20	ns
		STR HIGH; see Fig. 8						
		V_{CC} = 2.5 V			100		120	ns
		V_{CC} = 4.5 V			20		24	ns
		V_{CC} = 6.0 V			17		20	ns
t_{SU}	set-up time	D to CP; see Fig. 10						
		V_{CC} = 2.5 V			65		75	ns
		V_{CC} = 4.5 V			13		15	ns
		V_{CC} = 6.0 V			11		13	ns
		CP to STR; see Fig. 8						
		V_{CC} = 2.5 V			125		150	ns
		V_{CC} = 4.5 V			25		30	ns
		V_{CC} = 6.0 V			21		26	ns
t_h	hold time	D to CP; see Fig. 10						
		V_{CC} = 2.5 V			3		3	ns
		V_{CC} = 4.5 V			3		3	ns
		V_{CC} = 6.0 V			3		3	ns
		CP to STR; see Fig. 8						
		V_{CC} = 2.5 V			0		0	ns
		V_{CC} = 4.5 V			0		0	ns
		V_{CC} = 6.0 V			0		0	ns

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	
f_{max}	maximum frequency	CP; see Fig. 7						
		V_{CC} = 2.5 V			4.8		4.0	MHz
		V_{CC} = 4.5 V			24		20	MHz
		V_{CC} = 6.0 V			28		24	MHz
C_{PD}	power dissipation capacitance	C_L = 50 pF; f = 1 MHz; V_I = GND to V_{CC} [2]		83				pF
74HCT4094								
t_{pd}	propagation delay	CP to QS1; see Fig. 7 [1]						
		V_{CC} = 4.5 V			49		59	ns
		CP to QS2; see Fig. 7 [1]						
		V_{CC} = 4.5 V			45		54	ns
		CP to QPn; see Fig. 7 [1]						
		V_{CC} = 4.5 V			54		65	ns
		STR to QPn; see Fig. 8 [1]						
		V_{CC} = 4.5 V			49		65	ns
t_{en}	enable time	OE to QPn; see Fig. 9 [1]						
		V_{CC} = 4.5 V			44		53	ns
t_{dis}	disable time	OE to QPn; see Fig. 9 [1]						
		V_{CC} = 4.5 V			44		53	ns
t_t	transition time	QPn and QSn; see Fig. 7 [1]						
		V_{CC} = 4.5 V			19		22	ns
t_W	pulse width	CP HIGH or LOW; see Fig. 7						
		V_{CC} = 4.5 V			20		24	ns
		STR HIGH; see Fig. 8						
		V_{CC} = 4.5 V			20		24	ns
t_{su}	set-up time	Dn to CP; see Fig. 10						
		V_{CC} = 4.5 V			13		15	ns
		CP to STR; see Fig. 8						
		V_{CC} = 4.5 V			25		30	ns

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	
t_h	hold time	Dn to CP; see Fig. 10						
		V_{CC} = 4.5 V			4		4	ns
		CP to STR; see Fig. 8						
		V_{CC} = 4.5 V			0		0	ns
f_{max}	maximum frequency	CP; see Fig. 7						
		V_{CC} = 4.5 V			24		20	MHz
C_{PD}	power dissipation capacitance	C_L = 50 pF; f = 1 MHz; V_I = GND to V_{CC} - 1.5 V [2]		92				pF

[1] t_{pd} is the same as t_{PLH} and t_{PHL}; ten is the same as t_{PZH} and t_{PZL}; t_{dis} is the same as t_{PLZ} and t_{PHZ}; t_t is the same as t_{THL} and t_{TLH}.

[2] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

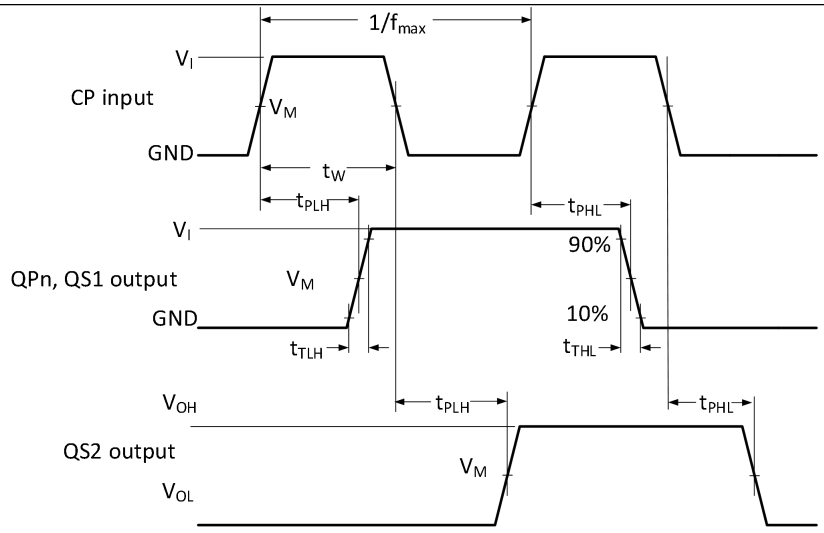
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

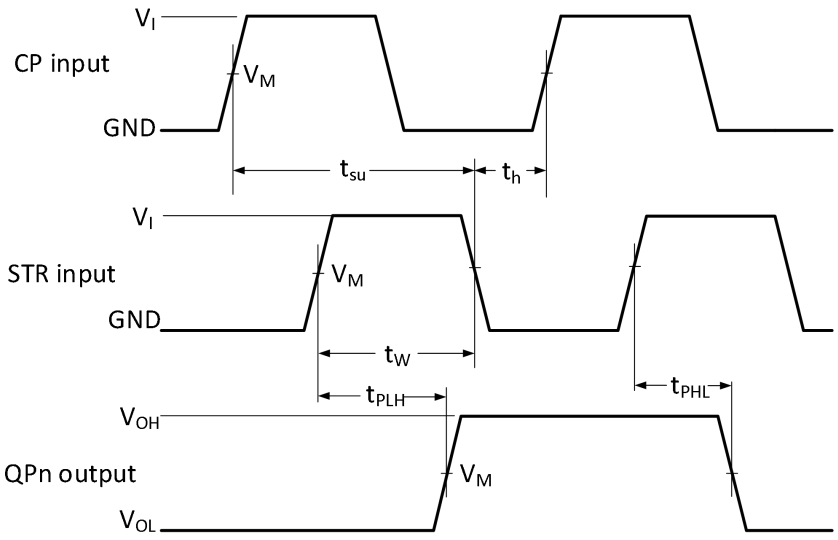
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

11.1. Waveforms and test circuit



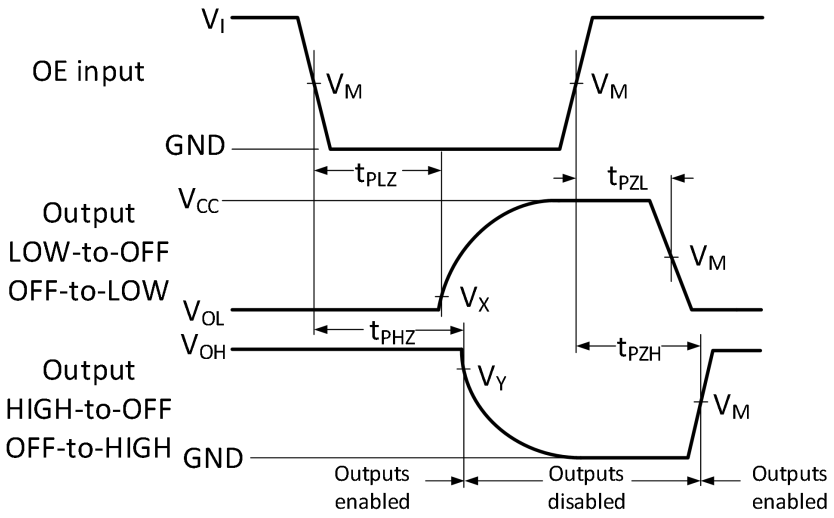
Measurement points are given in Table 8.
V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 7. Propagation delay input (CP) to output (QPn, QS1, QS2), output transition time, clock input (CP) pulse width and the maximum frequency (CP)



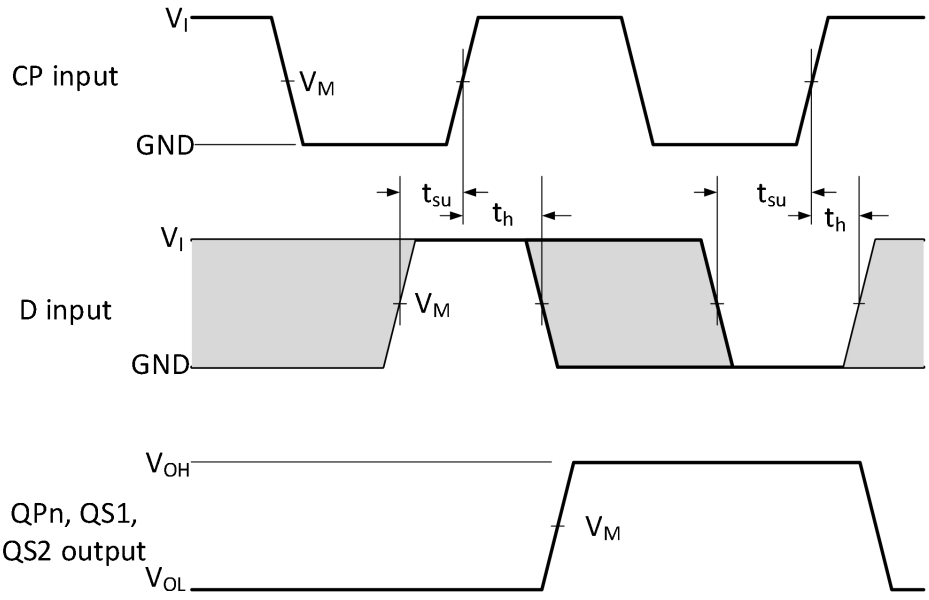
Measurement points are given in Table 8.
V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 8. Propagation delay strobe input (STR) to output (QPn), strobe input (STR) pulse width and the clock set-up and hold times for strobe input



Measurement points are given in Table 8.
V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 9. Enable and disable times

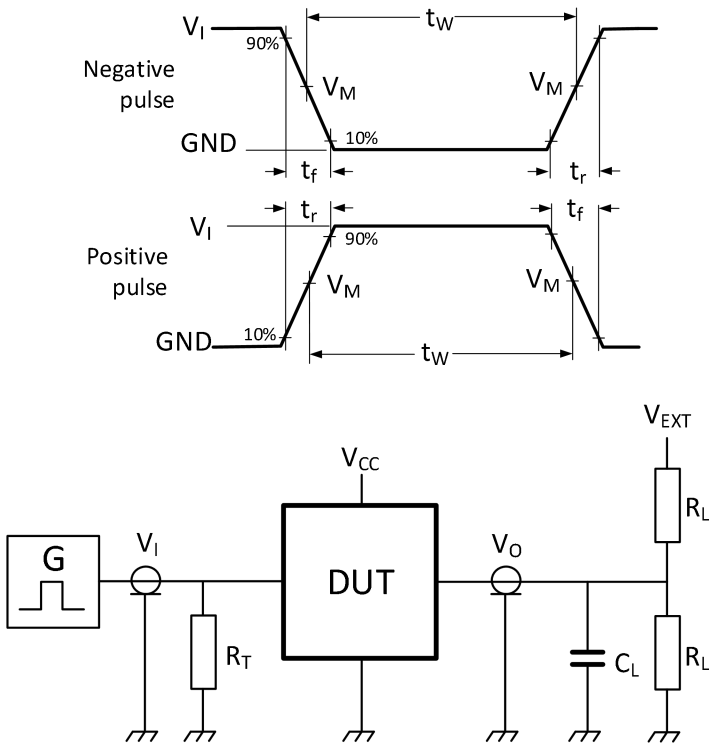


Measurement points are given in Table 8.
V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 10. The data input (D) to clock input (CP) set-up times and clock input (CP) to data input (D) hold times

Table 8. Measurement points

Type	Input	Output		
	V_M	V_M	V_X	V_Y
74HC4094	$0.5V_{CC}$	$0.5V_{CC}$	$0.1V_{OH}$	$0.9V_{OH}$
74HCT4094	1.3 V	1.3 V	$0.1V_{OH}$	$0.9V_{OH}$



Test data is given in Table 9.
Definitions for test circuit:
R_L = Load resistance.
C_L = Load capacitance including jig and probe capacitance.
R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.
V_{EXT} = External voltage for measuring switching times.

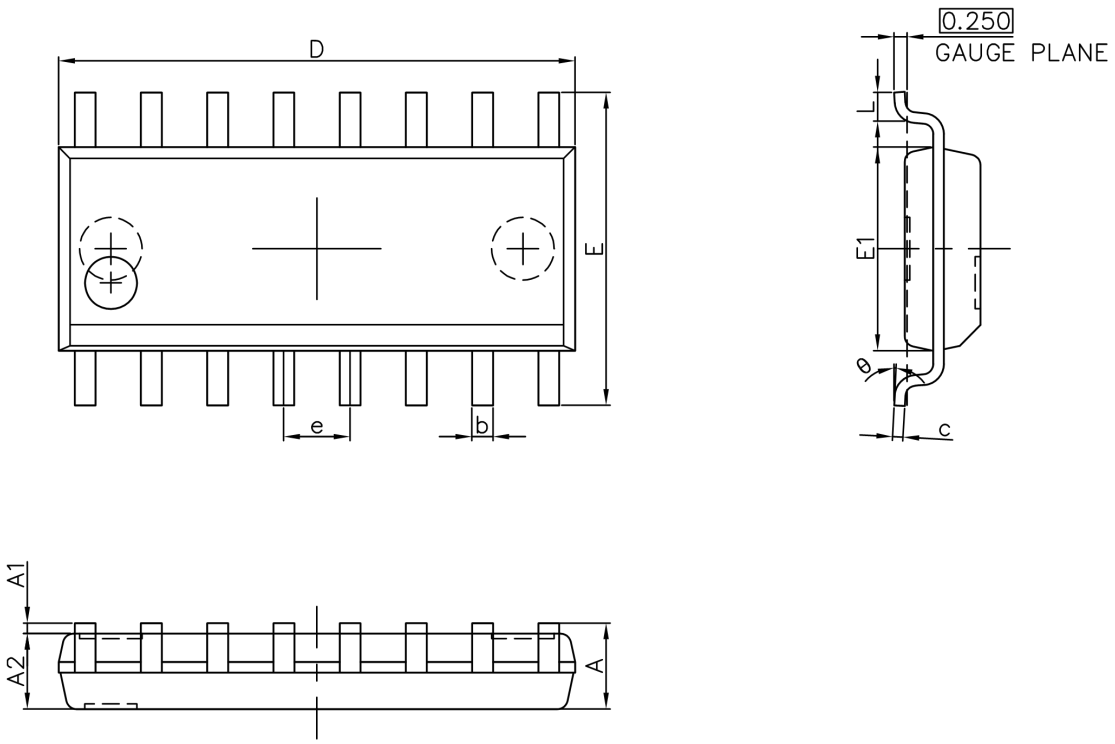
Fig. 11. Test circuit for measuring switching times

Table 9. Test data

Type	Input		Load		V_{EXT}		
	V_I	$t_r = t_f$	C_L	R_L	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
74HC4094	V_{CC}	2.0 ns	50 pF	500 Ω	open	GND	2 x V_{CC}
74HCT4094	3 V	2.0 ns	50 pF	500 Ω	open	GND	2 x V_{CC}

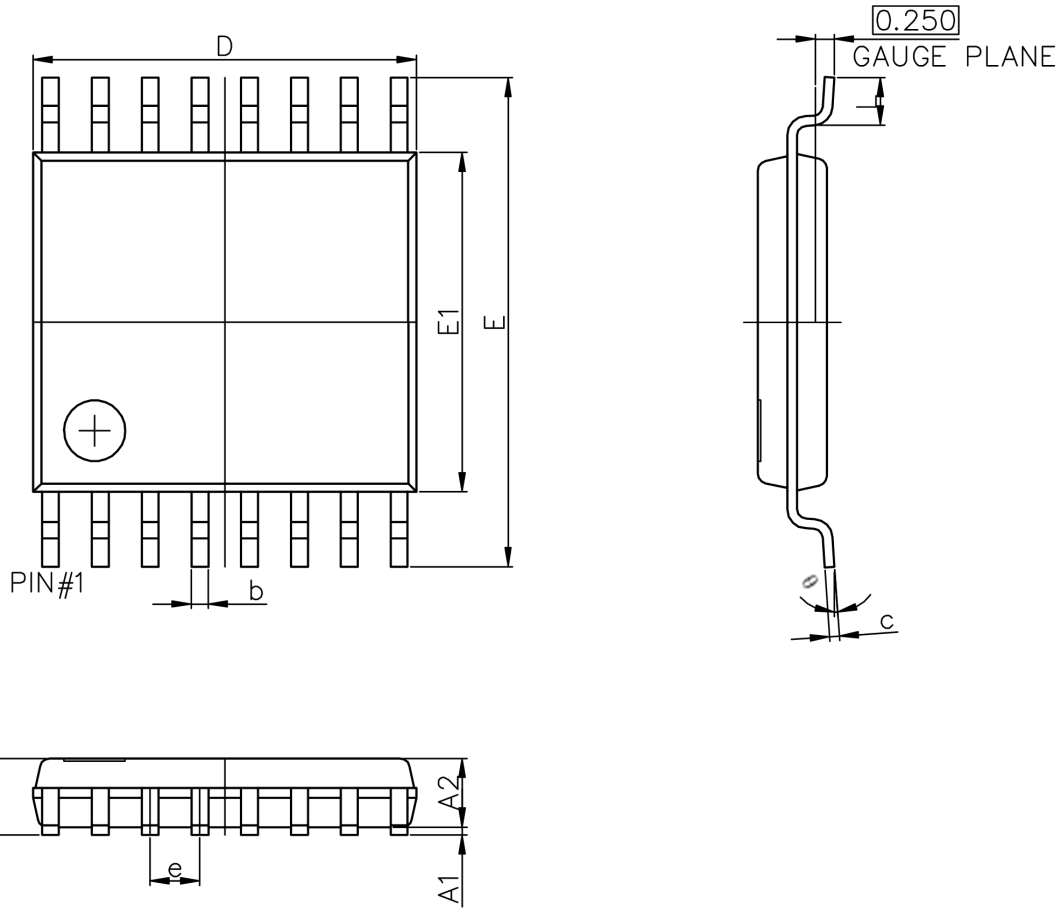
12. Package Outline

SOP-16L



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	——	1.750	——	0.069
A1	0.150	0.250	0.006	0.010
A2	1.400	1.500	0.055	0.059
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	9.800	10.000	0.386	0.394
e	1.270(BSC)		0.050(BSC)	
E	5.900	6.100	0.232	0.240
E1	3.800	4.000	0.150	0.157
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

TSSOP-16L



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	——	1.200	——	0.047
A1	0.020	0.100	0.001	0.004
A2	0.800	1.000	0.031	0.039
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
D	4.900	5.100	0.193	0.201
e	0.650(BSC)		0.026(BSC)	
E	6.250	6.550	0.252(BSC)	
E1	4.300	4.500	0.169	0.177
L	0.500	0.700	0.020	0.028
θ	1°	7°	1°	7°

13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
CDM	Charged Device Model
TTL	Transistor-Transistor Logic

14. Revision History

Table 11. Revision history

Document ID	Release Date	Data sheet status	Change notice	Supersedes
74HC_HCT4094 Rev. 1.0	Aug 08, 2024	Draft datasheet		