Description

MX74502D23 is a controller which operates in conjunction with an external back-to-back connected N channel MOSFETs to realize a low loss reverse polarity protection and load disconnect solution. The device can also be configured to drive high side MOSFET as high side switch with overvoltage protection. The wide supply input range 4V to 85V allows control of many popular DC bus voltages such 12V, 24V,48V and 60V input systems. The device can withstand and protect the loads from negative supply voltages down to -90V. The MX74502D23 does not have reverse current blocking actively.

The MX74502D23 controller provides a charge pump gate driver for an external N-channel MOSFET. With the enable pin low, the controller is off and draws approximately 1uA of current, thus offering low system current when input into sleep mode. MX74502D23 offers programmable overvoltage and undervoltage protection which cuts off the load from the input source in case of these fault events. The device offers an 8-pin DFN2*3 package.

Features

- 4V to 85V input range
- -90V input reverse voltage rating
- Integrated charge pump to drive
  External back-to-back N-channel MOSFETs
  External high side switch MOSFET
  External reverse polarity protection MOSFET
- 2.3A peak gate sink current capacity
- 12mA peak gate drive source capacity
- Enable control
- 100μA typical operating quiescent current（EN=High）
- 1μA shutdown current @12V input（EN=Low）
- Adjustable overvoltage and undervoltage protection
- Available in 8 pin DFN2*3 package

Application

- Power supply reverse polarity protection
- Industrial motor drives
- High side switch
- Battery high side MOSFET driver

Normal Information

Order Information

Part Number	Description
MX74502D23	DFN2*3-8L
MPQ	3000pcs

Package Dissipation Rating

package	RθJA(℃/W)
DFN2*3-8L	65

Absolute Maximum Ratings

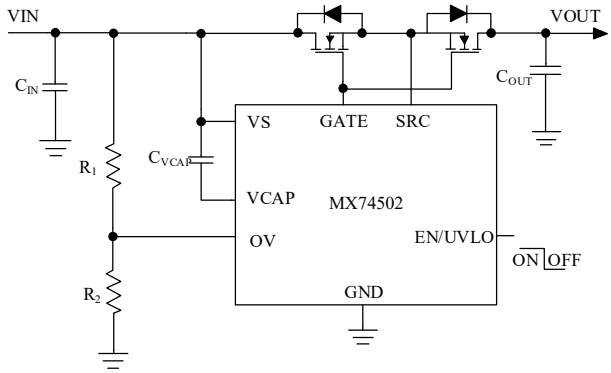
Parameters	Range
VS to GND	-100 to 100V
EN/UVLO,OV to GND,V_{VS}＞0V	-0.3 to 100V
EN/UVLO, OV, V_{VS}≤0V	V_{VS} to 100+V_{VS}
SRC to GND, V_{VS}≤0V	V_{VS}+0.3V(MAX)
SRC to GND,V_{VS}＞0V	-(100-V_{VS}) to V_{VS}
GATE to SRC	0 to 15V
VCAP to VS	0 to 15V
Junction, T_J	-40 to 150℃
T_{stg}	-40 to 150℃

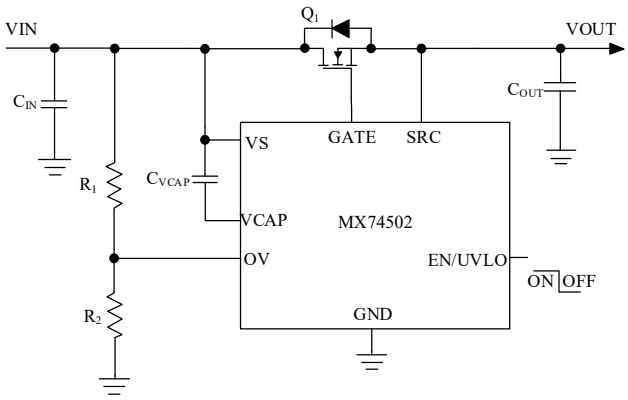
Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

Recommended Operating Conditions

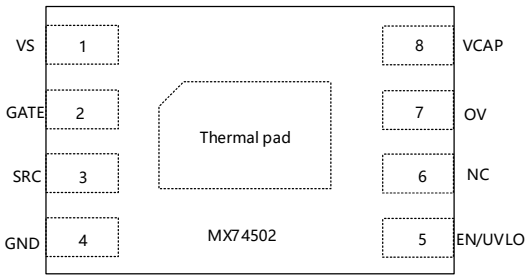
Parameters	Range
VS to GND	-90 to 85V
EN/UVLO, OV, SRC to GND	-90 to 85V
$C_{VCAP-VS}$	100nF~4.7uF
GATE to SRC	15V
Junction Temperature, T_J	-40 to 150℃

Typical Application





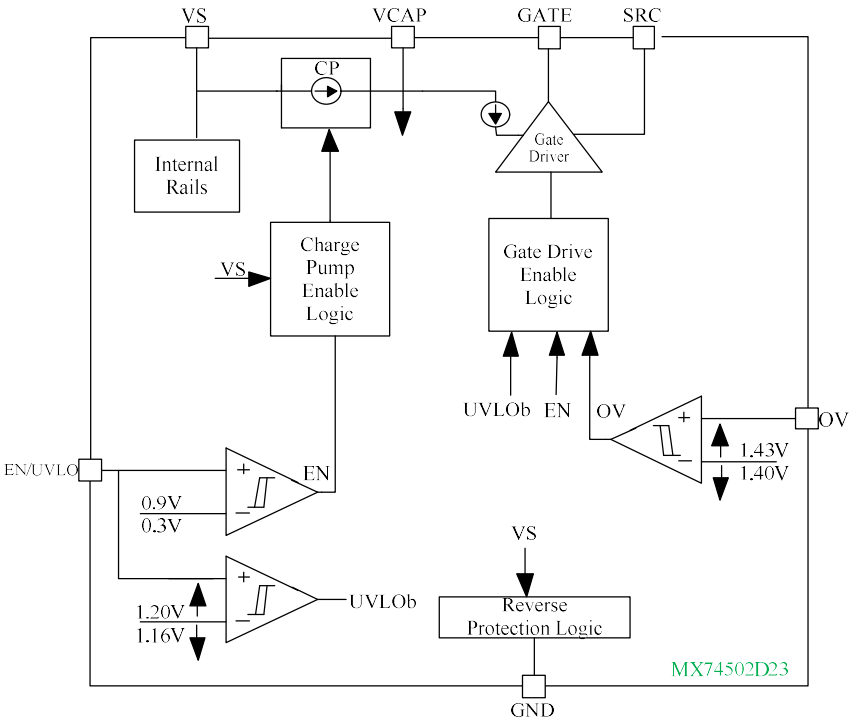
Terminal assignments



MX74502D23

Pin		Description
Name	No.	
VS	1	Input power supply pin to the controller. Connect a 100-nF capacitor across VS and GND pins.
GATE	2	Gate drive output. Connect to gate of the external N-channel MOSFET
SRC	3	Source pin. Connect to common source point of external back-to-back connected N-channel MOSFETs or the source pin of the high side switch MOSFET.
GND	4	Ground pin
EN	5	EN/UVLO Input. Connect to VS pin for always ON operation. Can be driven externally from a micro controller I/O. Pulling the pin low below $V_{(ENF)}$ makes the device enter into low IQ shutdown mode. For UVLO, connect an external resistor ladder from input supply to EN/UVLO to ground.
NC	6	No connection
OV	7	Adjustable overvoltage threshold input. Connect a resistor ladder from input supply to OV pin to ground. When the voltage at OV pin exceeds the overvoltage cutoff threshold then the GATE is pulled low. GATE turns ON when the OV pin voltage goes below the OVP falling threshold. Connect OV pin to ground when OV feature is not used.
VCAP	8	Charge pump output. Connect to external charge pump capacitor.
Thermal pad		No connection.

Block diagram



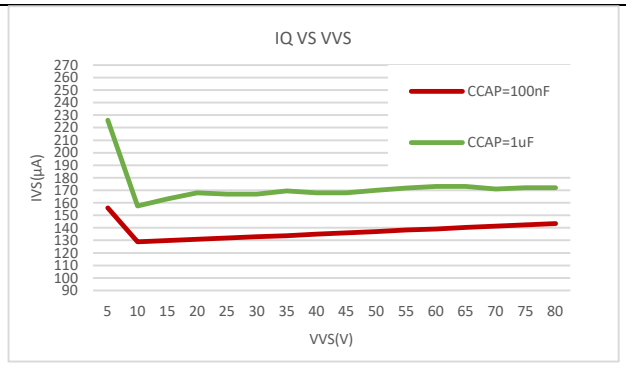
Electrical characteristics

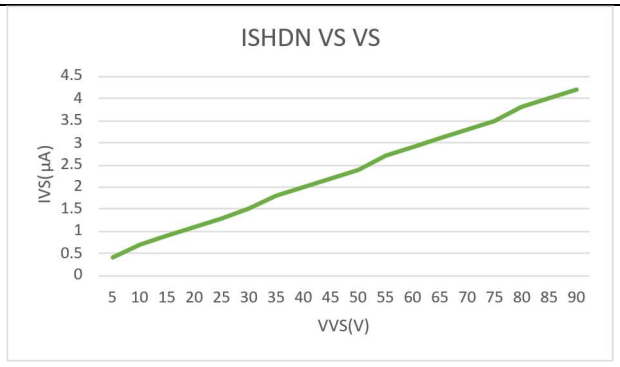
TJ = –40°C to +150°C; typical values at TJ = 25°C, V(VS) = 12 V, C(VCAP) = 1 µF, V(EN/UVLO) = 3 V, over operating free-air temperature range (unless otherwise noted)

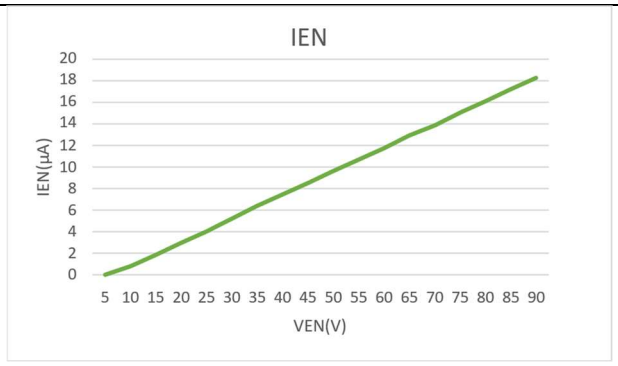
Symbol	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_S SUPPLY VOLTAGE						
$V_{(VS)}$	Operating input voltage		4		85	V
$V_{(VS\_POR)}$	VS POR Rising threshold		3.10	3.40	4.10	V
	VS POR Falling threshold		3.05	3.35	3.75	V
$V_{(VS\ POR(Hys))}$	VS POR Hysteresis			50		mV
$I_{(SHDN)}$	Shutdown Supply Current	$V_{(EN/UVLO)}$ = 0V	0.3	0.7	1.2	µA
$I_{(Q)}$	Operating Quiescent Current	$I_{GND,}$	100	150	210	µA
$I_{(REV)}$	VS pin leakage current during input reverse polarity	0 V ≤ $V_{(VS)}$ ≤ -65V		25		µA
ENABLE INPUT						
$V_{(EN\_UVLOF)}$	Enable/UVLO falling threshold		1.08	1.16	1.25	V
$V_{(EN\_UVLOR)}$	Enable/UVLO rising threshold		1.10	1.20	1.40	V
$V_{(ENF)}$	Enable threshold voltage for low IQ shutdown		0.30	0.70	0.90	V
$V_{(EN\_Hys)}$	Enable Hysteresis			40		mV
$I_{(EN/UVLO)}$	Enable sink current	$V_{(EN/UVLO)}$ = 12V		1		µA
GATE DRIVE						
$I_{(GATE)}$	Peak source current	$V_{(GATE)}$ – $V_{(SRC)}$ = 5V	5	12	20	mA
	Peak sink current	EN= High to Low $V_{(GATE)}$ – $V_{(SRC)}$ = 5 V		2.3		A
R_{DSON}	discharge switch R_{DSON}	EN = High to Low $V_{(GATE)}$ – $V_{(SRC)}$ = 100 mV		1.6	5	Ω
CHARGE PUMP						
$I_{(VCAP)}$	Charge Pump source current (Charge pump on)	$V_{(VCAP)}$ – $V_{(VS)}$ = 7V	50	110	300	µA
	Charge Pump sink current (Charge pump off)	$V_{(VCAP)}$ – $V_{(VS)}$ = 14V		4.0	5.5	µA
$V_{(VCAP)}$ –$V_{(VS)}$	Charge pump voltage at $V_{(VS)}$ = 3.4V	$I_{(VCAP)}$ ≤ 30µA	8			V
$V_{(VCAP)}$ –$V_{(VS)}$	Charge pump turn on voltage		10.3	11.6	13.0	V
$V_{(VCAP)}$ –$V_{(VS)}$	Charge pump turn off voltage		11.2	12.9	14.2	V
$V_{(VCAP)}$ –$V_{(VS)}$	Charge Pump Enable comparator Hysteresis			1.3		V
$V_{(VCAP\ UVLO)}$	$V_{(VCAP)}$ – $V_{(S)}$ UV release at rising edge		5.3	6.2	7.1	V
$V_{(VCAP\ UVLO)}$	$V_{(VCAP)}$ – $V_{(S)}$ UV threshold at falling edge		4.7	5.1	5.6	V
OVERVOLTAGE PROTECTION						
$V_{(OVR)}$	Overvoltage threshold input, rising		1.33	1.43	1.53	V
$V_{(OVF)}$	Overvoltage threshold input, falling		1.30	1.40	1.50	V
$V_{(OV\_Hys)}$	OV Hysteresis			30		mV
$I_{(OV)}$	OV Input leakage current	0V < $V_{(OV)}$ < 5V		50	100	nA
SWITCHING CHARACTERISTICS						
EN_{TDLY}	EN high to Gate Turn On delay	$V_{(VCAP)}$ > $V_{(VCAP\ UVLOR)}$, $V_{(EN/UVLO)}$ >$V_{(EN\_UVLOR)}$ to $V_{(GATE-SRC)}$ > 5V, $C_{(GATE-SRC)}$= 1.5nF	25	55	110	µs
$t_{UVLO\_OFF(deg)\_GATE}$	GATE Turnoff delay during EN/UVLO	$V_{(EN/UVLO)}$ ↓ to $V_{(GATE-SRC)}$ < 1V,$C_{(GATE-SRC)}$ = 1.5nF	1	2	3.5	µs
$t_{OVP\_OFF(deg)\_GATE}$	GATE Turnoff delay during OV	$V_{(OV)}$ ↑ to $V_{(GATE-SRC)}$ < 1V, $C_{(GATE-SRC)}$= 1.5nF	1	2	3	µs
$t_{OVP\_ON(deg)\_GATE}$	GATE Turn on delay during OV	$V_{(OV)}$ ↓ to $V_{(GATE-SRC)}$ > 5V, $C_{(GATE-SRC)}$= 1.5nF	4	7	10	µs

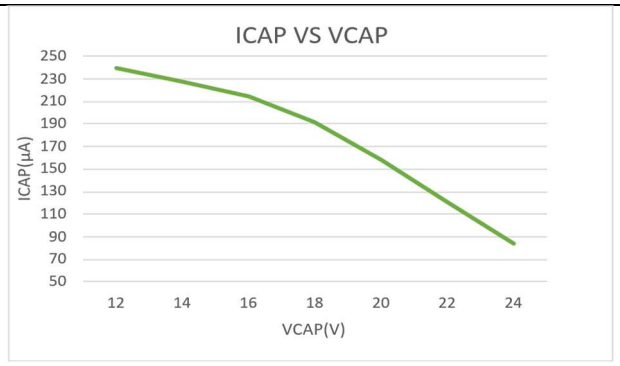
Characteristic plots

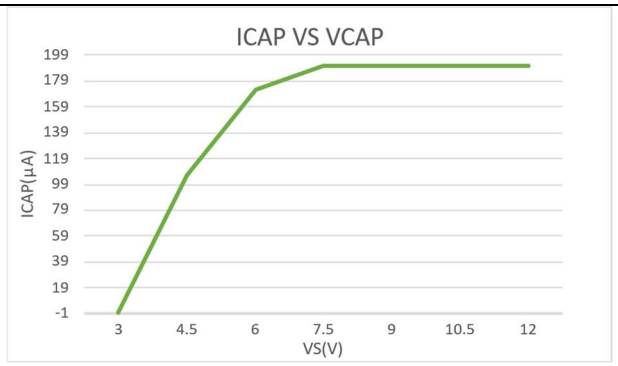
T_J =25°C, $V_{(ANODE)}$ =12V, $C_{(VCAP)}$ =1μF, $V_{(EN)}$ =3V (unless otherwise noted).

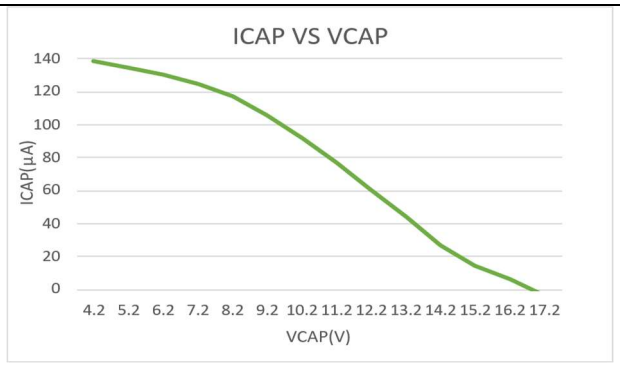


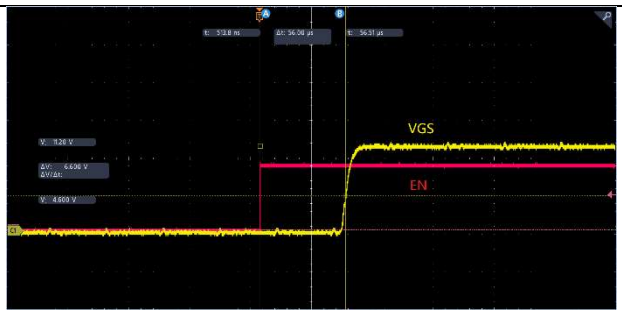


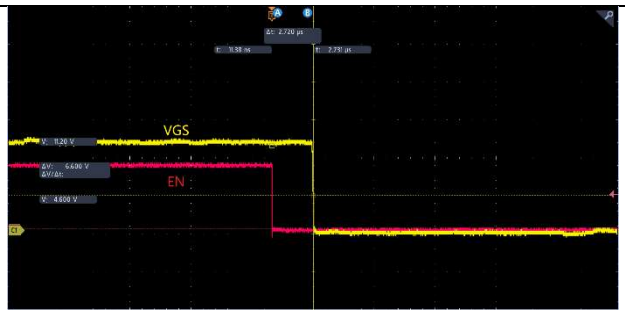


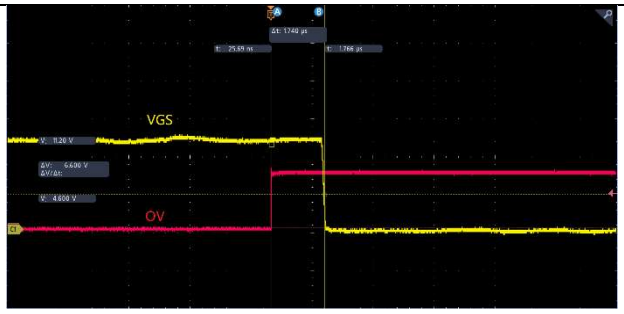
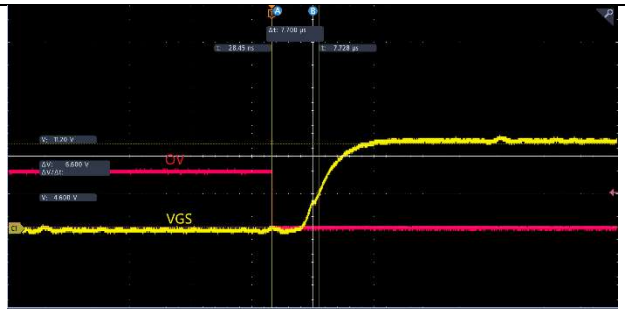
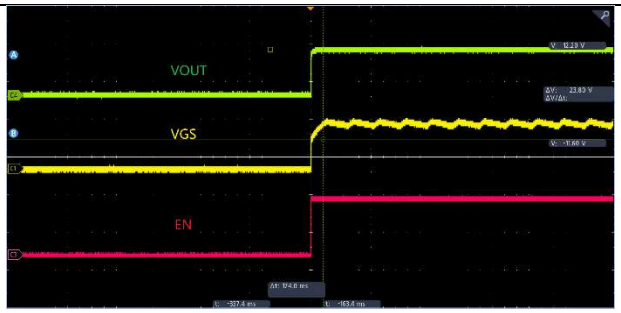
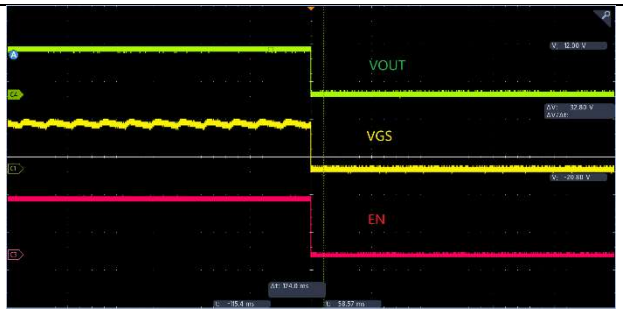
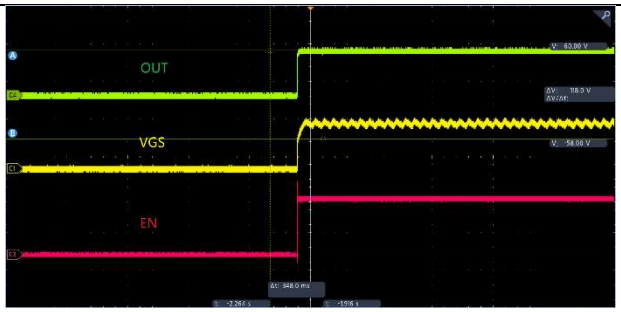
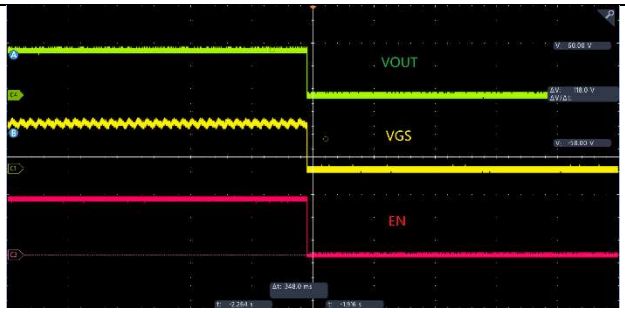




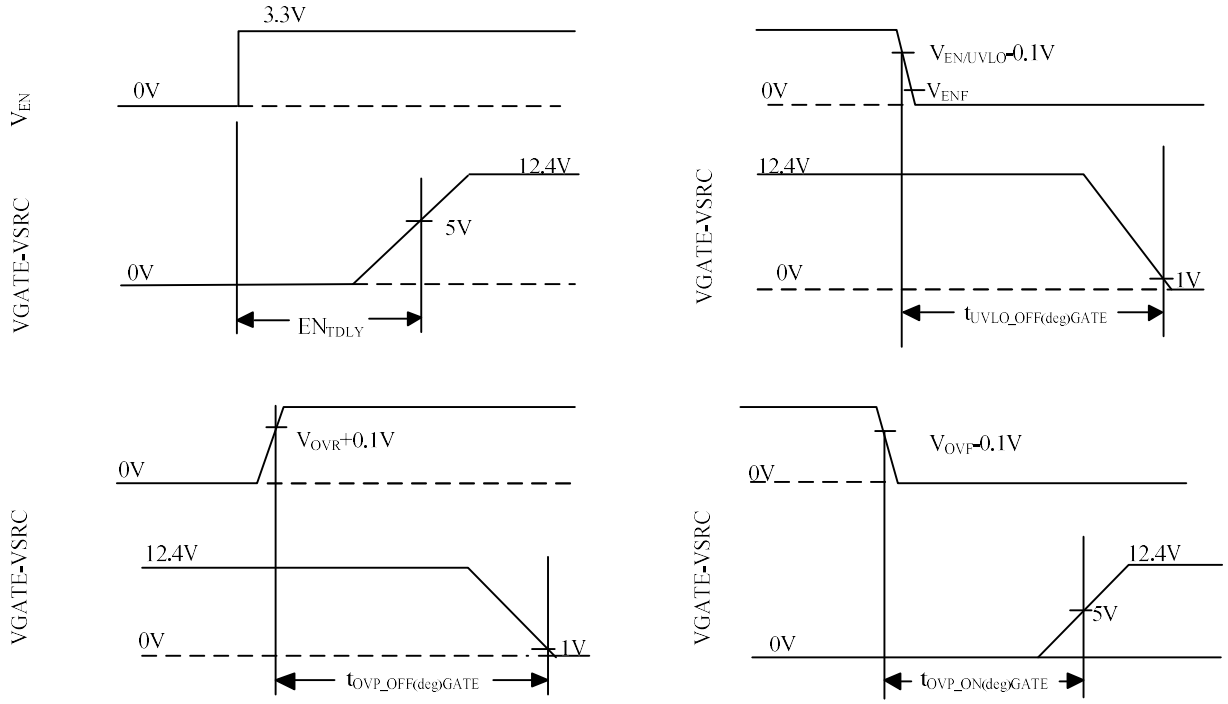






	
GATE Turn off delay during OV	GATE Turn on delay during OV
	
EN turn on when output is 12V3A	EN turn off when output is 12V3A
	
EN turn on when output is 60V3A	EN turn off when output is 60V3A

Parameter Measurement Information



Detailed description

Overview

The MX74502D23 controller has all the features necessary to implement an efficient and fast reverse polarity protection circuit with load disconnect feature. This easy to uses reverse polarity protection controller is paired with an external back-to-back connected N-channel MOSFETs to replace other reverse polarity schemes such as a P-channel MOSFETs. The wide input supply range of 4V to 85V allows protection and control of 12V、 24V 、48V and 60V input supply systems. The device can withstand and protect the loads from negative supply voltages down to –90V. An integrated charge pump drives external back-to-back connected N-channel MOSFETs with gate drive voltage of approximately 13V. MX74502D23 with its fast gate drive strength of 8mA peak is suitable for applications which need fast turn-on and turn-off of external MOSFET switch. MX74502D23 features adjustable overvoltage protection using the OV pin. With the enable pin low during the standby mode, both the external MOSFETs and controller off and draws a very low shutdown current of 1μA.

Input Voltage

The VS pin is used to power the MX74502D23's internal circuitry, typically drawing 150μA when enabled and 1μA when disabled. If the VS pin voltage is greater than the POR Rising threshold, then MX74502D23 operates in either shutdown mode or conduction mode in accordance with the EN/UVLO pin voltage. The voltage from VS to GND is designed to vary from 85V to –90V, allowing the MX74502D23 to withstand negative voltage transients.

Charge Pump (VCAP)

The charge pump supplies the voltage necessary to drive the external N-channel MOSFET. An external charge pump capacitor is placed between VCAP and VS pin to provide energy to turn on the external MOSFET. For the charge pump to supply current to the external capacitor the EN/UVLO pin voltage must be above the specified input high threshold, $V_{(EN\_UVLOR)}$. When enabled the charge pump sources a charging current of 110μA typically. If EN/UVLO pins is pulled low, then the charge pump remains disabled. To ensure that the external MOSFET can be driven above its specified threshold voltage, the VCAP to VS voltage must be above the undervoltage lockout threshold, typically 6.2V, before the internal gate driver is enabled. Use the following equation to calculate the initial gate driver enable delay

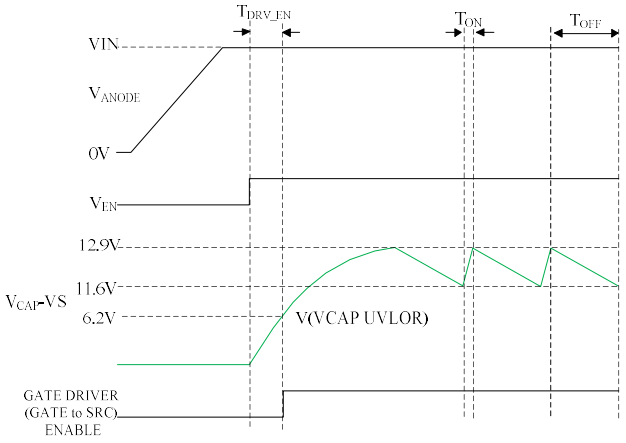
$$T_{(DRV\_EN)} = 75\mu s + C_{(VCAP)} \times \frac{V_{(VCAP\_UVLOR)}}{110\mu A}$$

where

• $C_{(VCAP)}$ is the charge pump capacitance connected across VS and VCAP pin

• $V_{(VCAP\_UVLOR)}$ = 6.2V(typical)

To remove any chatter on the gate drive approximately 1000mV of hysteresis is added to the VCAP undervoltage lockout. The charge pump remains enabled until the VCAP to VS voltage reaches 12.9V, typically, at which point the charge pump is disabled decreasing the current draw on the VS pin. The charge pump remains disabled until the VCAP to VS voltage is below to 11.6V typically at which point the charge pump is enabled. The voltage between VCAP and VS continues to charge and discharge between 11.6V and 12.9V as shown in following figure. By enabling and disabling the charge pump, the operating quiescent current of the MX74502D23 is reduced. When the charge pump is disable, it sinks 1μA typical when 12V input.



Gate Driver (GATE, SRC)

The gate driver is used to control the external N-Channel MOSFET by setting the appropriate GATE to SRC voltage.

Before the gate driver is enabled, the following three conditions must be achieved:

• The EN/UVLO pin voltage must be greater than the specified input high voltage.

• The VCAP to VS voltage must be greater than the undervoltage lockout voltage.

• The VS voltage must be greater than VS POR rising threshold.

If the above conditions are not achieved, then the GATE pin is

internally connected to the SRC pin, assuring that the external MOSFET is disabled. After these conditions are achieved, the gate driver operates in the conduction mode enhancing the external MOSFET completely.

Enable (EN/UVLO)

The MX74502D23 has an enable pin, EN/UVLO. The enable pin allows for the gate driver to be either enabled or disabled by an external signal. If the EN/UVLO pin voltage is greater than the rising threshold, the gate driver and charge pump operate as described in the Gate Driver (GATE, SRC*)* and Charge Pump (VCAP) sections. If the enable pin voltage is less than the input low threshold, the charge pump and gate driver are disabled placing the MX74502D23 in shutdown mode. The EN/UVLO pin can withstand a voltage as large as 85V and as low as –85V. This feature allows for the EN/UVLO pin to be connected directly to the VS pin if enable functionality is not needed. In conditions where EN/UVLO is left floating, the internal sink current of 2uA pulls EN/UVLO pin low and disables the device. An external resistor divider connected from input to EN/UVLO to ground can be used to implement the input Undervoltage Lockout (UVLO) functionality in the system. When EN/UVLO pin voltage is lower than UVLO comparator falling threshold ($V_{EN/UVLOF}$) but higher than enable falling threshold (V_{ENF}), the device disables gate drive voltage, however, charge pump is kept on. This action ensures quick recovery of gate drive when UVLO condition is removed. If UVLO functionality is not required, connect EN/UVLO pin to VS.

Overvoltage Protection (OV)

MX74502D23 provides programmable overvoltage protection feature with OV pin. A resistor divider can be connected from input source to OV pin to ground in order to set overvoltage threshold. An internal comparator compares the input voltage against fixed reference (1.43V) and disables the gate drive as soon as OV pin voltage goes above the OV comparator reference. When the resistor divider is referred from input supply side, device is configured for overvoltage cutoff functionality. When the resistor divider is referred from output side (V_{OUT}), the device is configured for overvoltage clamp functionality.

When OV pin voltage goes above OV comparator V_{OVR} threshold (1.43V typical), the device disables gate drive, however, charge pump remains active. When OV pin voltage falls below V_{OVF} threshold (1.39V typical), the gate is quickly turned on as charge pump is kept on and the device does not go through the device start-up process. When OV pin is not used, it can be connected to ground.

Device Functional Modes

Shutdown Mode

The MX74502D23 enters shutdown mode when the EN/UVLO pin voltage is below the specified input low threshold $V_{(ENF)}$. Both the gate driver and the charge pump are disabled in shutdown mode. During shutdown mode the MX74502D23 enters low I_Q operation with the VS pin only sinking 1μA of current.

Conduction Mode

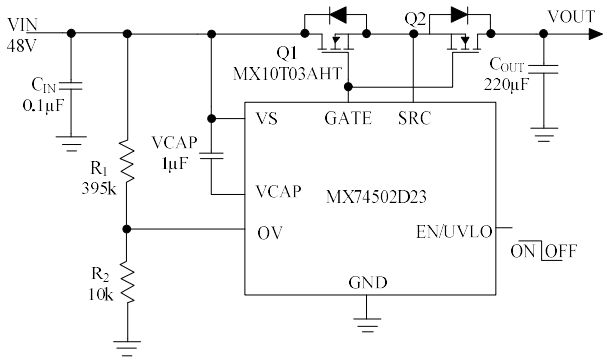
For the MX74502D23 to operate in conduction mode the gate driver must be enabled as described in the Gate Driver *(*GATE, SRC*)* section. If these conditions are achieved the GATE pin is Internally connected to the VCAP for fast turn-on of external FET in case of MX74502D23 gate drive is disabled when OV pin voltage is above V_{OVR} threshold or EN/UVLO pin voltage is lower than $V_{EN/UVLOF}$ threshold.

Application and Implementation

Application Information

The MX74502D23 is used with back-to-back connected N-Channel MOSFETs in a typical reverse polarity protection with load disconnect application. The schematic for the 48V input supply reverse polarity protection is shown in Typical Application diagram, where the MX74502D23 is used to drive the back-to-back connected MOSFETs Q1 and Q2 in series with a 48V supply.

Typical Application



Design Requirements

A design example, system design parameters are shown in the following table.

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	48V nominal
Overvoltage protection	58V
Output current	8A full load
Output capacitance	220µF typical output capacitance

Design Considerations

• Input operating voltage range (including overvoltage protection)

• Maximum load current

MOSFET Selection

The important MOSFET electrical parameters are the maximum continuous drain current I_D, the maximum drain-to-source voltage $V_{DS(MAX)}$, the maximum gate-to-source voltage $V_{GS(MAX)}$ and the drain-to-source on resistance R_{DSON}.

The maximum continuous drain current, I_D, rating must exceed the maximum continuous load current. The maximum drain-to-source voltage, $V_{DS(MAX)}$, must be high enough to withstand the highest differential voltage seen in the application. This requirement would include any anticipated fault conditions. The maximum V_{GS} MX74502D23 can drive is 13.8V, so a MOSFET with 15V minimum V_{GS} rating must be selected. If a MOSFET with V_{GS} rating < 15V is selected, a Zener diode can be used between GATE to SRC pin to clamp V_{GS} to safe level.

To reduce the MOSFET conduction losses, lowest possible $R_{DS(ON)}$ is preferred. Selecting a MOSFET with $R_{DS(ON)}$ that gives VDS drop 20mV to 50mV provides good trade off in terms of power dissipation and cost. As the load current is 8A, the MOSFET MX10T03AHT is ok for this application which the RDS(ON) is 4mΩ maximum.

Thermal resistance of the MOSFET must be considered against the expected maximum power dissipation in the MOSFET to ensure that the junction temperature (T_J) is well controlled.

Overvoltage Protection

Resistors R1 and R2 connected in series is used to program the overvoltage threshold. Connecting R1 to VIN provides overvoltage cutoff and switching the connection to VOUT provides overvoltage clamp response. By calculating the following formula, the resistance value required to set the overvoltage threshold V_{OV} to 58V is obtained.

$$V_{OVR} = \frac{R_2 \times V_{OV}}{R_1 + R_2}$$

For minimizing the input current drawn from the supply through resistors R1 and R2, it is recommended to use higher value of resistance. Using high value resistors adds error in the calculations because the current through the resistors at higher value becomes comparable to the leakage current into the OV pin. Select (R1 + R2) such that current through resistors is around 100 times higher than the leakage through OV pin. Based on the device's electrical characteristics, V_{OVR} is 1.43V, select (R1) = 395kΩ and R2 = 10kΩ as a standard resistor value to set overvoltage cutoff of 58V.

Charge Pump VCAP, Input and output Capacitance

Minimum required capacitance for charge pump VCAP and input and output capacitance are:

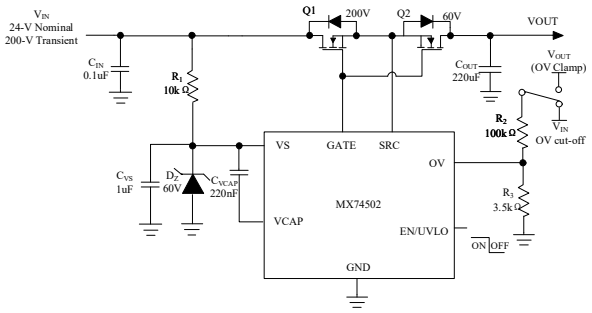
• C_{VCAP}: minimum recommended value of VCAP (µF) ≥50 × Effective $C_{ISS(MOSFET)}$(µF), 0.22µF is selected

• C_{IN}: typical input capacitor of 0.1µF

• C_{OUT}: typical output capacitor 220µF

Input Surge Stopper Using MX74502D23

Many industrial applications need to comply with input overvoltage transients and surge events specified by standards such as IEC61000-4-x. MX74502D23 can be configured as input surge stopper to provide overvoltage along with input reverse supply protection.



As shown in the figure above MOSFET Q1 is used to turn off or clamp output voltage to acceptable safe level and protect the MOSFET Q2 and MX74502D23 from input transient. Note that only the VS pin is exposed to input transient through a resistor, R1. A 60V rated Zener diode is used to clamp and protect the VS pin within recommended operating condition. Rest of the circuit is not exposed to higher voltage as the MOSFET Q1 can either be turned off completely or output voltage clamped to safe level.

VS Capacitance, Resistor R_1 and Zener Clamp (D_Z)

A minimum of 0.1µF C_{VS} capacitance is required. During input overvoltage transient, resistor R1 and Zener diode D_Z are used to protect VS pin from exceeding the maximum ratings by clamping V_{VS} to 60V. Choosing R1 = 10kΩ, the peak power dissipated in

Zener diode D_Z can be calculated as follows.

$$P_{DZ} = V_{DZ} \times \frac{(V_{IN(MAX)} - V_{DZ})}{R_1}$$

Where V_{DZ} is the breakdown voltage of Zener diode. Select the Zener diode which can handle peak power requirement.

Peak power dissipated in resistor R1 can be calculated as follows

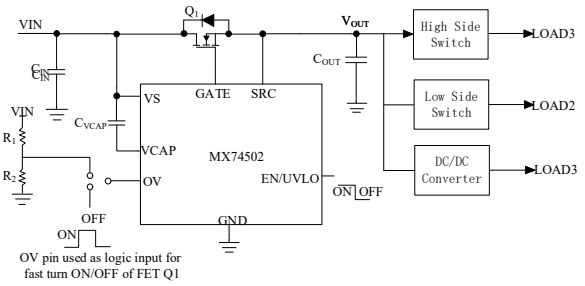
$$P_{R1} = \frac{(V_{IN(MAX)} - V_{DZ})^2}{R_1}$$

Select a resistor package which can handle peak power and maximum DC voltage.

Fast Turn-On and Turn-Off High Side Switch Driver Using MX74502D23

In applications such as industrial motor drives and safety power line communication digital output modules, N-Channel MOSFET based high side switch is very commonly used to disconnect the loads from supply line in case of faults such as overvoltage event. MX74502D23 can be used to drive external MOSFET to realize simple high side switch with overvoltage protection. The following diagram shows a typical application circuit where MX74502D23 is used to drive external MOSFET Q1 as a main power path connect and disconnect switch. A resistor divider from input to OV pin to ground can be used to set the overvoltage threshold.

If VOUT node (SRC pin) of the device is expected to drop in case of events such as overcurrent or short-circuit on load side, then additional Zener diode is required across gate and source pin of external MOSFET to protect it from exceeding its maximum V_{GS} rating.



Many industrial safety applications require fast switching off of MOSFET to verify proper functioning of the high side disconnect switch for diagnostic purposes. MX74502D23H OV pin can be used as control input to realize fast turn-on and turn-off load switch functionality. With OV pin pulled above V_{OVR} threshold of (1.43V typical), MX74502D23H turns off the external MOSFET (with Ciss = 4.7nF) within 1µs typically. When the OV pin is pulled low, MX74502D23H with its peak gate drive strength of 8 mA turns on external MOSFET with turn on speed of 8µs typical.

Power Supply Recommendations

The MX74502D23 reverse polarity protection controller is designed for the supply voltage range of $4V \leq V_S \leq 85V$. If the input supply is located more than a few inches from the device, MAXIN recommends an input ceramic bypass capacitor higher than 0.1µF. To prevent MX74502D23 and surrounding components from being damaged under the conditions of a direct output short circuit, use a power supply having overload and short-circuit protection.

Layout

Layout Guidelines

• Place the input capacitor C_{IN} of 0.1µF minimum close to VS pin to ground. This typically helps with better EMI performance.

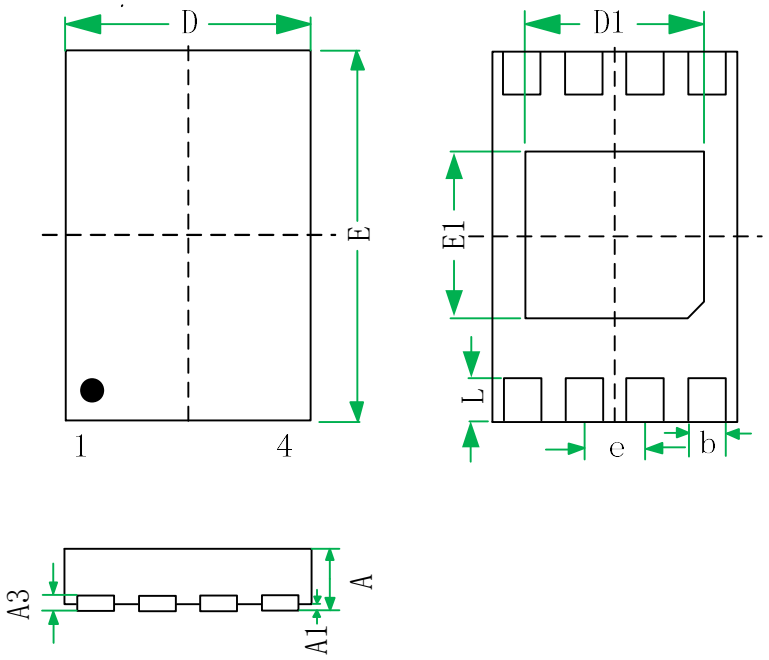
• Connect GATE and SRC pin of MX74502D23 close to the MOSFET's GATE and SOURCE pin.

• Use thick traces for source and drain of the MOSFET to minimize resistive losses because the high current path of for this solution is through the MOSFET.

• The charge pump capacitor across VCAP and VS pin must be kept away from the MOSFET to lower the thermal effects on the capacitance value.

• The GATE pin of the MX74502D23 must be connected to the MOSFET gate with short trace. Avoid excessively thin and long running trace to the Gate Drive.

Package information



DFN2*3-8L for MX74502D23

SYMBOL	MILLIMETERS		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.18	0.20	0.25
D	1.90	2.00	2.10
E	2.90	3.00	3.10
D1	1.40	1.50	1.60
E1	1.50	1.60	1.70
b	0.20	0.25	0.30
e		0.500BSC	
L	0.35	0.40	0.45

Restrictions on Product Use

◆ MAXIN micro is continually working to improve the quality and reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing MAXIN products, to comply with the standards of safety in making a safe design for the entire system, and to avoid situations in which a malfunction or failure of such MAXIN products could cause loss of human life, bodily injury or damage to property.

◆ In developing your designs, please ensure that MAXIN products are used within specified operating ranges as set forth in the most recent MAXIN products specifications.

◆ The information contained herein is subject to change without notice.

Version update record:

Preliminary: the original version.

V11: updated detailed electrical characteristics and block diagram.

V12: updated the package information.