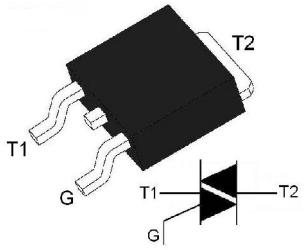
Triacs

TO-252-2L

RoHS COMPLIANT

General Description

Glass passivated triacs in a plastic envelope, intended for use in applications requiring high bidirectional transient and blocking voltage capability and high thermal cycling performance. Typical applications include motor control, industrial and domestic lighting, heating and static switching.



Absolute Maximum Rating (Ta=25°C)

Limiting values in accordance with the Absolute Maximum System

Parameter	Symbol	Conditions		Min	Max			Unit
Repetitive peak off-state voltages	V_{RRM} V_{DRM}			-	-500 500	-600 600	-800 800	V
On-State RMS Current	$I_{T(RMS)}$	full sine wave; $T_{mb} \leq 107$ °C		-	4			A
Non-repetitive peak on-state current	I_{TSM}	full sine wave; T_j = 25 °C prior to surge	t = 20 ms	-	25			A
			t = 16.7 ms	-	27			
I^2t for fusing	I^2t	t = 10 ms		-	3.1			A^2s
Repetitive rate of rise of on-state current after triggering	dI_T/dt	I_{TM} = 3 A; I_G = 0.2 A; dI_G/dt = 0.2 A/µs			50			A/µs
Peak gate current	I_{GM}			-	2			A
Peak Gate Voltage	V_{GM}			-	5			V
Peak gate power	P_{GM}			-	5			W
Average gate power	$P_{G(AV)}$	over any 20 ms period		-	0.5			W
Operating junction temperature	T_J			-	125			°C
Storage Temperature	Tstg			-40	150			°C

Thermal Resistances

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Thermal resistance junction to solder point	Rth j-sp	full or half cycle	-		3.0	K/W
Thermal resistance junction to ambient	Rth j-a	pcb mounted;	-	75		K/W

Static Characteristics (T_j = 25 °C unless otherwise stated)

Snubberless™ and logic level (3 Quadrants)

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
Gate trigger current	I_{GT}	V_D = 12 V, I_T = 0.1 A	I - II -III			10	mA
Latching current	I_L	V_D = 12 V, I_{GT} = 0.1 A	I -III			15	mA
			II			20	
Holding current	I_H	V_D = 12 V, I_{GT} = 0.1 A	I -III			15	mA
			II			20	
On-state voltage	V_T	I_T = 5A			1.4	1.7	V
Gate trigger voltage	V_{GT}	V_D = 12 V; I_T = 0.1 A			0.7	1.5	V
		V_D = 400 V; I_T = 0.1 A; T_j = 125 °C		0.25	0.4		
Off-state leakage current	I_D	V_D = $V_{DRM(max)}$; T_j = 125 °C				0.5	mA

Standard (4 Quadrants)

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
Gate trigger current	I_{GT}	V_D = 12 V, I_T = 0.1 A	I - II -III			10	mA
			IV			15	
Latching current	I_L	V_D = 12 V, I_{GT} = 0.1 A	I -III-IV			15	mA
			II			20	
Holding current	I_H	V_D = 12 V, I_{GT} = 0.1 A	I -III-IV			15	mA
			II			20	
On-state voltage	V_T	I_T = 5A			1.4	1.7	V
Gate trigger voltage	V_{GT}	V_D = 12 V; I_T = 0.1 A			0.7	1.5	V
		V_D = 400 V; I_T = 0.1 A; T_j = 125 °C		0.25	0.4		
Off-state leakage current	I_D	V_D = $V_{DRM(max)}$; T_j = 125 °C				0.5	mA

Dynamic Characteristics Tj = 25 ˚C unless otherwise stated

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Critical rate of rise of off-state voltage	dV_D/dt	V_{DM} =67% V_{DRM}(max); T_j = 125 °C exponential waveform; gate open circuit		50	-	V/μs
Gate controlled turn-on time	tgt	I_{TM} = 6 A; V_D = $V_{DRM(max)}$; I_G = 0.1 A; dI_G/dt = 5 A/μs;		2		μs

Typical Characteristics

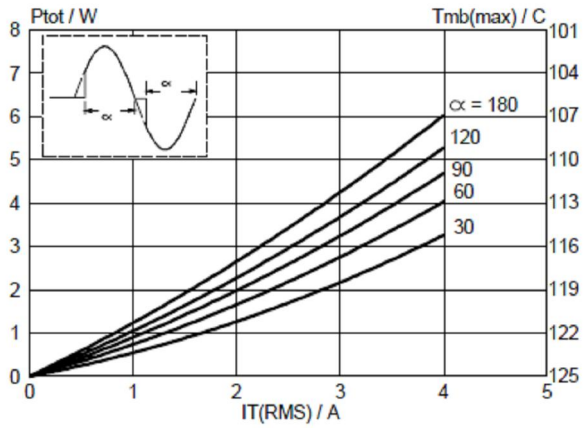


Fig.1. Maximum on-state dissipation, Ptot, vs rms on-state current, $I_{T(RMS)}$, where α = conduction angle.

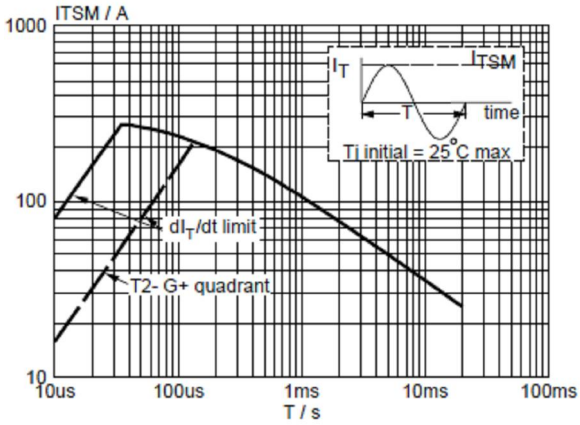


Fig.2. Maximum permissible non-repetitive peak on-state current I_{TSM}, vs pulse width tp, for sinusoidal currents, tp ≤ 20ms.

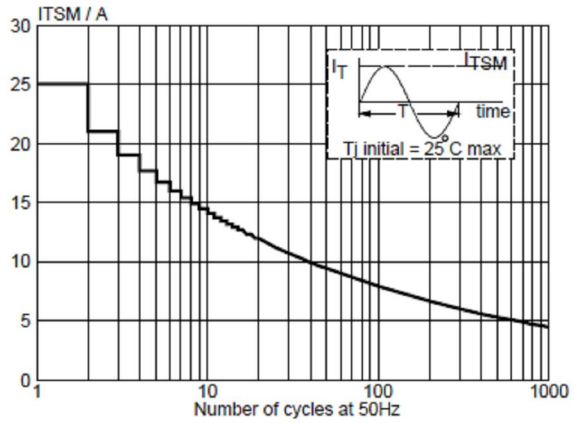


Fig.3. Maximum permissible non-repetitive peak on-state current I_{TSM}, vs number of cycles, for sinusoidal currents, f = 50 Hz.

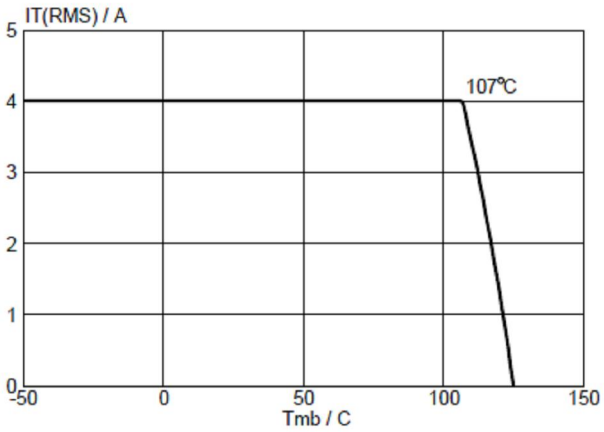


Fig.4. Maximum permissible rms current $I_{T(RMS)}$ vs mounting base temperature T_{mb}.

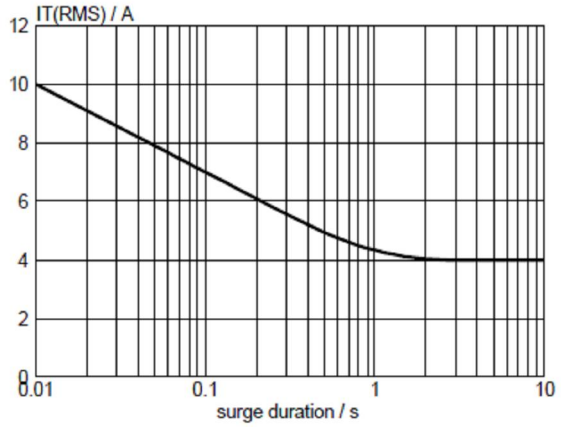


Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, vs surge duration, for sinusoidal currents, f = 50 Hz; T_{mb}≤107˚C.

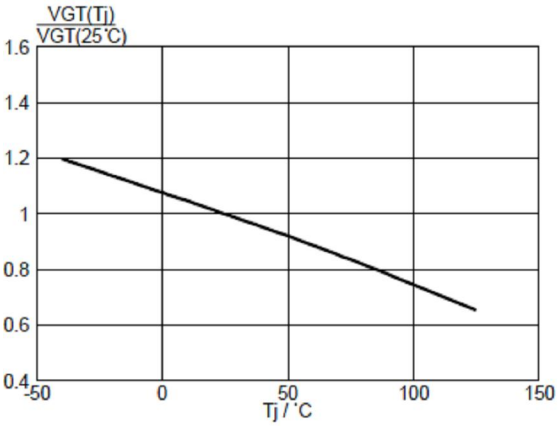


Fig.6. Normalised gate trigger voltage V_{GT}(Tj)/ V_{GT}(25˚C), vs junction temperature T_j.

Typical Characteristics

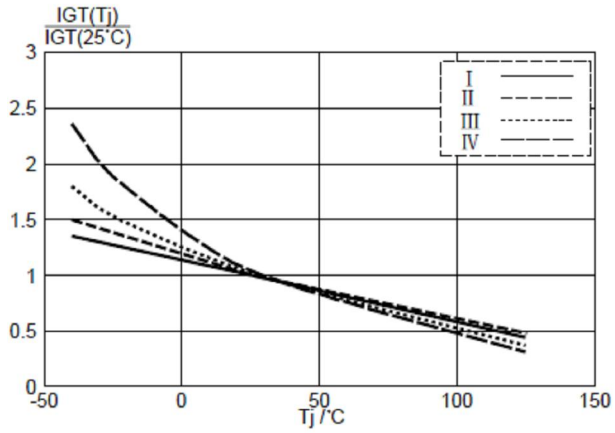


Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25^{\circ}C)$, vs junction temperature T_j.

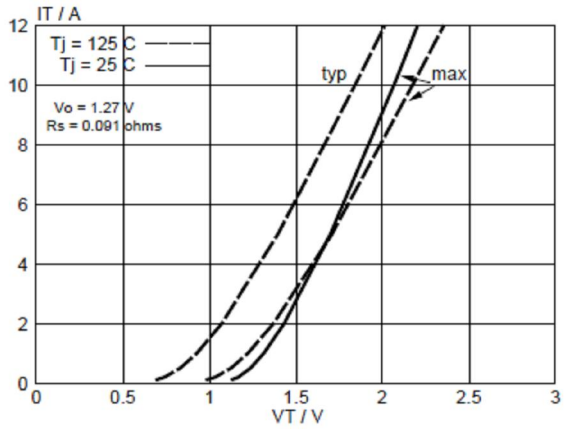


Fig.8. Typical and maximum on-state characteristic.

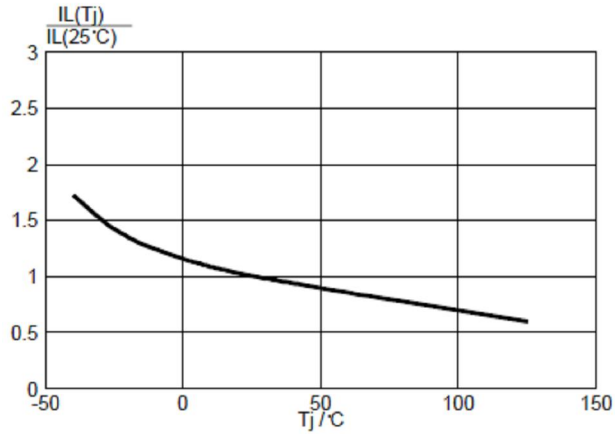


Fig.9. Normalised latching current $I_L(Tj)/ I_L(25^{\circ}C)$, vs junction temperature T_j.

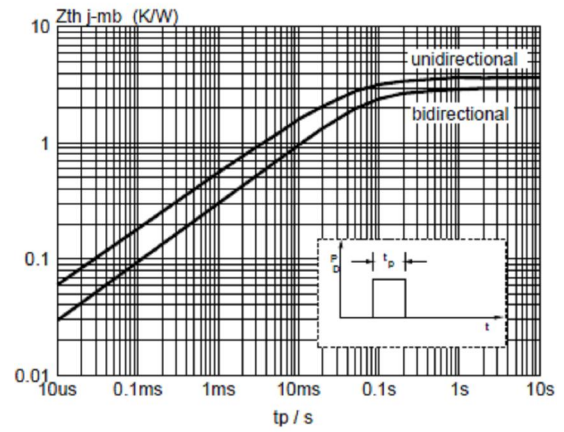


Fig.10. Transient thermal impedance Zth j-mb, vs pulse width tp.

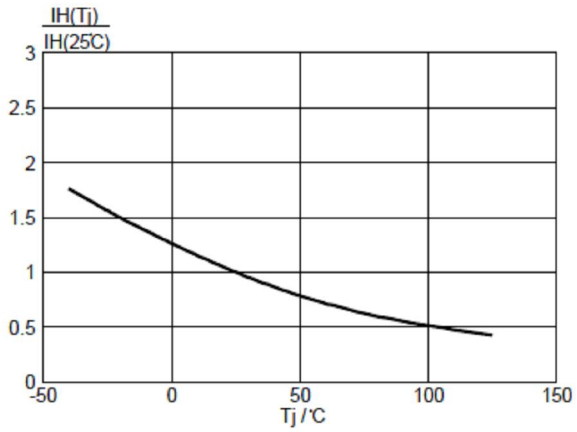


Fig.11. Normalised holding current $I_H(Tj)/ I_H(25^{\circ}C)$, vs junction temperature T_j.

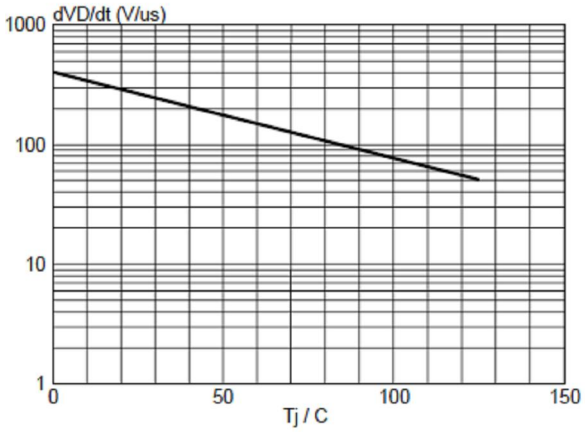
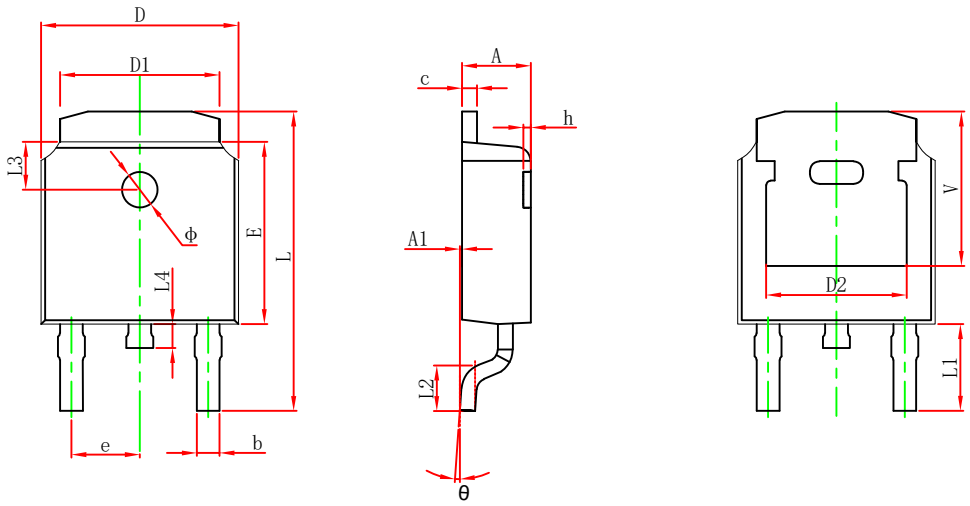


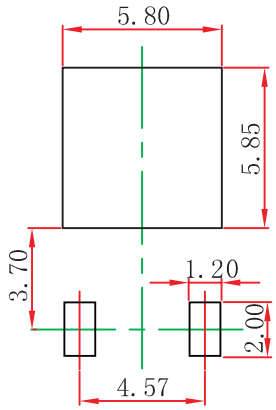
Fig.12. Typical, critical rate of rise of off-state voltage, dV_D/dt vs junction temperature Tj.

TO-252-2L Package Outline Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	2.200	2.400	0.087	0.094
A1	0.000	0.127	0.000	0.005
b	0.635	0.770	0.025	0.030
c	0.460	0.580	0.018	0.023
D	6.500	6.700	0.256	0.264
D1	5.100	5.460	0.201	0.215
D2	4.830 REF.		0.190 REF.	
E	6.000	6.200	0.236	0.244
e	2.186	2.386	0.086	0.094
L	9.712	10.312	0.382	0.406
L1	2.900 REF.		0.114 REF.	
L2	1.400	1.700	0.055	0.067
L3	1.600 REF.		0.063 REF.	
L4	0.600	1.000	0.024	0.039
Φ	1.100	1.300	0.043	0.051
θ	0°	8°	0°	8°
h	0.000	0.300	0.000	0.012
V	5.250 REF.		0.207 REF.	

TO-252-2L Suggested Pad Layout



Note:
1.Controlling dimension:in millimeters.
2.General tolerance:± 0.05mm.
3.The pad layout is for reference purposes only.