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PRODUCT SPECIFICATION

Customer : _____

Product Name : Real Time Clock

Part NO : FRTC85063

Issue Date : _____

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Prepared	Checked	Customer Check
ChenTT	Zelig	

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1 Features

- Provides year, month, day, weekday, hours, minutes, and seconds based on a 32.768 kHz quartz crystal
- Clock operating voltage: 1.1 V to 5.5 V
- Low current; typical 0.3 μA at VDD = 3.3 V and Tamb = 25 ℃
- 400 kHz two-line IIC-bus interface (at VDD = 1.8 V to 5.5 V)
- Programmable clock output for peripheral
- devices (32.768 kHz, 16.384 kHz, 8.192 kHz, 4.096 kHz, 2.048 kHz, 1.024 kHz, and 1 Hz)
- Selectable integrated oscillator load
- capacitors for C_L = 7 pF or C_L = 12.5pF
- Alarm function
- Countdown timer
- Minute and half minute interrupt
- Oscillator stop detection function
- Internal Power-On Reset (POR)
- Programmable offset register for frequency adjustment

2 Applications

- Digital still camera
- Digital video camera
- Printers
- Copy machines
- Mobile equipment
- Battery powered devices

3 Description

The FRTC85063 is a CMOS Real-Time Clock (RTC) and calendar optimized for low power consumption. An offset register allows fine-tuning of the clock. All addresses and data are transferred serially via the two-line bidirectional I2C-bus. Maximum data rate is 400 kbit/s. The register address is incremented automatically after each written or read data byte.

4 Ordering Information

Ordering Code	Package	Package Description
FRTC85063S	SOP8	4.9mm x 6mm
FRTC85063M	MSOP8	3mm x 4.9mm
FRTC85063Q	TDFN 2.6x2.6-10L	2.6mm x 2.6mm

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5 Function Block

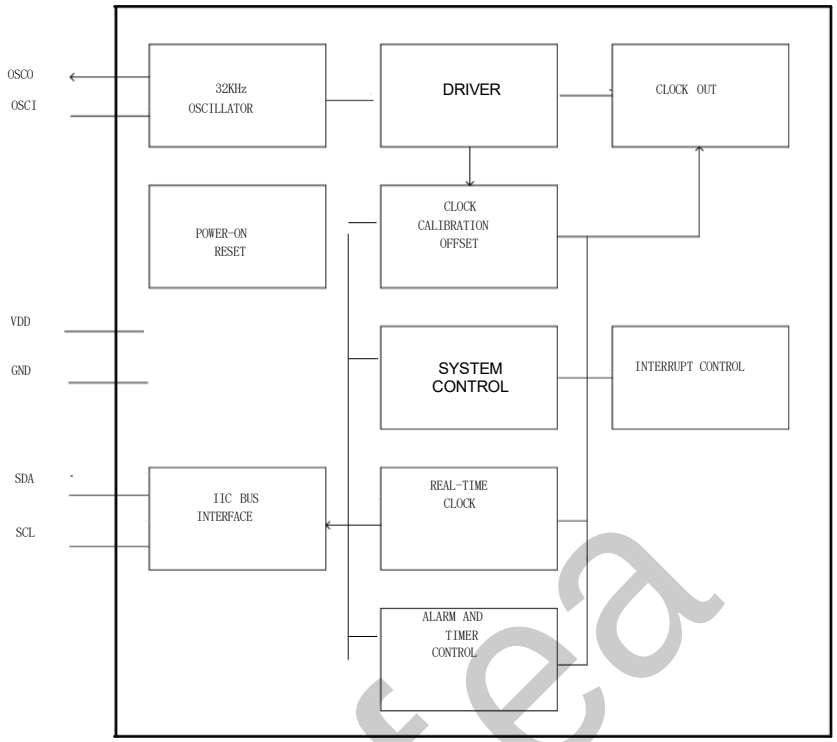
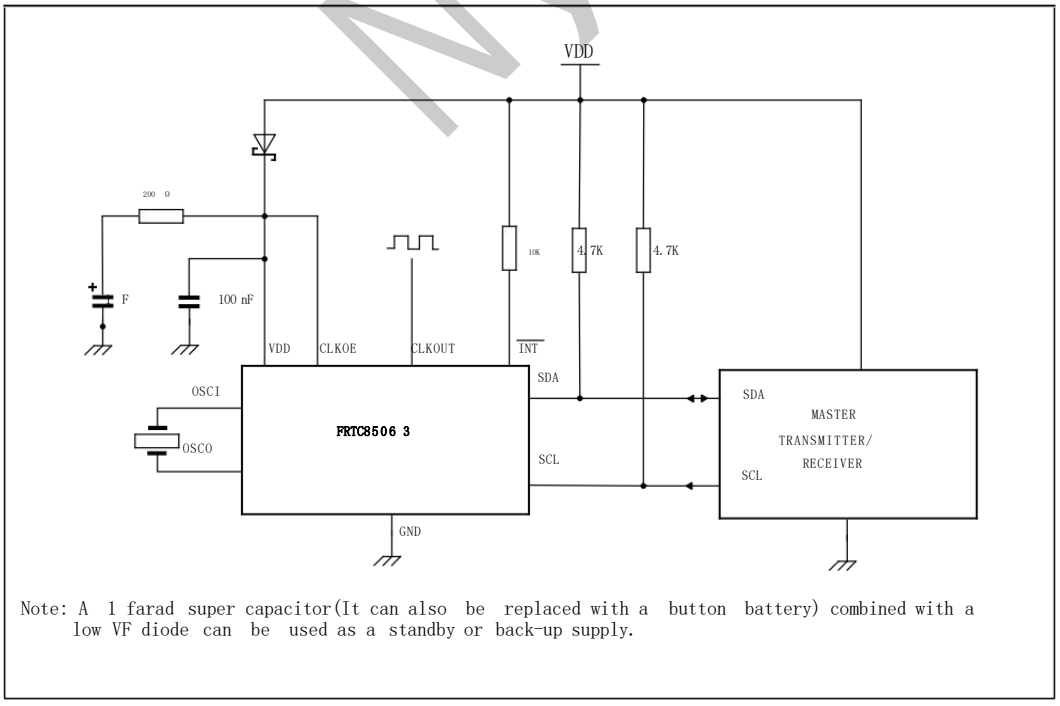


Figure1 Function block

6 Typical Application Circuit



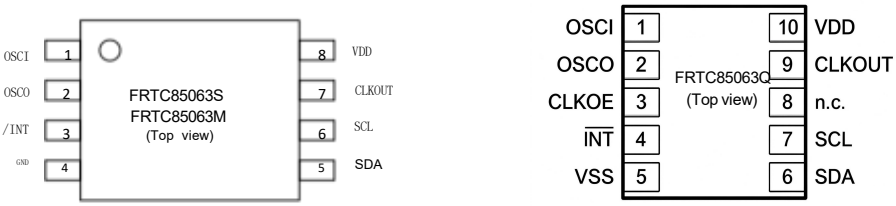
Note: A 1 farad super capacitor(It can also be replaced with a button battery) combined with a low VF diode can be used as a standby or back-up supply.

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7 Pin Configuration

Figure2 Typical application circuit



Pin configuration

Figure3

8 Pin Description

Pin Number		Pin Name	Type	Description
PIN8	PIN10			
1	1	OSCI	I	oscillator input
2	2	OSCO	O	oscillator output
__	3	CLKOE[1]	I	CLKOUT enable or disable pin; enable is active HIGH
3	4	/INT[1]	O	interrupt output (open-drain)
4	5	GND	P	ground supply voltage
5	6	SDA[1]	I/O	serial data line
6	7	SCL[1]	I	serial clock input
_	8	NC	/	not connected
7	9	CLKOUT	O	clock output (push-pull)
8	10	VDD	P	supply voltage

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9 Function Description

The FRTC85063 integrates multiple functional blocks within a single device: eighteen 8-bit registers featuring automatic address incrementation, an on-chip 32.768 kHz oscillator with built-in capacitance, a frequency divider that supplies the reference clock for the Real-Time Clock (RTC) and calendar functions, and an I2C-bus interface supporting data rates up to 400 kbit/s.

The internal address pointer automatically advances following each byte read or write operation, continuing sequentially up to register address 11h. Upon reaching this boundary, the next increment causes the address to wrap back to 00h.

All registers are implemented as addressable 8-bit parallel registers, though certain bit positions remain unused. The register map is organized as follows.

Addresses 00h and 01h – Control and status registers

Address 02h – Offset adjustment register for clock fine-

tuning Address 03h – General-purpose RAM byte (user-

accessible)

Addresses 04h through 0Ah – Time-keeping counters (seconds through years)

Addresses 0Bh through 0Fh – Alarm condition registers

Addresses 10h, 11h, and 12h – Timer function registers

Time and calendar data—including seconds, minutes, hours, days, months, and years, along with their corresponding alarm settings—are all represented in Binary Coded Decimal (BCD) format.

To ensure data integrity, the device freezes all time counter values whenever any RTC register is accessed (either read or written). This mechanism prevents erroneous reading or writing of the clock/calendar data during internal carry operations (e.g., rollover conditions). Please refer to the separate specification for detailed timing constraints regarding maximum access duration.

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11 Registers Table

Addr. (hex)	Function (time range BCD format)	Register definition							
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Control and status registers									
00	Control_ 1	EXT_TEST	_	STOP	SR	_	CIE	12_24	CAP_SEL
01	Control_2	AIE	AF	MI	HMI	TF	COF[2:0]		
02	Offset	MODE	OFFSET [6:0]						
03	RAM_byte	B [7:0]							
Time and date registers									
04	Seconds	OS	SECONDS (0 to 59)						
05	Minutes	_	MINUTES (0 to 59)						
06	Hours	_	_	AMPM	HOURS (1 to 12) in 12-hour mode				
				HOURS (0 to 23) in 24-hour mode					
07	Days	_	_	DAYS (1 to 31)					
08	Weekdays	_	_	_	_	_	WEEKDAYS (0 to 6)		
09	Months	_	_	_	MONTHS (1 to 12)				
0A	Years	YEARS (0 to 99)							
Alarm register									
0B	Second_alarm	AEN_S	SECOND _ALARM (0 to 59)						
0C	Minute_alarm	AEN__M	MINUTE _ALARM (0 to 59						
0D	Hour_alarm	AEN__H	_	AMPM	HOUR_ALARM (1 to 12) in 12-hour mode				
				HOUR_ALARM (0 to 23) in 24-hour mode					
0E	Day_alarm	AEN__D	_	DAY_ALARM (1 to 31)					
0F	Weekday_alarm	AEN__W	_	_	_	_	WEEKDAY_ALARM(0 to 6)		
Timer registers									
10	Timer_value	T [7:0]							
11	Timer_mode	_	_	_	TCF [1:0]		TE	TIE	TI__TP
12	Timer_value	T [15:8]							

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12 Control and status register

To ensure that all control registers will be set to their default values, the VDD level must be at zero volts at initial power-up. If this is not possible, a reset must be initiated with the software reset command when power is stable.

Control_1 Register(0X00)

Bit	Symbol	W/R	Default value	Description
7	EXT_TEST	RW	0	**external clock test mode** **0** = normal mode **1** = external clock test mode
6	_	RO	0	unused
5	STOP	RO	0	**STOP bit** **0** = RTC clock runs **1** = RTC clock is stopped; all RTC dividerchain flip-flops are asynchronously set logic 0
4	SR	RW	0	**software reset** **0** = no software reset **1** = initiate software reset[1]; this bit always returns a 0 when read
3	_	RO	0	unused
2	CIE	RW	0	**correction interrupt enable** **0** = no correction interrupt generated **1** = interrupt pulses are generated at every correction cycle
1	12_24	RW	0	**12 or 24-hour mode** **0** = 24-hour mode is selected **1** = 12-hour mode is selected
0	CAP_SEL	RW	0	**internal oscillator capacitor selection** for quartz crystals with a corresponding load capacitance **0** = 7 pF **1** = 12.5 pF

Note:
[1] For a software reset, 01011000 (58h) must be sent to register Control_1

12.1 External clock test mode

The device provides a dedicated test mode to facilitate board-level verification and debugging. When activated, this mode enables users to apply external test stimuli and exercise direct control over RTC functionality.
To enable test mode, the EXT_TEST bit within the Control_1 register must be set to logic high. Upon entering this mode, the CLKOUT pin undergoes a functional reconfiguration, transitioning from an output to an input. The internal clock source is then substituted with the external signal supplied through the
CLKOUT pin.
The external clock signal applied to CLKOUT must adhere to the following timing specifications: minimum pulse width of 300 ns and maximum period of 1,000 ns. This externally derived clock feeds into an internal 26-stage divider chain (prescaler), which scales the frequency down to the 1 Hz rate required for RTC timekeeping.
The prescaler can be forced into a known initial condition through the STOP bit. When the STOP bit is asserted, the prescaler counter is cleared to zero. (The STOP bit must be de-asserted before the prescaler resumes normal counting operation.)
Following a stop condition, the first 1-second increment occurs after 32 rising edges have been detected on the CLKOUT pin. Subsequently, each additional 1-second increment takes place after every 64 rising edges.

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Remark: Entry into test mode is not synchronized to the internal 64 Hz clock. When entering the test mode, no assumption as to the state of the prescaler can be made.

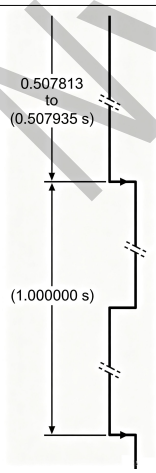
Operation example:

1. Set EXT_TEST test mode (register Control_1, bit EXT_TEST = 1).
2. Set STOP (register Control_1, bit STOP = 1).
3. Clear STOP (register Control_1, bit STOP = 0).
4. Set time registers to desired value.
5. Apply 32 clock pulses to pin CLKOUT.
6. Read time registers to see the first change.
7. Apply 64 clock pulses to pin CLKOUT.
8. Read time registers to see the second change.

Repeat 7 and 8 for additional increments.

12.2 STOP bit function

The function of the STOP bit is to allow for accurate starting of the time circuits. The STOP bit function causes the upper part of the prescaler (F2 to F14) to be held in reset and thus no 1 Hz ticks are generated. It also stops the output of clock frequencies below 8 kHz on pin CLKOUT.

Bit	Prescaler bits	[1] 1 Hz tick	Time	Comment
STOP	F0F1-F2 to F14		hh:mm:ss	
Clock is running normally				
0	01-0 0001 1101 0100		12:45:12	prescaler counting normally
STOP bit is activated by user. F_0 F_1 are not reset and values cannot be predicted externally				
1	XX-0 0000 0000 0000		12:45:12	prescaler is reset; time circuits are frozen
New time is set by user				
1	XX-0 0000 0000 0000		08:00:00	prescaler is reset; time circuits are frozen
STOP bit is released by user				
0	XX-0 0000 0000 0000		08:00:00	prescaler is now running
	XX-1 0000 0000 0000		08:00:00	
	XX-0 1000 0000 0000		08:00:00	
	XX-1 1000 0000 0000		08:00:00	
	:		:	
	11-1 1111 1111 1110		08:00:00	
	00-0 0000 0000 0001		08:00:01	0 to 1 transition of F14 increments the time circuits
	10-0 0000 0000 0001		08:00:01	
	:		:	
	11-1 1111 1111 1111		08:00:01	
	00-0 0000 0000 0000		08:00:01	
	10-0 0000 0000 0000		08:00:01	
	:		:	
	11-1 1111 1111 1110		08:00:01	
	00-0 0000 0000 0001		08:00:02	0 to 1 transition of F_{14} increments the time circuits

Note:

[1] F_0 is clocked at 32.768 kHz.

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The lower two stages of the prescaler (F_0 and F_1) are not reset. And because the I2C-bus is asynchronous to the crystal oscillator, the accuracy of restarting the time circuits is between zero and one 8.192 kHz cycle.

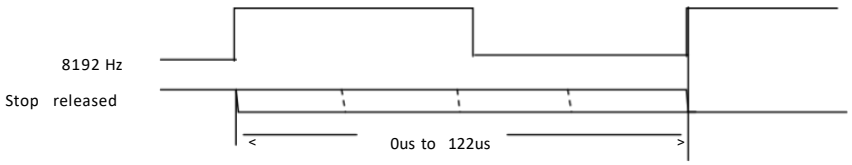


Figure4 STOP bit release timing

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The first increment of the time circuits is between 0.507813 s and 0.507935 s after STOP bit is released. The uncertainty is caused by the prescaler bits F0 and F1 not being reset and the unknown state of the 32 kHz clock.

12.3 Software reset

A reset is automatically generated at power-on. There is a low probability that some devices will have corruption of the registers after the automatic power-on reset if the device is powered up with a residual VDD level. It is required that the VDD starts at zero volts at power up or upon power cycling to ensure that there is no corruption of the registers. If this is not possible, a reset must be initiated after power-up (i.e. when power is stable) with the software reset command. Software reset command is setting Control_1 (00h) to 01011000 (58h) In reset state, registers are set according to Table and the address pointer returns to address 00h.

Address	Register name	Bit							
		7	6	5	4	3	2	1	0
00h	Control_ 1	0	0	0	0	0	0	0	0
01h	Control_2	0	0	0	0	0	0	0	0
02h	Offset	0	0	0	0	0	0	0	0
03h	RAM_byte	0	0	0	0	0	0	0	0
0Bh	Second_alarm	1	0	0	0	0	0	0	0
0Ch	Minute_alarm	1	0	0	0	0	0	0	0
0Dh	Hour_alarm	1	0	0	0	0	0	0	0
0Eh	Day_alarm	1	0	0	0	0	0	0	0
0Fh	Weekday_alarm	1	0	0	0	0	0	0	0
10h	Timer_value	0	0	0	0	0	0	0	0
11h	Timer_mode	0	0	0	1	1	0	0	0

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12.4 Control_2 Register(0x01)

Bit	Symbol	Default Value	Description
7	AIE	0	**alarm interrupt** 0 = Disabled 1 = Enabled
6	AF	0	**alarm flag** 0 = read: alarm flag inactive 0 = write: alarm flag is cleared 1= read: alarm flag active 1= write: alarm flag remains unchanged
5	MI	0	**minute interrupt** 0=Disabled 1=Enabled
4	HMI	0	**half minute interrupt** 0=Disabled 1=Enabled
3	TF	0	**timer flag** 0=no timer interrupt generated 1=flag set when timer interrupt generated
2 to 0	COF [2:0]	000	**CLKOUT control**

Note:
[1] For a software reset, 01011000 (58h) must be sent to register Control_1

AIE: This bit activates or deactivates the generation of an interrupt when AF is asserted, respectively. **AF:** When an alarm occurs, AF is set logic 1. This bit maintains its value until overwritten by command.

To prevent one flag being overwritten while clearing another, a logic AND is performed during a write access.

12.5 MI and HMI: minute and half minute interrupt

The minute interrupt (bit MI) and half minute interrupt (bit HMI) are pre-defined timers for generating interrupt pulses on pin INT; The timers are running in sync with the seconds counter.

The minute and half minute interrupts must only be used when the frequency offset is set to normal mode (MODE = 0), In normal mode, the interrupt pulses on pin INT are 1⁄64 s wide.

When starting MI, the first interrupt will be generated after 1 second to 59 seconds. When starting HMI, the first interrupt will be generated after 1 second to 29 seconds.

Subsequent periods do not have such a delay. The timers can be enabled independently from one another. However, a minute interrupt enabled on top of a half minute interrupt is not distinguishable.

12.6 Effect of bits MI and HMI on INT generation

Minute interrupt (bit MI)	Half minute interrupt (bit HMI)	Result
0	0	no interrupt generated
1	0	an interrupt every minute
0	1	an interrupt every 30 s
1	1	an interrupt every 30 s

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The duration of the timer is affected by the register Offset. Only when OFFSET[6:0] has the value 00h the periods are consistent.

12.7 Timer flag

The timer flag (bit TF) is set logic 1 on the first trigger of MI, HMI, or the countdown timer. The purpose of the flag is to allow the controlling system to interrogate what caused the interrupt: timer or alarm. The flag can be read and cleared by command.

The status of the timer flag TF can affect the INT pulse generation depending on the setting of TI_TP

12.7.1 When TI_TP is set logic 1.

An INT pulse is generated independent of the status of the timer flag TF.
TF stays set until it is cleared.

TF does not affect INT.
Tiny Real-Time Clock/calendar with alarm function and I2C-bus.
The countdown timer runs in a repetitive loop and keeps generating timed periods.

12.7.2 When TI_TP is set logic 0

The INT generation follows the TF flag.
TF stays set until it is cleared.
If TF is not cleared before the next coming interrupt, no INT is generated.
The countdown timer stops after the first countdown.

12.7.3 COF[2:0]: Clock output frequency

A programmable square wave is available at pin CLKOUT. Operation is controlled by the COF[2:0] bits in the register Control_2. Frequencies of 32.768 kHz (default) down to 1 Hz can be generated for use as a system clock, microcontroller clock, input to a charge pump, or for calibration of the oscillator.

Pin CLKOUT is a push-pull output and enabled at power-on. CLKOUT can be disabled by setting

COF[2:0] to 111 or by setting CLKOE LOW (TDFN 2.6x2.6-10L only). When disabled, the CLKOUT is LOW. If CLKOE is HIGH and COF[2:0]=111 there will be no clock and CLKOUT will be LOW.

The duty cycle of the selected clock is not controlled. However, due to the nature of the clock generation, all clock frequencies except 32.768 kHz have a duty cycle of 50 : 50.

The STOP bit function can also affect the CLKOUT signal, depending on the selected frequency. When the STOP bit is set logic 1, the CLKOUT pin generates a continuous LOW for those frequencies that can be stopped

COF[2:0]	CLKOUT frequency (Hz)	Typical duty cycle[1]	Effect of STOP bit
000[2]	32768	60 : 40 to 40 : 60	no effect
001	16384	50 : 50	no effect
010	8192	50 : 50	no effect
011	4096	50 : 50	CLKOUT = LOW
100	2048	50 : 50	CLKOUT = LOW

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101	1024	50 : 50	CLKOUT = LOW
110	1[3]	50 : 50	CLKOUT = LOW
111	CLKOUT = LOW	_	_

Note:

[1] Duty cycle definition: % HIGH-level time: % LOW-level time.

[2] Default values: The duty cycle of the CLKOUT when outputting 32,768 Hz could change from 60:40 to 40:60 depending on the detector since the 32,768 Hz is derived from the oscillator output which is not perfect. It could change from device to device and it depends on the silicon diffusion. There is nothing that can be done from outside the chip to influence the duty cycle.

[3] 1 Hz clock pulses are affected by offset correction pulses.

12.8 Offset (0X02)

The FRTC85063 incorporates an offset register (address 02h) which can be used to implement several functions, such as:

1. Accuracy tuning
2. Aging adjustment
3. Temperature compensation

Bit	Symbol	Default value	Description
7	MODE	0	**offset mode** 0=normal mode: offset is made once every two hours 1=course mode: offset is made every 4 minutes
6 to 0	OFFSET [6:0]		**offset value**

For MODE = 0, each LSB introduces an offset of 4.34 ppm. For MODE = 1, each LSB introduces an offset of 4.069 ppm. The offset value is coded in two's complement giving a range of +63 LSB to -64 LSB.

OFFSET [6:0]	Offset value in decimal	Offset value in ppm	
		Normal mode MODE = 0	Fast mode MODE = 1
0111111	+63	+273.420	+256.347
0111110	+62	+269.080	+252.278
:	:	:	:
0000010	+2	+8.680	+8.138
0000001	+1	+4.340	+4.069
0000000[1]	0	0 [1]	0 [1]
1111111	-1	-4.340	-4.069
1111110	-2	-8.680	-8.138
:	:	:	:
1000001	-63	-273.420	-256.347
1000000	-64	-277.760	-260.416

Note:

[1] Default value.

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Correction is achieved through the addition or subtraction of clock adjustment pulses, which effectively alters the duration of an individual second. This method operates on the time-base division chain rather than modifying the oscillator's natural frequency.

The application of correction pulses can be externally monitored. To enable interrupt generation associated with this function, the CIE bit (located in Control_1) must be set to logic 1. During each correction cycle, a pulse is output on the INT pin. The width of this output pulse is determined by the selected correction mode.

12.8.1 Correction when MODE = 0

The correction is triggered once every two hours and then correction pulses are applied once per minute until the programmed correction values have been implemented。

Correction value	Update every nth hour	Minute	Correction pulses on INT per minute[1]
+1 or -1	2	00	1
+2 or -2	2	00 and 01	1
+3 or -3	2	00, 01, and 02	1
:	:	:	:
+59 or -59	2	00 to 58	1
+60 or -60	2	00 to 59	1
+61 or -61	2	00 to 59	1
	2nd and next hour	00	1
+62 or -62	2	00 to 59	1
	2nd and next hour	00 and 01	1
+63 or -63	02	00 to 59	1
	2nd and next hour	00, 01, and 02	1
-64	02	00 to 59	1
	2nd and next hour	00, 01, 02, and 03	1

Note:

The correction pulses on pin INT are $\frac{1}{64}$ s wide.

In MODE = 0, any timer or clock output using a frequency below 64 Hz is affected by the clock correction

Frequency (Hz)	Effect of correction
CLKOUT	
32768	no effect
16384	no effect
8192	no effect
4096	no effect
2048	no effect
1024	no effect
1	affected
Timer source clock	
4096	no effect
64	no effect
1	affected
$\frac{1}{60}$	affected

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12.8.2 Correction when MODE = 1

The correction is triggered once every four minutes and then correction pulses are applied once per second up to a maximum of 60 pulses. When correction values greater than 60 pulses are used, additional correction pulses are made in the 59th second.

Clock correction is made more frequently in MODE = 1; however, this can result in higher power consumption.

Correction value	Update every n^{th} minute	Second	Correction pulses on INT per second[1]
+1 or −1	2	00	1
+2 or −2	2	00 and 01	1
+3 or −3	2	00, 01, and 02	1
:	:	:	:
+59 or −59	2	00 to 58	1
+60 or −60	2	00 to 59	1
+61 or −61	2	00 to 58	1
	2	59	2
+62 or −62	2	00 to 58	1
	2	59	3
+63 or −63	2	00 to 58	1
	2	59	4
−64	2	00 to 58	1
	2	59	5

Note:
The correction pulses on pin INT are 1/1024 s wide. For multiple pulses, they are repeated at an interval of 1/512 s.

In MODE = 1, any timer source clock using a frequency below 1.024 kHz is also affected by the clock correction

Frequency (Hz)	Effect of correction
CLKOUT	
32768	no effect
16384	no effect
8192	no effect
4096	no effect
2048	no effect
1024	no effect
1	affected
Timer source clock	
4096	no effect
64	affected
1	affected
1/60	affected

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12.9 Offset calibration workflow

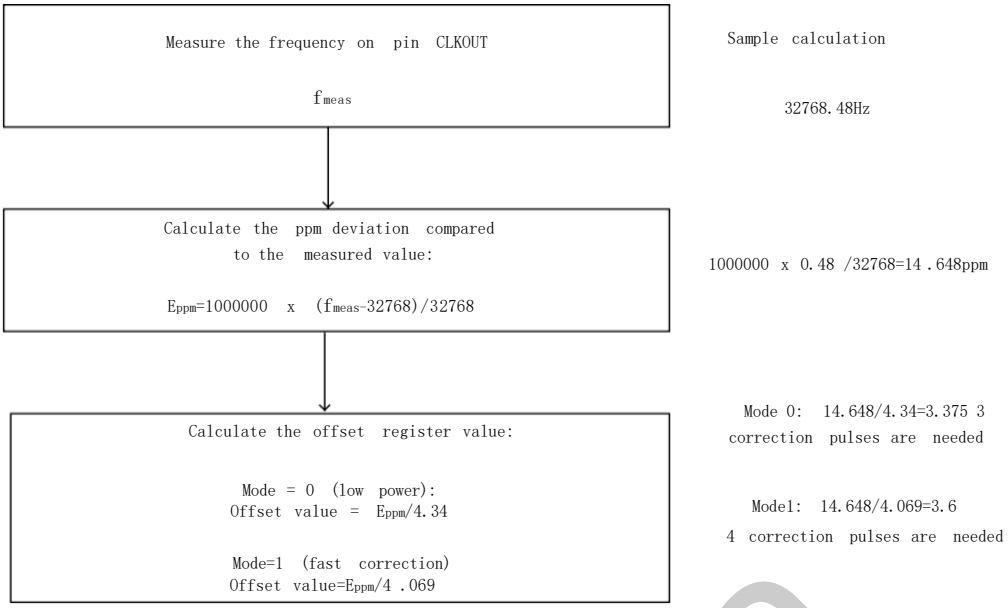


Figure5 Offset calibration calculation workflow

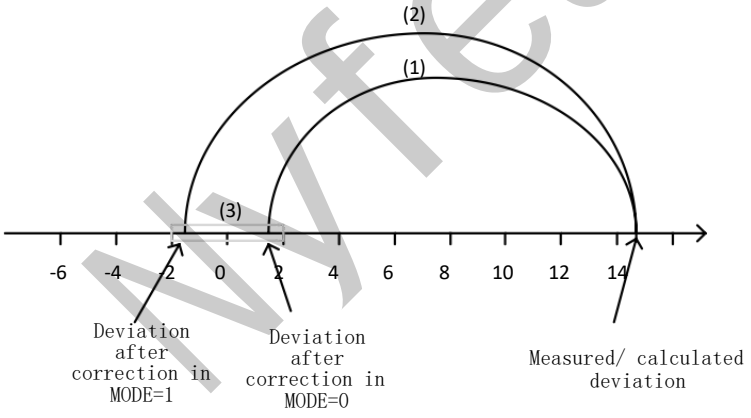


Figure6 Result of offset calibration

With the offset calibration an accuracy of ±2 ppm (0.5 x offset per LSB) can be reached ±1ppm corresponds to a time deviation of 0.0864 seconds per day.

(1) 3 correction pulses in MODE = 0 correspond to -13.02 ppm.

(2) 4 correction pulses in MODE = 1 correspond to -16.276 ppm.

(3) Reachable accuracy zone.

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12.9.1 RAM_byte Register(0x03)

The FRTC85063 provides a free RAM byte, which can be used for any purpose, for example, status byte of the system.

Bit	Symbol	Value	Description
7 to 0	B[7:0]	00000000[1] to 11111111	**RAM content**

Note:
[1] Default value.

12.9.2 Seconds Register(0x04)

Bit	Symbol	Value	Place value	Description
7	OS	[1] 1	_	**Oscillator flag** 0=clock integrity is guaranteed 1=clock integrity is not guaranteed; oscillator has stopped or has been interrupted
6 to4	SECONDS	0[1] to 5	ten’s place	actual seconds coded in BCD format
3 to 0		0[1] to 9	unit place	

Note:
[1] Default value.

12.9.3 Minutes Register(0x05)

Bit	Symbol	Default Value	Place value	Description
7	_	0	_	unused
6 to4	MINUTES	0	ten’s place	**actual minutes** coded in BCD format
3 to 0		0	unit place	

12.9.4 Hours Register(0x06)

Bit	Symbol	Default Value	Place value	Description
7 to 6	_	00	_	unused
12-hour mode[1]				
5	AMPM	0	_	**AM/PM indicator** 0=AM 1=PM
4	HOURS	0	ten’s place	**actual hours in 12-hour mode** coded in BCD format
3 to0		0	unit place	
24-hour mode[1]				
5 to 4	HOURS	0	ten’s place	**actual hours in 24-hour mode** coded in BCD format
3 to0		0	unit place	

Note:
[1] Hour mode is set by the 12_24 bit in register Control_1

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12.9.5 Days Register(0x07)

Bit	Symbol	Default Value	Place value	Description
7 to 6	_	00	_	unused
5 to4	DAYS[1]	0	ten's place	**actual day** coded in BCD format
3 to0		0	unit place	

Notes:
[1] If the year counter contains a value, which is exactly divisible by 4 (including the year 00), the FRTC85063 compensates for leap years by adding a 29th day to February.

12.9.6 Weekdays Register(0x08)

Bit	Symbol	Value	Description
7 to 3	_	00000	unused
2 to0	WEEKDAYS	0 to 6	**actual weekday** values

Day[1]	Bit		
	2	1	0
Sunday	0	0	0
Monday	0	0	1
Tuesday	0	1	0
Wednesday	0	1	1
Thursday	1	0	0
Friday	1	0	1
Saturday[2]	1	1	0

Notes:
[1] Definition may be reassigned by the user.
[2] Default value

12.9.7 Months Register(0x09)

Bit	Symbol	Value	Place value	Description
7 to 5	_	000	_	unused
4	MONTHS	0 to 1	ten's place	**actual month** coded in BCD forma
3 to 0		0 to 9	unit place	

Month	Upper-digit (ten's place)	Digit (unit place)			
	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
January[1]	0	0	0	0	1
February	0	0	0	1	0
March	0	0	0	1	1
April	0	0	1	0	0
May	0	0	1	0	1
June	0	0	1	1	0

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July	0	0	1	1	1
August	0	1	0	0	0
September	0	1	0	0	1
October	1	0	0	0	0
November	1	0	0	0	1
December	1	0	0	1	0

Note:
[1] Default value.

12.9.8 Years Register(0x0A)

Bit	Symbol	Value	Place value	Description
7 to 4	YEARS	0[1] to 9	ten's place	**actual year** coded in BCD format
3 to0		0[1] to 9	unit place	

Note:
[1] Default value.

12.10 Setting and reading the time

The data flow and data dependencies starting from the 1 Hz clock tick

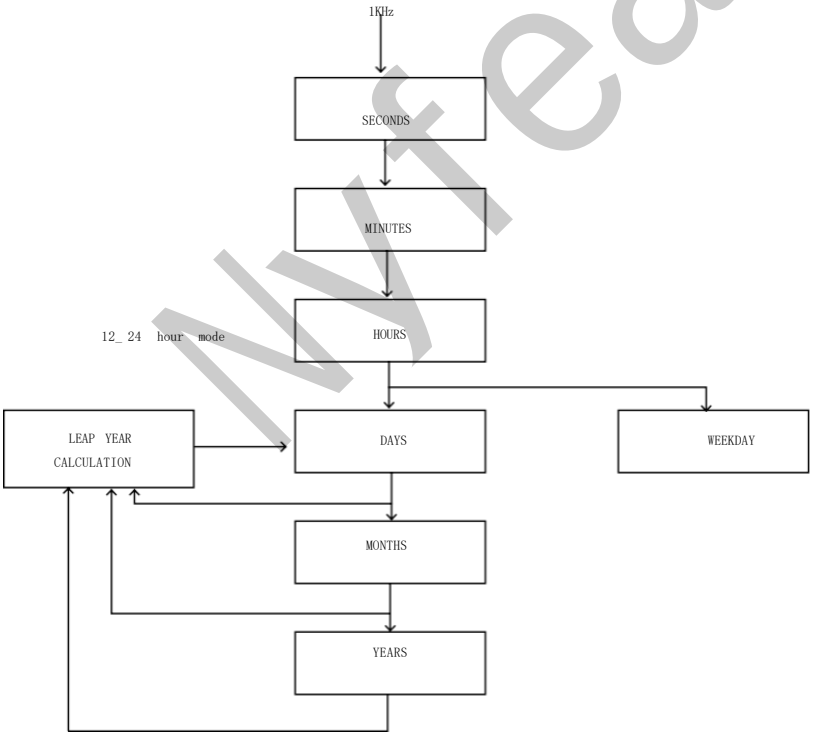


Figure7 Data flow for the time function

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Upon completion of the read or write operation, the timekeeping circuitry is released from its frozen state. Any increment request that was pending during the access window will then be serviced. The device can buffer a maximum of one such request; consequently, all read/write accesses must be concluded within a 1-second timeframe to prevent loss of pending increment events.Setting or reading seconds through to years should be made in one single access.Failing to comply with this method could result in the time becoming corrupted.

12.10.1 Second_alarm Register(0x0B)

Bit	Symbol	Default Value	Place value	Description
7	AEN_S	1	-	**second alarm** 0=enabled 1=disabled
6 to 4	SECOND_ALARM	0	ten's place	**second alarm information** coded in BCD format
3 to 0		0	unit place	

12.10.2 Minute_alarm Register(0x0C)

Bit	Symbol	Default Value	Place value	Description
7	AEN__M	1	-	**minute alarm** 0=enabled 1=disabled
6 to 4	MINUTE_ALARM	0	ten's place	**minute alarm information** coded in BCD format
3 to 0		0	unit place	

Note:
[1] Default value.

12.10.3 Hour_alarm Register(0x0D)

Bit	Symbol	Value	Place value	Description
7	AEN__H	1[1]	-	**hour alarm** 0=enabled 1=disabled
6	-	0[1]	-	unused
12-hour mode[2]				
5	AMPM	0[1]	-	**AM/PM indicator** 0=AM 1=PM
4	HOUR_ALARM	0[1] to 1	ten's place	**hour alarm information in 12-hour mode** coded in BCD format
3 to0		0[1] to 9	unit place	
24-hour mode[2]				
5 to 4	HOUR_ALARM	0[1] to 2	ten's place	**hour alarm information in 24-hour mode** coded in BCD format
3 to0		0[1] to 9	unit place	

Note:
[1] Default value.
[2] Hour mode is set by the 12_24 bit in register Control_1

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12.10.4 Day_alarm Register(0x0E)

Bit	Symbol	Value	Place value	Description
7	AEN__D	1[1]		**day alarm** 0=enabled 1=disabled
6	_	0	_	unused
5 to 4	DAY_ALARM	0[1] to 3	ten's place	**day alarm information** coded in BCD format
3 to 0		0[1] to 9	unit place	

Note:
[1] Default value.

12.10.5 Weekday_alarm Register(0x0F)

Bit	Symbol	Value	Description
7	AEN__W	1[1]	**weekday alarm** 0=enabled 1=disabled
6 to 3	_	0	unused
2 to 0	WEEKDAY_ALARM	0[1] to 6	**weekday alarm information** coded in BCD format

Note:
[1] Default value.

12.11 Alarm function

By clearing the alarm enable bit (AEN_x) in any of the alarm registers, the corresponding alarm condition becomes active and is monitored for a match. When a match occurs (i.e., the alarm triggers), the alarm flag AF is set to logic 1. The asserted AF flag can then be utilized to drive an interrupt output (INT) if the
interrupt function is enabled. The AF flag remains set until explicitly cleared via a software command.

The registers at addresses 0Bh through 0Fh contain alarm information. When one or more of these registers is loaded with second, minute, hour, day or weekday, and its corresponding AEN_x is logic 0, then that information is compared with the current second, minute, hour, day, and weekday. When all enabled comparisons first match, the alarm flag (AF in register Control_2) is set logic 1.

The generation of interrupts from the alarm function is controlled via bit AIE. If bit AIE is enabled, the INT pin follows the condition of bit AF. AF remains set until cleared by command. Once AF has been cleared, it will only be set again when the time increments to match the alarm condition once more. Alarm
registers which have their AEN_x bit at logic 1 are ignored.

12.11.1 Timer_value Register(0x10/0x12)

Bit	Symbol	Value	Description
7 to0	T [7:0]	0h[1] to FFh	**countdown timer value**[2]
7 to0	T [15:8]	1FFhto FFFFh	_

Note:
[1] Default value.
[2] Countdown period in seconds: *CountdownPeriod=T/SourceClockFrequency* where T is the countdown value.

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12.11.2 Timer_mode Register (0x11)

Bit	Symbol	Default Value	Description
7 to 5	_	000	unused
4 to 3	TCF[1:0]	11	**timer clock frequency** 00=4.096 kHz timer source clock 01=64 Hz timer source clock 10=1 Hz timer source clock 11=1/60 Hz timer source clock
2	TE	0	**timer enable** 0=timer is disabled 1=timer is enabled
1	TIE	0	**timer interrupt enable** 0=no interrupt generated from timer 1=interrupt generated from timer
0	TI__TP	0	**timer interrupt mode** 0=interrupt follows timer flag 1=interrupt generates a pulse

12.12 Timer functions

The timer has four selectable source clocks allowing for countdown periods in the range from 244 ms to 4 hours 15 min(FRTC85063) .

FRTC85063:

TCF[1:0]	Timer source clock frequency[1]	Delay	
		Minimum timer duration T= 1	Maximum timer duration T= 255
00	4.096 kHz	244 us	62.256 ms
01	64 Hz	15.625 ms	3.984 s
10	1 Hz[2]	1 s	255 s
11	1/60 Hz[2]	60 s	4 hours 15 min

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Note:

[1] When not in use, TCF[1:0] must be set to 1/60 Hz for power saving.

[2] Time periods can be affected by correction pulses.

Remark: Note that all timings which are generated from the 32.768 kHz oscillator are based on the assumption that there is 0 ppm deviation. Deviation in oscillator frequency results in deviation in timings. This is not applicable to interface timing.

When the counter decrements from 1, the timer flag (bit TF in register Control_2) is set and the counter automatically re-loads and starts the next timer period.

If a new value of T is written before the end of the current timer period, then this value takes immediate effect. Does not recommend changing T without first disabling the counter by setting bit TE logic 0. The update of T is asynchronous to the timer clock.

Therefore changing it without setting bit TE logic 0 may result in a corrupted value loaded into the countdown counter. This results in an undetermined countdown period for the first period. The countdown value T will, however, be correctly stored and correctly loaded on subsequent timer periods. When starting the timer for the first time, the first period has an uncertainty. The uncertainty is a result of the enable instruction being generated from the interface clock which is asynchronous from the timer
source clock. Subsequent timer periods do not have such delay. The amount of delay for the first timer period depends on the chosen source clock.

Timer source clock	Minimum timer period	Maximum timer period
4.096 kHz	T	T+1
64 Hz	T	T+1
1 Hz	$(T-1)+\frac{1}{64Hz}$	$T+\frac{1}{64Hz}$
1/60 Hz	$(T-1)+\frac{1}{64Hz}$	$T+\frac{1}{64Hz}$

At the end of every countdown, the timer sets the countdown timer flag (bit TF in register Control_2). Bit TF can only be cleared by command. The asserted bit TF can be used to generate an interrupt at pin INT. The interrupt may be generated as a pulsed signal every countdown period or as a permanently
active signal which follows the condition of bit TF. Bit TI_TP is used to control this mode selection and the interrupt output may be disabled with bit TIE.

When reading the timer, the current countdown value is returned and not the initial value T. Since it is not possible to freeze the countdown timer counter during read back, it is recommended to read the register twice and check for consistent results.

Timer source clock frequency selection of 1 Hz and 1⁄60 Hz is affected by the Offset register. The duration of a program period varies according to when the offset is initiated. For example, if a 100 s timer is set using the 1 Hz clock as source, then some 100 s periods will contain correction pulses and
therefore be longer or shorter depending on the setting of the Offset register.

12.12.1 Countdown timer interrupts

The pulse generator for the countdown timer interrupt uses an internal clock and is dependent on the selected source clock for the countdown timer and on the countdown value T. As a consequence, the width of the interrupt pulse varies.

Source clock (Hz)	INT period (s)	
	T= 1 [1]	T> 1 [1]
4096	1/8192	1/4096
64	1/128	1/64
1	1/64	1/64
1/60	1/64	1/64

Note:
T = loaded countdown value. Timer stops when T = 0.

13 IIC Bus Interface

This bus is intended for communication between different ICs. It consists of two lines: one bidirectional for data signals (SDA) and one for clock signals (SCL). Both the SDA and the SCL lines must be pulled up via a pull-up resistors.

The following protocol has been defined:

Data transfer may be initiated only when the bus is not busy.

- During data transfer, the data line must remain stable whenever the clock line is high.
- Changes in the data line while the clock line is high will be interpreted as

control signals. Accordingly, the following bus conditions have been defined:

13.1 Bus not busy

Both data and clock lines remain high.

13.2 Start data transfer

A change in the state of the data line, from high to low, while the clock is high, defines the START condition.

13.3 Stop data transfer

A change in the state of the data line, from low to high, while the clock is high, defines the STOP condition.

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13.4 Data valid

The state of the data line represents valid data when after a start condition, the data line is stable for the duration of the high period of the clock signal. The data on the line may be changed during the low period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a start condition and terminated with a stop condition. The number of data bytes transferred between the start and stop conditions is not limited. The information is transmitted byte-wide and each receiver acknowledges with a ninth bit.

13.5 Acknowledge

Each byte of eight bits is followed by one acknowledge bit. This acknowledge bit is a low level put on the bus by the receiver, whereas the master generates an extra acknowledge related clock pulse.

A slave receiver which is addressed is obliged to generate an acknowledge after the reception of each byte. Also, a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is a stable low during the high period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master receiver must signal an end-of-data to the slave transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this case, the transmitter must leave the data line high to enable the master to generate the STOP condition.

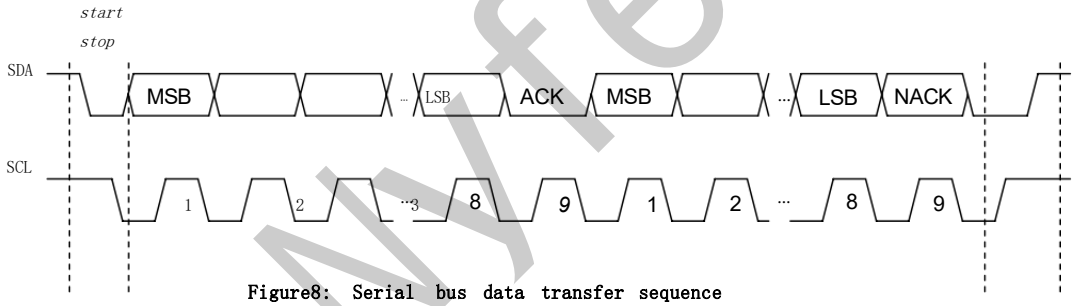


Figure8: Serial bus data transfer sequence

13.6 Read mode

In this mode, the master reads the FRTC85063 slave after setting the slave address Following the write mode control bit (R/W = 0) and the acknowledge bit, the word address An is written to the on-chip

address pointer. Next the START condition and slave address are repeated, followed by the READ mode control bit (R/W = 1). At this point, the master transmitter becomes the master receiver. The data byte which was addressed will be transmitted and the master receiver will send an acknowledge bit to the slave transmitter. The address pointer is only incremented on reception of an acknowledge bit.

The FRTC85063 slave transmitter will place the data byte at address An + 1 on the bus. The master receiver reads and acknowledges the new byte and the address pointer is incremented to An + 2. This cycle of reading consecutive addresses will continue until the master receiver sends a STOP condition to the slave transmitter.

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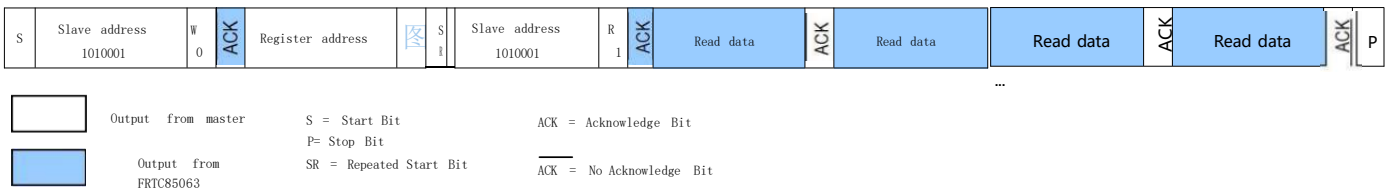


Figure9 Read Mode Sequence

13.7 Write mode

In this mode the master transmitter transmits to the FRTC85063 slave receiver. Following the START condition and slave address, a logic '0' (R/W = 0) is placed on the bus and indicates to the addressed device that word address An will follow and is to be written to the on-chip address pointer. The data word to be written to the memory is strobed in next and the internal address pointer is incremented to the next memory location within the RAM on the reception of an acknowledge clock. The FRTC85063 slave receiver will send an acknowledge clock to the master transmitter after it has received the slave address and again after it has received the word address and each data byte.

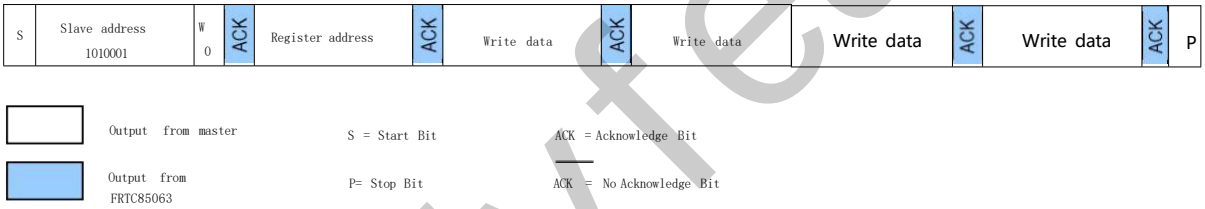


Figure10 Write Mode Sequence

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14 Limiting values

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		-0.5	+6.5	V
I_{DD}	supply current		-50	+50	mA
V_I	input voltage	on pins SCL, SDA, OSCI, CLKOE	-0.5	+6.5	V
V_O	output voltage		-0.5	+6.5	V
I_I	input current	at any input	-10	+10	mA
I_O	output current	at any output	-10	+10	mA
P_{tot}	total power dissipation		_	300	mW
V_{ESD}	electrostatic discharge voltage	HBM	_	±5000	V
		CDM			
		FRTC85063Q	_	±1750	V
		FRTC85063S	_	±2000	V
		FRTC85063M	_	±2000	V
I_{lu}	latch-up current		_	200	mA
T_{stg}	storage temperature		-65	+150	° C
T_{amb}	ambient temperature	operating device	-40	+85	° C

Note:

The FRTC85063 part is not guaranteed (nor characterized) above the operating range as denoted in the datasheet. Recommends not to bias the FRTC85063 device during reflow (e.g. if utilizing a 'coin' type battery in the assembly). If customer so chooses to continue to use this assembly method, there must be the allowance for a full `0 V' level Power supply `reset' to re- enable the device. Without a proper POR, the device may remain in an indeterminate state.

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15 DC Electrical Characteristics

VDD = 1.1 V to 5.5 V; GND = 0 V; Tamb = -40 ° C to +85 ° C; fosc = 32.768 kHz; unless otherwise specified.

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
Supplies						
V_{DD}	supply voltage	interface inactive; f_{SCL} =0 Hz[1]	1.1	_	5.5	V
		interface active; f_{SCL} = 400 kHz[2]	1.8	_	5.5	V
I_{DD}	supply current	CLKOUT disabled; V_{DD} = 3.3 V, f_{SCL} =0 Hz [3]				
		T_{amb} = 25 ° C	_	220	450	nA
		T_{amb} = 50 ° C[4]	_	250	500	nA
		T_{amb} = 85 ° C	_	470	600	nA
		interface active; f_{SCL} = 400 kHz	_	18	50	uA
Inputs[5]						
V_I	input voltage		-0.5	_	+5.5	V
V_{IL}	LOW-level input voltage		-0.5	_	+0.3V_{DD}	V
V_{IH}	HIGH-level input voltage		0.7V_{DD}	_	5.5	V
I_{LI}	input leakage current	V_I = GNDor V_{DD}	_	0	_	mA
		post ESD event	-0.15	_	+0.15	mA
C_i	input capacitance[6]		_	_	7	pF
Outputs						
V_{OH}	HIGH-level output voltage	on pin CLKOUT	0.8V_{DD}	_	V_{DD}	V
V_{OL}	LOW-level output voltage	on pins SDA, INT, CLKOUT	V_{SS}	_	0.2V_{DD}	V
I_{OH}	HIGH-level output current	output source current; V_{OH} = 2.9 V; V_{DD} = 3.3 V; on pin CLKOUT	1	3	_	mA
I_{OL}	LOW-level output current	output sink current; V_{OL} = 0.4 V V_{DD} = 3.3 V				
		on pin SDA	3	8.5	_	mA
		on pin INT	2	6	_	mA
		on pin CLKOUT	1	3	_	mA

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16 Crystal electrical characteristics

VDD = 1.1 V to 5.5 V; VSS = 0 V; Tamb = -40 °C to +85 °C; fosc = 32.768 kHz; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Oscillator						
Df_{osc}/f_{osc}	relative oscillator frequency variation	DV_{DD} = 200 mV; T_{amb} = 25 °C	_	0.075	_	ppm
$C_{L(itg)}$	integrated load capacitance	C_L = 7 pF	4.2	7	9.8	pF
		C_L = 12.5 pF	7.5	12.5	17.5	pF
R_s	series resistance		_	_	100	k Ω

17 IIC AC Characteristics

VDD = 1.8 V to 5.5 V; GND =0 V; Tamb = -40 °C to +85 °C; fosc = 32.768 kHz; unless otherwise specified. All timing values are valid within the operating supply voltage and temperature range and referenced to VIL and VIH with an input voltage swing of GND to VDD

Symbol	Parameter	Min	Max	Unit
C_b	capacitive load for each bus line		400	pF
f_{SCL}	SCL clock frequency[1]	0	400	kHz
$t_{HD;STA}$	hold time (repeated) START condition	0.6	_	us
$t_{SU;STA}$	set-up time for a repeated START condition	0.6	_	us
t_{LOW}	LOW period of the SCL clock	1.3	_	us
t_{HIGH}	HIGH period of the SCL clock	0.6	_	us
t_r	rise time of both SDA and SCL signals	20	300	ns
t_f	fall time of both SDA and SCL signals[2]	20 ′(V_{DD} / 5.5 V)	300	ns
t_{BUF}	bus free time between a STOP and START condition	1.3	_	us
$t_{SU;DAT}$	data set-up time	100	_	ns
$t_{HD;DAT}$	data hold time	0	_	ns
$t_{SU;STO}$	set-up time for STOP condition	0.6	_	us
$t_{VD;DAT}$	data valid time	0	0.9	us
$t_{VD;ACK}$	data valid acknowledge time	0	0.9	us
t_{SP}	pulse width of spikes that must be suppressed by the input filter	0	50	ns

Note:

[1]I2C-bus access time between two STARTs or between a START and a STOP condition to this device must be less than one second.

[2] A device must internally provide a hold time of at least 300 ns for the SDA signal (with respect to the VIH(min) of the SCL signal) to bridge the undefined region of the falling edge of SCL.The maximum tf for the SDA and SCL bus lines is specified at

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300 ns. The maximum fall time for the SDA output stage tf is specified at 250 ns. This allows series protection resistors to be connected in between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified tf.

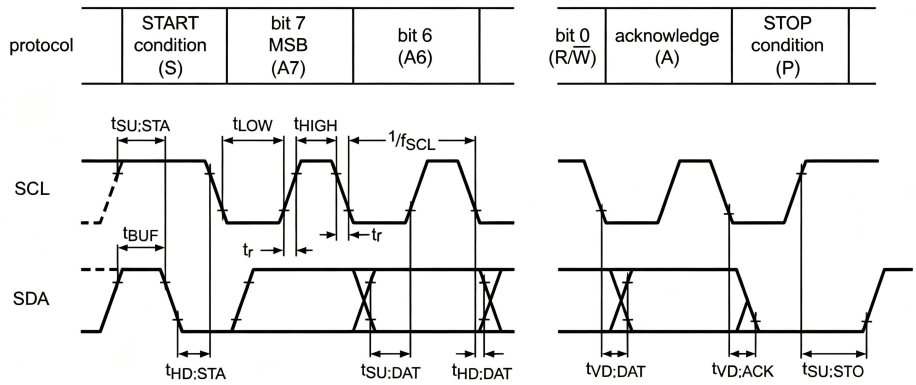


Figure11 I2C-bus timing diagram; rise and fall times refer to 30 % and 70 %

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18 Handing information

The I/O pins on this device are equipped with integrated ESD protection structures to withstand typical handling conditions. However, as this is a MOS-type component, proper ESD control measures must be strictly observed throughout all handling, assembly, and testing processes. Refer to JESD625-A, IEC 61340-5, or locally applicable electrostatic discharge standards for detailed procedural requirements.

19 Introducing to soldering

Soldering remains one of the primary techniques for mounting IC packages onto Printed Circuit Boards (PCBs) to establish functional electrical interconnections. A properly formed solder joint fulfills both
mechanical anchoring and electrical continuity roles. No universal soldering approach suits every IC package type. Wave soldering is frequently selected for mixed-technology boards that combine through-hole components with Surface Mount Devices (SMDs); however, this method proves less effective for fine-pitch SMD configurations. For applications demanding tight pitches and high component densities—characteristics of modern miniaturized designs—reflow soldering offers a more appropriate solution.

20 Wave and reflow solding

Wave soldering employs a circulating fountain of molten solder to form interconnections between components and the board. This technique is applicable to the following component types:

- Through-hole devices
- Leaded or leadless SMDs that have been temporarily affixed to the PCB surface with adhesive

However, wave soldering is not universally compatible with all SMD types. Components featuring solder-ball terminations, as well as certain leadless packages with contact lands situated beneath the package body, are unsuitable for this process. Additionally, leaded SMDs with lead pitches below approximately 0.6 mm are prone to solder bridging and should not be processed via wave soldering.
Reflow soldering, by contrast, begins with the deposition of solder paste onto the board, followed by component placement and subsequent thermal profiling to reflow the solder. This method is compatible with leaded packages, ball-grid array devices, and leadless package configurations alike.
Critical parameters that influence both wave and reflow processes include:

- PCB characteristics, such as surface finish, solder mask application, and via design
- Land pattern geometry, incorporating solder-dam features and component orientation
- Package moisture sensitivity level (MSL) ratings
- Inspection and repair
- Lead-free soldering versus SnPb soldering

21 Wave soldering

Several key factors must be controlled to achieve reliable wave soldering results:

- Process-related considerations – including adhesive and flux application methods, lead trimming or clinching procedures, conveyor speed and board handling dynamics, solder wave height and flow characteristics, as well as the dwell time during which assemblies are exposed to the molten wave.

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• Solder bath conditions – encompassing bath temperature setpoints and control, along with monitoring and management of metallic contamination and impurity levels within the solder alloy.

22 Reflow soldering

Several essential factors must be considered to ensure a successful reflow soldering process:

• Solder alloy selection – The choice between lead-free and SnPb solders significantly impacts the thermal profile. It should be noted that lead-free processing typically demands higher minimum peak temperatures relative to SnPb alternatives, which consequently narrows the available operating window for the process.

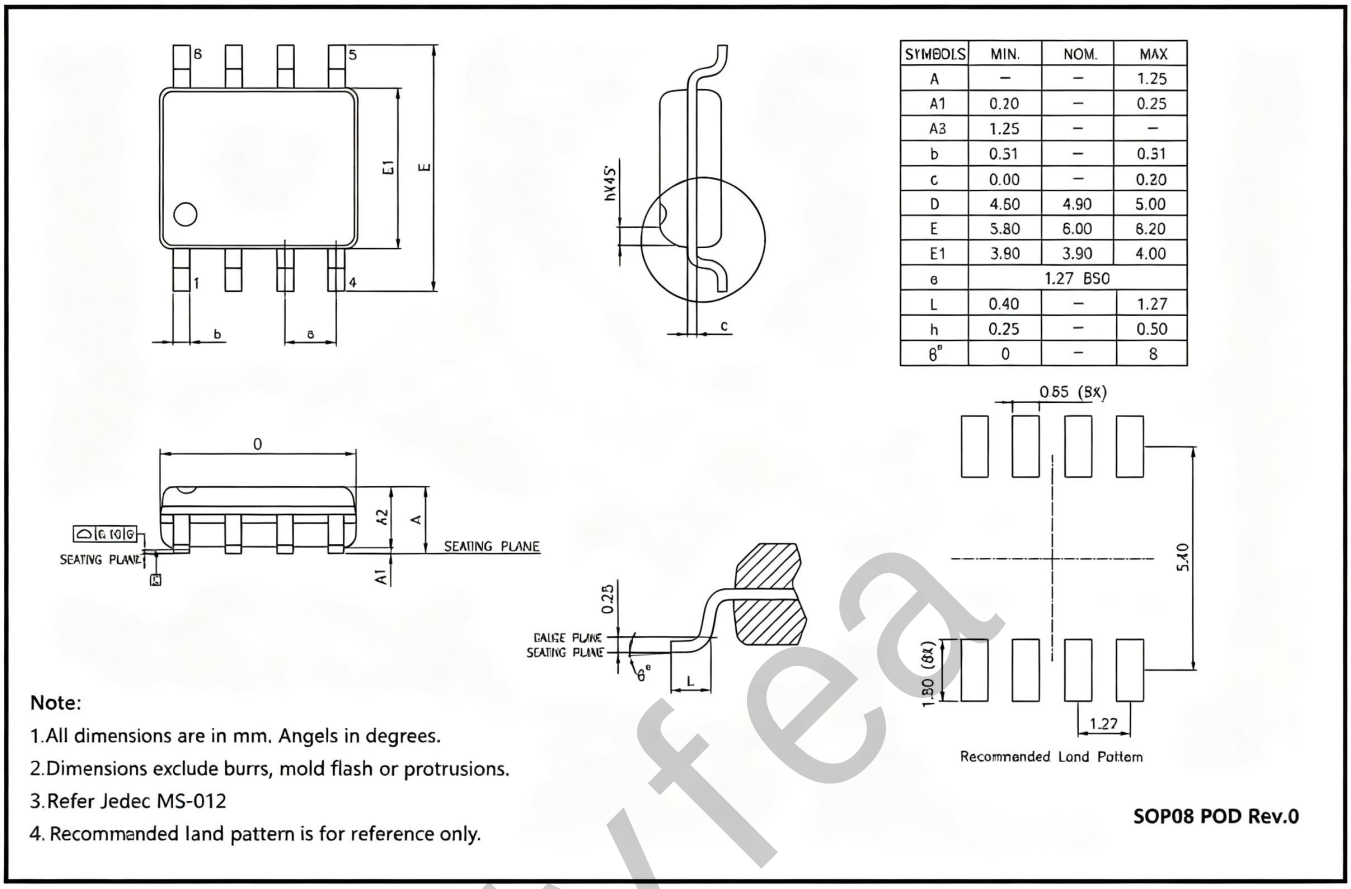
• Solder paste deposition quality – Key challenges include paste smearing during stencil printing, proper release characteristics from the aperture, and tuning of the process window to accommodate boards
populated with a diverse mix of large and small components simultaneously.

• Thermal profile management – The reflow temperature curve consists of several distinct zones: preheating, soak, reflow (where the assembly reaches its peak temperature), and cooling. Achieving reliable solder joint formation requires that the peak temperature meets or exceeds the minimum threshold dictated by the solder paste's metallurgical properties. At the same time, the peak temperature must
remain below the maximum safe limit for both the packages and the PCB substrate to prevent thermal damage. The appropriate peak temperature for a given package is determined by its physical dimensions—specifically, thickness and overall body volume.

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23 Package Information

23.1 SOP8



SYMBOLS	MIN.	NOM.	MAX
A	–	–	1.25
A1	0.20	–	0.25
A3	1.25	–	–
b	0.51	–	0.31
c	0.00	–	0.20
D	4.50	4.90	5.00
E	5.80	6.00	6.20
E1	3.90	3.90	4.00
e		1.27 BSC	
L	0.40	–	1.27
h	0.25	–	0.50
θ°	0	–	8

Note:

1.All dimensions are in mm. Angels in degrees.

2.Dimensions exclude burrs, mold flash or protrusions.

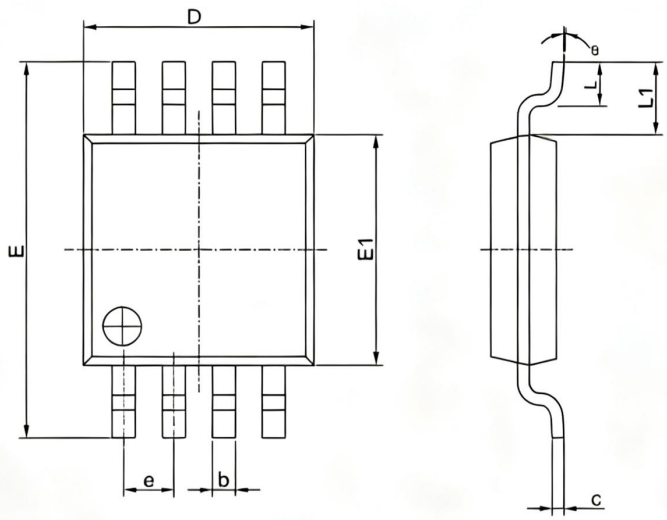
3.Refer Jedec MS-012

4. Recommanded land pattern is for reference only.

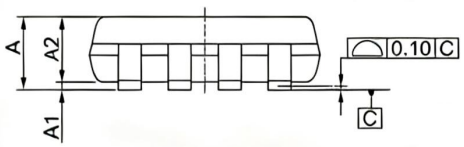
SOP08 POD Rev.0

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23.2 MSOP8



PKG DIMENSIONS(MM)		
SYMBOL	Min.	Max.
A	–	1.10
A1	0.00	0.15
A2	0.75	0.95
b	0.22	0.38
c	0.08	0.23
D	2.80	3.20
E	4.65	5.15
E1	2.80	3.20
e	0.65 BSC	
L	0.40	0.80
L1	0.95 REF	
θ	0°	8°



Note:

1.All dimensions are in mm. Angels in degrees.

2.Refer Jedec MO-187

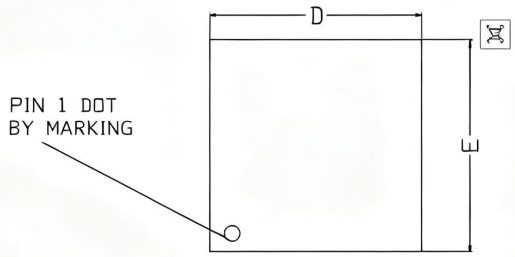
3.Dimensions exclude burrs, mold flash or protrusions.

MSOP08

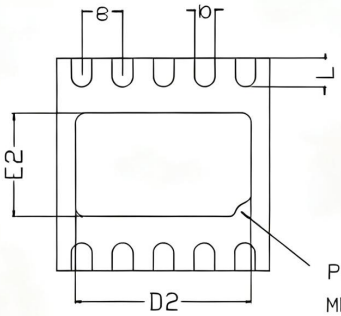
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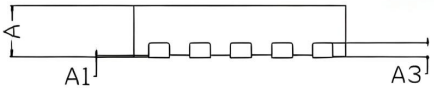
23.3 TDFN10



TOP VIEW



BOTTOM VIEW



SIDE VIEW

COMMON DIMENSIONS(MM)			
PKG. REF.	MIN.	NOM.	MAX
A	0.50	0.55	0.50
A1	0.00	–	0.05
A3		0.15 REF.	
D	2.55	2.60	2.65
E	2.55	2.60	2.65
D2	2.00	2.15	2.25
E2	1.11	1.25	1.30
b	0.20	0.25	0.30
L	0.25	0.35	0.45
e		0.5 BSC	

Note:

1. All dimensions are in mm. Angels in degrees.
2. Dimensions exclude burrs, mold flash or protrusions.
3. Refer Jedec MO-220

TDFN 2.6X2.6-10L (ZZ) POD Rev.0

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