钍地半导体
Tudi Semiconductor

Product Specification

TUDI-MAX515

10-BIT DIGITAL-TO-ANALOG CONVERTERS

网址 www.sztdbdt.com

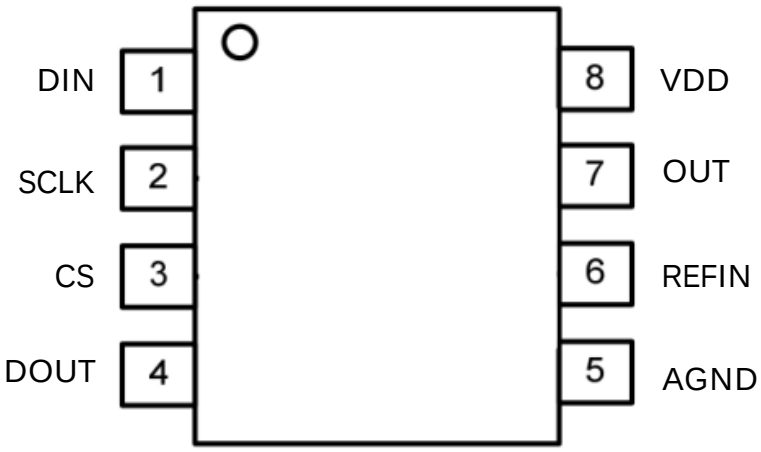
用芯智造·卓越品质

semiconductor device manufacturer

- Design
- research and development
- production
- and sales

Features

- 5V Single Supply Operation
- 3-Wire Serial Interface
- High-Impedance Reference Inputs
- Internal Power-On Reset
- Low Power Consumption: 1.75mW Max
- Update Rate of 1.21MHz
- Settling Time to 0.5LSB: 12.5μs Typ
- Monotonic Over Temperature
- 10-Bit CMOS Voltage Output DAC in an8-Terminal Package
- Voltage Output Range: 2 Times the Reference Input Voltage



Description

The MAX515 is a 10-bit voltage output digital-to-analog converter (DAC) with a buffered reference input (high impedance). The DAC has an output voltage range that is two times the reference voltage, and the DAC is monotonic. The device is simple to use, running from a single supply of 5V. A power-on-reset function is incorporated to ensure repeatable start-up conditions.

Digital control of the MAX515 is over a three-wire serial bus that is CMOS compatible and easily interfaced to industry standard microprocessor and microcontroller devices. The device receives a 16-bit data word to produce the analog output. The digital inputs feature Schmitt triggers for high noise immunity. Digital communication protocols include the SPI ™, QSPI ™, and Microwire ™ standards.The 8-terminal small-outline D package allows digital control of analog functions in space-critical applications. The MAX515C is characterized for operation from 0°C to +70°C. The MAX515E is characterized for operation from –40°C to +85°C.

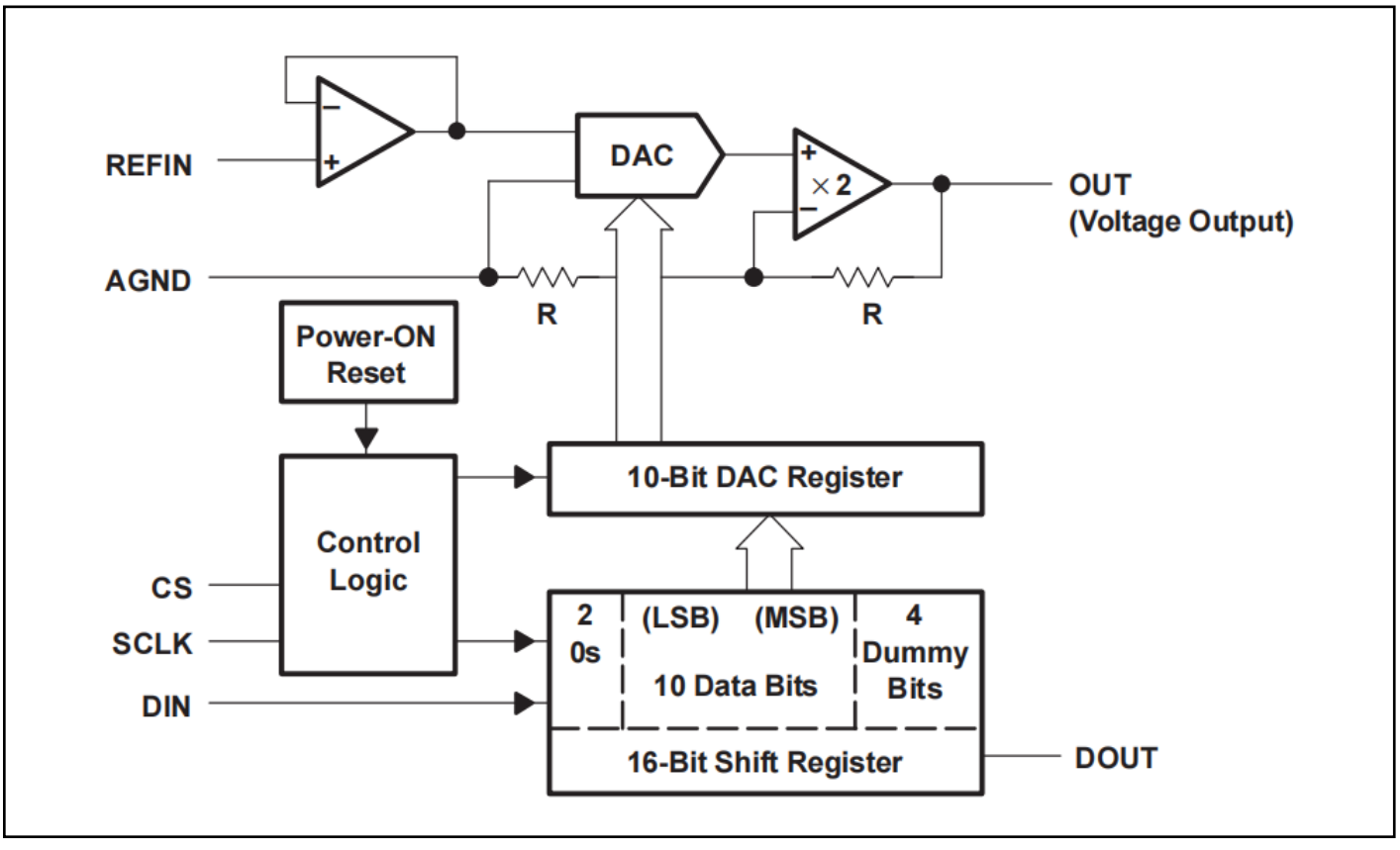
Applications

- Battery-Powered Test Instruments
- Digital Offset and Gain Adjustment
- Battery Operated/Remote Industrial Controls
- Machine and Motion Control Devices
- Cellular Telephones

Pin description

Name	No.	IV/O	Description
DIN	1	I	Serial data input
SCLK	2	I	Serial clock input
CS	3	I	Chip select,active low
DOUT	4	O	Serial data output for daisy chaining
AGND	5		Analog ground
REFIN	6	I	Reference input
OUT	7	O	DAC analog voltage output
VDD	8		Positive power supply

Functional block diagram



Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

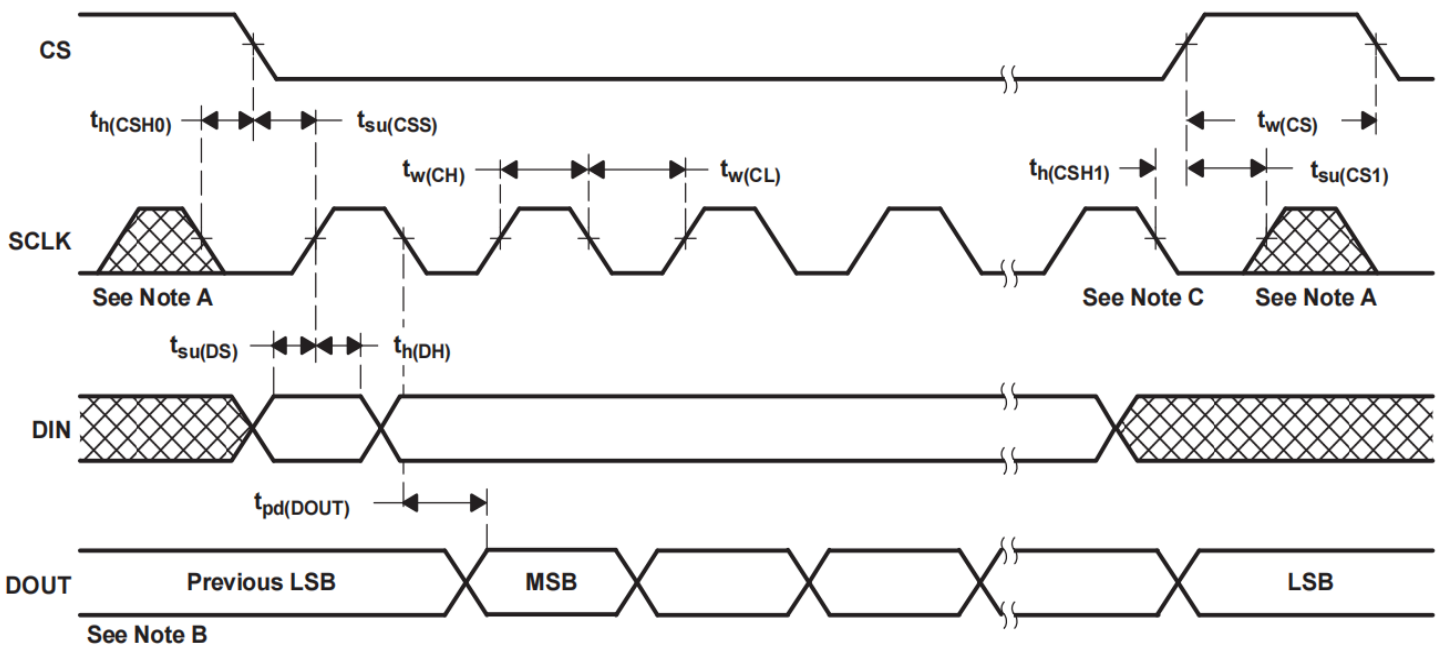
		UNIT
Supply voltage (VoD to AGND)		7V
Digital input voltage range to AGND		-0.3V to VDD+0.3V
Reference input voltage range to AGND		-0.3V to VDD+0.3V
Output voltage at OUT from external source		VDD+0.3V
Continuous current at any terminal		±20mA
Operating free-air temperature range,TA	MAX515C	0℃ to+70℃
	MAX515E	-40℃ to +85℃
Storage temperature range,Tstg		-65℃ to+150℃
Lead temperature 1,6mm(1/16 inch)from case for 10 seconds		+260℃

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Recommended Operating Conditions

		Min	Nom	Max	Unit
Supply voltage,VoD		4.5	5	5.5	V
High-level digital input voltage,VH		2.4			V
Low-level digital input voltage,VL				0.8	V
Reference voltage,Vref to REFIN terminal		2	2.048	VDD-2	V
Load resistance,RL		2			kΩ
Operating free-air temperature,TA	MAX515C	0		70	℃
	MAX515E	40		85	℃

Parameter Measurement Information



NOTES: A. The input clock, applied at the SCLK terminal, should be inhibited low when CS is high to minimize clock feedthrough.
B. Data input from preceeding conversion cycle.
C. Sixteenth SCLK falling edge

Figure 1. Timing Diagram

Digital Input Timing Requirements (See Figure 1)

Parameter		Min	Nom	Max	Unit
tsu(DS)	Setup time,DIN before SCLK high	45			ns
tn(DH)	Hold time,DIN valid after SCLK high	0			ns
tsu(CSS)	Setup time,CS low to SCLK high	1			ns
tsu(CS1)	Setup time,CS high to SCLK high	50			ns
tn(CSHO)	Hold time,SCLK low to CS low	1			ns
tn(CSH₁)	Hold time,SCLK low to CS high	0			ns
tw(CS)	Pulse duration,minimum chip select pulse width high	20			ns
tw(CL)	Pulse duration,SCLK low	25			ns
tw(CH)	Pulse duration,SCLK high	25			ns

Electrical Characteristics

over recommended operating free-air temperature range, V_{DD}= 5V ± 5%, V_{ref}= 2.048V (unless otherwise noted)

Static DAC specifications						
Parameter		**Test conditions**	**Min**	**Typ**	**Max**	**Unit**
Resolution			10			bits
Integral nonlinearity,end point adjusted (INL)		Vref=2.048V, See(1)			±1	LSB
Differential nonlinearity(DNL)		Vref=2.048V, See(2)		±0.1	±0.5	LSB
Ezs Zero-scale error (offset error at zero scale)		Vref=2.048V, See(3)			±3	LSB
Zero-scale-error temperature coefficient		Vref=2.048V, See(4)		3		ppm/°C
EG Gain error		Vref=2.048V, See (5)			±3	LSB
Gain-error temperature coefficient		Vref=2.048V, See(6)	80	1		ppm/℃
PSRR Power-supply rejection ratio	Zero scale	See(7)(8)	80			dB
	Gain					
Analog full scale output		RL=100kΩ	2Vref(1023/1024)			V

(1) The relative accuracy or integral nonlinearity (INL), sometimes referred to as linearity error, is the maximum deviation of the output from the line between zero and full scale excluding the effects of zero code and full-scale errors (see text). Tested from code 3 to code 1024.

(2) The differential nonlinearity (DNL), sometimes referred to as differential error, is the difference between the measured and ideal 1LSB amplitude change of any two adjacent codes. Monotonic means the output voltage changes in the same direction (or remains constant) as a change in the digital input code. Tested from code 3 to code 1024.(3) Zero-scale error is the deviation from zero-voltage output when the digital input code is zero (see text).

(4) Zero-scale-error temperature coefficient is given by: $E_{ZS}TC = [EZS(T_{max}) - E_{ZS}(T_{min})]/V_{ref} \times 10^6/(T_{max} - T_{min})$.

(5) Gain error is the deviation from the ideal output(V_{ref} − 1LSB) with an output load of 10kΩ excluding the effects of the zero-scale error.

(6) Gain temperature coefficient is given by: $E_GTC = [EG(T_{max}) - E_G(T_{min})]/V_{ref} \times 10^6/(T_{max} - T_{min})$.

(7) Zero-scale-error rejection ratio (EZS-RR) is measured by varying the$V_{DD}$from 4.5V to 5.5V dc and measuring the proportion of this signal imposed on the zero-code output voltage.

(8) Gain-error rejection ratio (EG-RR) is measured by varying the$V_{DD}$from 4.5V to 5.5V dc and measuring the proportion of this signal imposed on the full-scale output voltage after subtracting the zero-scale change.

Voltage Output (Out)

Parameter	Test conditions		Min	Typ	Max	Unit
Digital Output (DOUT)						
VoH Output voltage,high-level	Io=-2mA		VDD-1			V
VoL Output voltage,low-level	Io=2mA				0.4	V
Power Supply						
VDD Supply voltage			4.5	5	5.5	V
DD Power supply current	VDD=5.5V,No load, All inputs =0V or VDD	Vref=0		150	250	μA
	VDD=5.5V,No load, Allinputs =OV or VDD	Vref=2.048V		230	350	μA
Analog output dynamic performance						
Signal-to-noise +distortion,S/(N+D)	Vref=1Vpp at 1kHz+2.048Vdc, code=1111111111(1)			60		dB
Vo Voltage output range	RL=10kΩ		0		VDD-0.4	V
Output load regulation accuracy	Vo(oUT)=2V, RL=2kΩ				0.5	LSB
losc Output short circuit current	OUT to VoD or AGND			20		mA
VoLlow) Output voltage,low-level	lo(oUT≤5mA				0.25	V
VoH(high) Output voltage,high-level	lo(oUT≤-5mA		4.75			V
Reference Input						
VI Input voltage			0		VDD-2	V
ri Input resistance			10			MQ
Ci Input capacitance				5		pF
Digital Input (DIN, SCLK, CS)						
VIH High-level digital input voltage			2.4			V
VIL Low-level digital input voltage					0.8	V
lH High-level digital input current	V_1 =VDD				± 1	μA
IL Low-level digital input current	V_1 =0				± 1	μA
C; Input capacitance				8		pF

(1) The limiting frequency value at $1V_{PP}$is determined by the output-amplifier slew rate.

Output Switching Characteristics

Parameter	Test Conditions	Min	Nom	Max	Unit
tpd(DOUT) Propagation delay time,DOUT	CL=50pF			50	ns

Operating Characteristics

over recommended operating free-air temperature range, V_{DD}= 5V ±5%, V_{ref}= 2.048V (unless otherwise noted)

Parameter	Test Conditions		Min	Typ	Max	Unit
Analog output dynamic performance						
SR Output slew rate	CL=100pF, TA=+25℃	RL=10kΩ,	0.3	0.5		Vlμs
ts Output settling time	To 0.5LSB, RL=10kΩ,	CL=100pF,(1)		12.5		μ s
Glitch energy	DIN =All Os to all 1s			5		nV-s
Reference Input						
Reference feedthrough	REFIN=1Vpp at 1kHz+2.048Vdc(2)			-80		dB
Reference input bandwidth(f-3dB)	REFIN =0.2Vpp+2.048Vdc			30		kHz

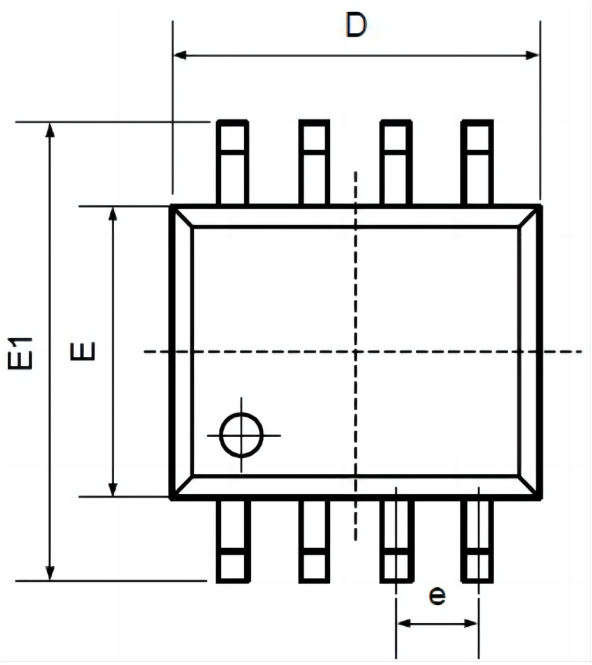
(1) Settling time is the time for the output signal to remain within ±0.5LSB of the final measured value for a digital input code change of 000 hex to 3FF hex or 3FF hex to 000 hex.

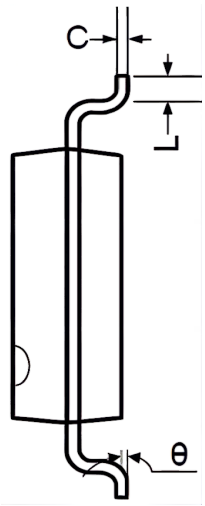
(2) Reference feedthrough is measured at the DAC output with an input code = 000 hex and aV_{ref}input = 2.048Vdc + 1Vppat 1kHz.

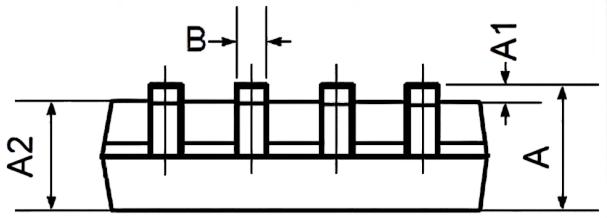
Order information

Order Number	Package	Package Quantity	Marking On The park	Temperature
MAX515CSA-TUDI	SOP8	Tape,Reel,2500	MAX515CSA	0℃ to 70℃
MAX515CPA-TUDI	DIP8	Tube,50,A box of 2000	MAX515CPA	
MAX515ESA-TUDI	SOP8	Tape,Reel,2500	MAX515ESA	-40℃ to 85℃
MAX515EPA-TUDI	DIP8	Tube,50,A box of 2000	MAX515EPA	

Package SOP8

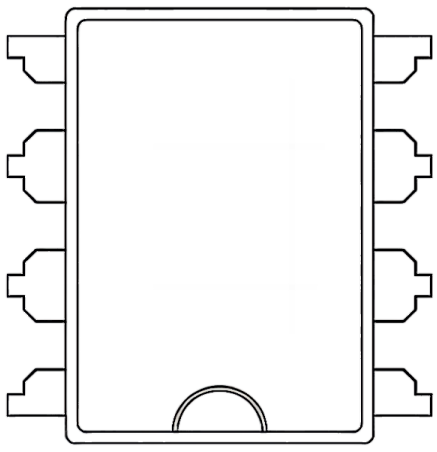


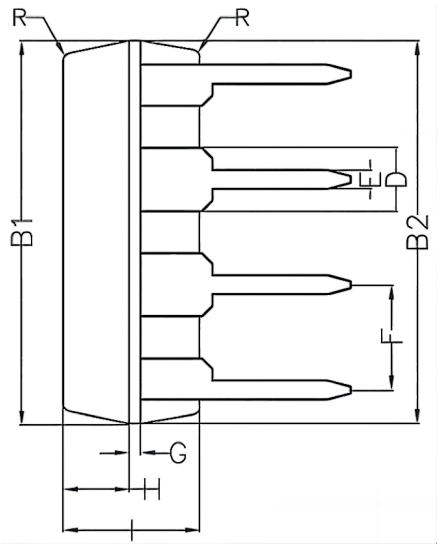


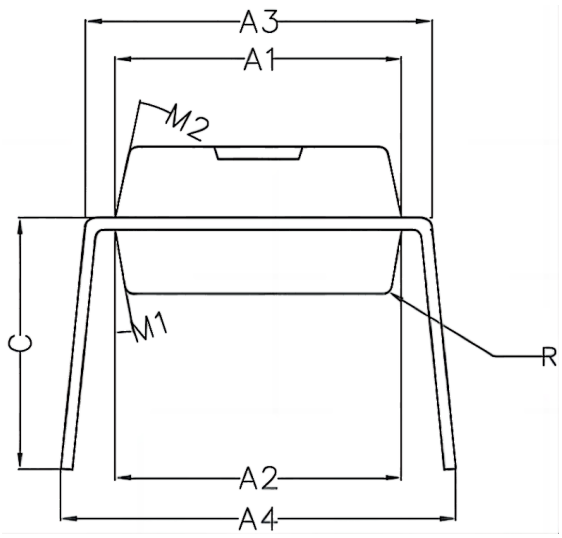


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
B	0.330	0.510	0.013	0.020
C	0.190	0.250	0.007	0.010
D	4.780	5.000	0.188	0.197
E	3.800	4.000	0.150	0.157
E1	5.800	6.300	0.228	0.248
e	1.270TYP		0.050TYP	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Package DIP8







Symbol	Min	Non	Max
A1	6.28	6.33	6.38
A2	6.33	6.38	6.43
A3	7.52	7.62	7.72
A4	7.80	8.40	9.00
B1	9.15	9.20	9.25
B2	9.20	9.25	9.30
C		5.57	
D		1.52	
E	0.43	0.45	0.47
F		2.54	
G		0.25	
H	1.54	1.59	1.64
工	3.22	3.27	3.32
R		0.20	
M1	9°	10°	11°
M2	11°	12°	13°

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