

**Octal D-type flip-flop: positive edge-trigger: 3-state****CJ74HC/HCT574 Logic****1 Introduction**

The CJ74HC/HCT574 is an octal positive-edge triggered D-type flip-flop with 3-state outputs. The device features a clock (CP) and output enable (/OE) inputs. A HIGH on /OE causes the outputs to assume a high-impedance OFF-state. Operation of the /OE input does not affect the state of the flip-flops.

2 Available Packages

PART NUMBER	PACKAGE
CJ74HC574	SOP20
	TSSOP20
CJ74HCT574	SOP20
	TSSOP20

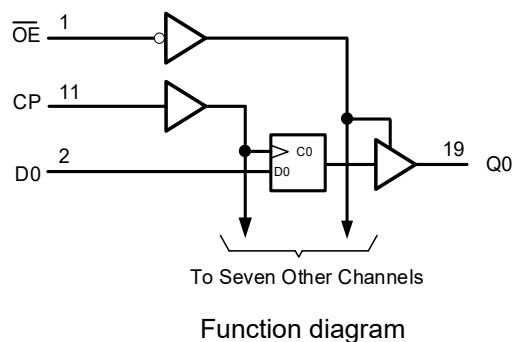
Note: For all available packages, please refer to the part Orderable Information.

3 Features

- Input levels:
 - For CJ74HC574: CMOS level
 - For CJ74HCT574: TTL level
- 3-state non-inverting outputs for bus oriented applications
- 8-bit positive, edge-triggered register
- Specified from -40°C to +125°C

4 Applications

- Printers
- Network Switches
- Tests and Measurements
- Wireless Infrastructure
- Motor Controls
- Server Motherboards



5 Orderable Information

DEVICE	PACKAGE	OP TEMP	ECO PLAN	MSL	PACKING OPTION	SORT
CJ74HC574AGN	SOP20	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 2000 Units / Reel	Active
CJ74HCT574AGN	SOP20	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 2000 Units / Reel	Active
CJ74HC574BGN	TSSOP20	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 4000 Units / Reel	Active
CJ74HCT574BGN	TSSOP20	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 4000 Units / Reel	Active

Note:

ECO PLAN: For the RoHS and Green certification standards of this product, please refer to the official report provided by JSCJ.

MSL: Moisture Sensitivity Level. Determined according to JEDEC industry standard classification.

SORT: Specifically defined as follows:

Active: Recommended for new products;

Customized: Products manufactured to meet the specific needs of customers;

Preview: The device has been released and has not been fully mass produced. The sample may or may not be available;

NoRD: It is not recommended to use the device for new design. The device is only produced for the needs of existing customers;

Obsolete: The device has been discontinued.

6 Pin Configuration and Marking Information

6.1 Pin Configuration

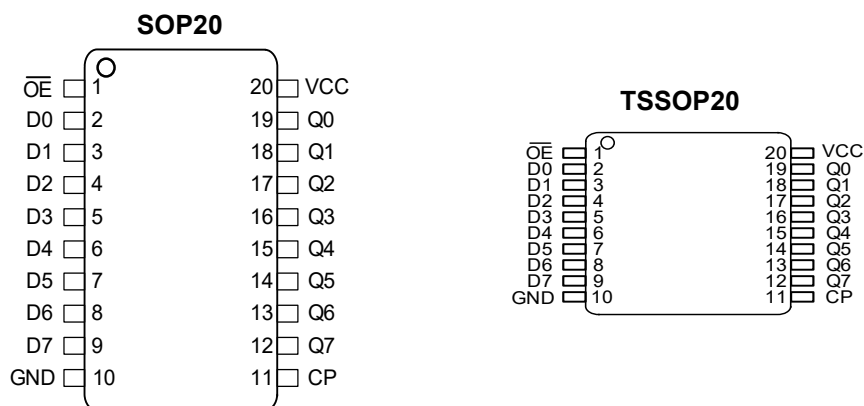


Figure 6-1 Pin configuration

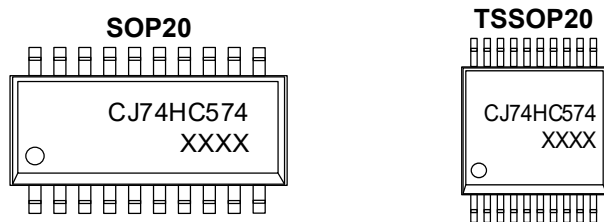
6.2 Pin Function

PIN		I/O ⁽¹⁾	DESCRIPTION
No.	NAME		
1	$\overline{OE}$	I	3-state output enable input (active LOW)
2	D0	I	Data input
3	D1	I	Data input
4	D2	I	Data input
5	D3	I	Data input
6	D4	I	Data input
7	D5	I	Data input
8	D6	I	Data input
9	D7	I	Data input
10	GND	G	Ground (0V)
11	CP	I	Clock input (LOW-to-HIGH, edge-triggered)
12	Q7	O	Flip-flop output
13	Q6	O	Flip-flop output
14	Q5	O	Flip-flop output
15	Q4	O	Flip-flop output
16	Q3	O	Flip-flop output
17	Q2	O	Flip-flop output
18	Q1	O	Flip-flop output
19	Q0	O	Flip-flop output
20	VCC	P	Supply voltage

(1) I-Input, O-Output, P-Power, G-Ground

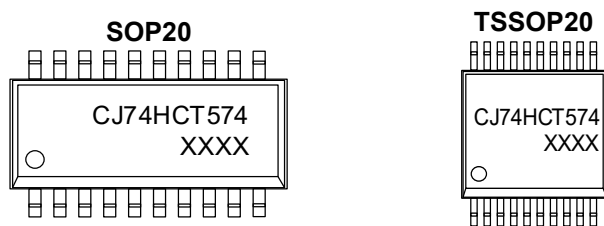
6.3 Marking Information

6.3.1 CJ74HC574



XXXX: Code, indicates weekly record information.

6.3.2 CJ74HCT574



XXXX: Code, indicates weekly record information.

7 Specifications

7.1 Absolute Maximum Ratings

Voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	MAX.	UNIT
V _{CC}	Supply voltage	-		-0.5	+7.0	V
I _{IK}	Input clamping current	V _I < -0.5V or V _I > V _{CC} +0.5V		-	±20	mA
I _{OK}	Output clamping current	V _O < -0.5V or V _O > V _{CC} +0.5V		-	±20	mA
I _O	Output current	-0.5V < V _O < V _{CC} +0.5V		-	±35	mA
I _{CC}	Supply current	-		-	70	mA
I _{GND}	Ground current	-		-70	-	mA
T _{stg}	Storage temperature	-		-65	+150	°C
P _{tot}	Total power dissipation	-		-	500	mW
T _L	Soldering temperature	10s	SOP/TSSOP	-	260	°C

Note: Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to GND. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

7.2 Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
CJ74HC574						
V _{CC}	Supply voltage	-	2.0	5.0	6.0	V
V _I	Input voltage	-	0	-	V _{CC}	V
V _O	Output voltage	-	0	-	V _{CC}	V
T _{amb}	Ambient temperature	-	-40	-	+125	°C
CJ74HCT574						
V _{CC}	Supply voltage	-	4.5	5.0	5.5	V
V _I	Input voltage	-	0	-	V _{CC}	V
V _O	Output voltage	-	0	-	V _{CC}	V
T _{amb}	Ambient temperature	-	-40	-	+125	°C

7.3 ESD Ratings

SYMBOL	ESD RATINGS		VALUE	UNIT
V _{ESD-HBM}	Electrostatic discharge	Human body model (HBM) ⁽¹⁾	±2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

7.4 Electrical Characteristics

7.4.1 DC Characteristics 1

$T_{amb}=25^{\circ}\text{C}$, voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
CJ74HC574							
V _{IH}	HIGH-level input voltage	V _{CC} =2.0V		1.5	-	-	V
		V _{CC} =4.5V		3.15	-	-	V
		V _{CC} =6.0V		4.2	-	-	V
V _{IL}	LOW-level input voltage	V _{CC} =2.0V		-	-	0.5	V
		V _{CC} =4.5V		-	-	1.35	V
		V _{CC} =6.0V		-	-	1.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}	I _O =-20uA; V _{CC} =2.0V	1.9	2.0	-	V
			I _O =-20uA; V _{CC} =4.5V	4.4	4.5	-	V
			I _O =-20uA; V _{CC} =6.0V	5.9	6.0	-	V
			I _O =-6.0mA; V _{CC} =4.5V	3.98	4.32	-	V
			I _O =-7.8mA; V _{CC} =6.0V	5.48	5.81	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}	I _O =20uA; V _{CC} =2.0V	-	0	0.1	V
			I _O =20uA; V _{CC} =4.5V	-	0	0.1	V
			I _O =20uA; V _{CC} =6.0V	-	0	0.1	V
			I _O =6.0mA; V _{CC} =4.5V	-	0.15	0.26	V
			I _O =7.8mA; V _{CC} =6.0V	-	0.16	0.26	V
I _I	Input leakage current	V _I =V _{CC} or GND; V _{CC} =6.0V		-	-	±1.0	uA
I _{OZ}	OFF-state output current	V _I =V _{IH} or V _{IL} ; V _{CC} =6.0V; V _O =V _{CC} or GND		-	-	±1.0	uA
I _{CC}	Supply current	V _I =V _{CC} or GND; I _O =0A; V _{CC} =6.0V		-	-	8.0	uA
C _I	Input capacitance	-		-	3.5	-	pF
CJ74HCT574							
V _{IH}	HIGH-level input voltage	V _{CC} =4.5V to 5.5V		2.0	-	-	V
V _{IL}	LOW-level input voltage	V _{CC} =4.5V to 5.5V		-	-	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} =4.5V	I _O =-20uA	4.4	4.5	-	V
			I _O =-6.0mA	3.98	4.32	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} =4.5V	I _O =20uA	-	0	0.1	V
			I _O =6.0mA	-	0.16	0.26	V
I _I	Input leakage current	V _I =V _{CC} or GND; V _{CC} =5.5V		-	-	±1.0	uA
I _{OZ}	OFF-state output current	V _I =V _{IH} or V _{IL} ; V _{CC} =5.5V; V _O =V _{CC} or GND		-	-	±1.0	uA
I _{CC}	Supply current	V _I =V _{CC} or GND; I _O =0A; V _{CC} =5.5V		-	-	8.0	uA
ΔI _{CC}	Additional supply current	Per input pin; V _I =V _{CC} -2.1V; Other inputs at V _{CC} or GND; I _O =0A;	Per input pin; Dn inputs	-	50	180	uA
			Per input pin; OE input	-	125	450	uA

		$V_{CC}=4.5V$ to $5.5V$	Per input pin; CP input	-	150	540	μA
C_i	Input capacitance	-		-	3.5	-	pF

7.4.2 DC Characteristics 2

$T_{amb} = -40^{\circ}C$ to $+85^{\circ}C$, voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
CJ74HC574							
V _{IH}	HIGH-level input voltage	V _{CC} =2.0V		1.5	-	-	V
		V _{CC} =4.5V		3.15	-	-	V
		V _{CC} =6.0V		4.2	-	-	V
V _{IL}	LOW-level input voltage	V _{CC} =2.0V		-	-	0.5	V
		V _{CC} =4.5V		-	-	1.35	V
		V _{CC} =6.0V		-	-	1.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}	I _O =-20uA; V _{CC} =2.0V	1.9	-	-	V
			I _O =-20uA; V _{CC} =4.5V	4.4	-	-	V
			I _O =-20uA; V _{CC} =6.0V	5.9	-	-	V
			I _O =-6.0mA; V _{CC} =4.5V	3.84	-	-	V
			I _O =-7.8mA; V _{CC} =6.0V	5.34	-	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}	I _O =20uA; V _{CC} =2.0V	-	-	0.1	V
			I _O =20uA; V _{CC} =4.5V	-	-	0.1	V
			I _O =20uA; V _{CC} =6.0V	-	-	0.1	V
			I _O =6.0mA; V _{CC} =4.5V	-	-	0.33	V
			I _O =7.8mA; V _{CC} =6.0V	-	-	0.33	V
I _I	Input leakage current	V _I =V _{CC} or GND; V _{CC} =6.0V		-	-	±2.0	uA
I _{OZ}	OFF-state output current	V _I =V _{IH} or V _{IL} ; V _{CC} =6.0V; V _O =V _{CC} or GND		-	-	±2.0	uA
I _{CC}	Supply current	V _I =V _{CC} or GND; I _O =0A; V _{CC} =6.0V		-	-	80	uA
CJ74HCT574							
V _{IH}	HIGH-level input voltage	V _{CC} =4.5V to 5.5V		2.0	-	-	V
V _{IL}	LOW-level input voltage	V _{CC} =4.5V to 5.5V		-	-	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} =4.5V	I _O =-20uA	4.4	-	-	V
			I _O =-6.0mA	3.84	-	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} =4.5V	I _O =20uA	-	-	0.1	V
			I _O =6.0mA	-	-	0.33	V
I _I	Input leakage current	V _I =V _{CC} or GND; V _{CC} =5.5V		-	-	±2.0	uA
I _{OZ}	OFF-state output current	V _I =V _{IH} or V _{IL} ; V _{CC} =5.5V; V _O =V _{CC} or GND		-	-	±2.0	uA
I _{CC}	Supply current	V _I =V _{CC} or GND; I _O =0A; V _{CC} =5.5V		-	-	80	uA
ΔI _{CC}	Additional supply current	Per input pin; V _I =V _{CC} -2.1V;	Per input pin; D _n inputs	-	-	225	uA

		Other inputs at V_{CC} or GND; $I_O=0A$; $V_{CC}=4.5V$ to 5.5V	Per input pin; OE input	-	-	563	μA
			Per input pin; CP input	-	-	675	μA

7.4.3 DC Characteristics 3

$T_{amb}=-40^{\circ}C$ to $+125^{\circ}C$, voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
CJ74HC574							
V _{IH}	HIGH-level input voltage	V _{CC} =2.0V		1.5	-	-	V
		V _{CC} =4.5V		3.15	-	-	V
		V _{CC} =6.0V		4.2	-	-	V
V _{IL}	LOW-level input voltage	V _{CC} =2.0V		-	-	0.5	V
		V _{CC} =4.5V		-	-	1.35	V
		V _{CC} =6.0V		-	-	1.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}	I _O =-20uA; V _{CC} =2.0V	1.9	-	-	V
			I _O =-20uA; V _{CC} =4.5V	4.4	-	-	V
			I _O =-20uA; V _{CC} =6.0V	5.9	-	-	V
			I _O =-6.0mA; V _{CC} =4.5V	3.7	-	-	V
			I _O =-7.8mA; V _{CC} =6.0V	5.2	-	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}	I _O =20uA; V _{CC} =2.0V	-	-	0.1	V
			I _O =20uA; V _{CC} =4.5V	-	-	0.1	V
			I _O =20uA; V _{CC} =6.0V	-	-	0.1	V
			I _O =6.0mA; V _{CC} =4.5V	-	-	0.4	V
			I _O =7.8mA; V _{CC} =6.0V	-	-	0.4	V
I _I	Input leakage current	V _I =V _{CC} or GND; V _{CC} =6.0V		-	-	±4.0	uA
I _{OZ}	OFF-state output current	V _I =V _{IH} or V _{IL} ; V _{CC} =6.0V; V _O =V _{CC} or GND		-	-	±4.0	uA
I _{CC}	Supply current	V _I =V _{CC} or GND; I _O =0A; V _{CC} =6.0V		-	-	160	uA
CJ74HCT574							
V _{IH}	HIGH-level input voltage	V _{CC} =4.5V to 5.5V		2.0	-	-	V
V _{IL}	LOW-level input voltage	V _{CC} =4.5V to 5.5V		-	-	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} =4.5V	I _O =-20uA	4.4	-	-	V
			I _O =-6.0mA	3.7	-	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} =4.5V	I _O =20uA	-	-	0.1	V
			I _O =6.0mA	-	-	0.4	V
I _I	Input leakage current	V _I =V _{CC} or GND; V _{CC} =5.5V		-	-	±4.0	uA
I _{OZ}	OFF-state output current	V _I =V _{IH} or V _{IL} ; V _{CC} =5.5V; V _O =V _{CC} or GND		-	-	±4.0	uA
I _{CC}	Supply current	V _I =V _{CC} or GND; I _O =0A; V _{CC} =5.5V		-	-	160	uA

ΔI_{CC}	Additional supply current	Per input pin; $V_i = V_{CC} - 2.1V$; Other inputs at V_{CC} or GND; $I_o = 0A$; $V_{CC} = 4.5V$ to $5.5V$;	Per input pin; Dn inputs	-	-	245	μA
			Per input pin; $\overline{OE}$ input	-	-	613	μA
			Per input pin; CP input	-	-	735	μA

7.4.4 AC Characteristics 1

$T_{amb} = 25^\circ C$, GND = 0V, $C_L = 50pF$, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
CJ74HC574							
t _{PLH} , t _{PHL}	CP to Qn propagation delay	See Figure 8-6	V _{CC} =2.0V	-	47	150	ns
			V _{CC} =4.5V	-	17	30	ns
			V _{CC} =5.0V; C _L =15pF	-	14	-	ns
			V _{CC} =6.0V	-	14	26	ns
t _{PZH} , t _{PZL}	OE to Qn enable time	See Figure 8-8	V _{CC} =2.0V	-	44	140	ns
			V _{CC} =4.5V	-	16	28	ns
			V _{CC} =6.0V	-	13	24	ns
t _{PLZ} , t _{PHZ}	OE to Qn disable time	See Figure 8-8	V _{CC} =2.0V	-	39	125	ns
			V _{CC} =4.5V	-	14	25	ns
			V _{CC} =6.0V	-	11	21	ns
t _{THL} , t _{TLH}	Transition time	Qn output; See Figure 8-6	V _{CC} =2.0V	-	14	60	ns
			V _{CC} =4.5V	-	5	12	ns
			V _{CC} =6.0V	-	4	10	ns
t _w	Pulse width	CP; HIGH or LOW; See Figure 8-7	V _{CC} =2.0V	80	-	-	ns
			V _{CC} =4.5V	16	-	-	ns
			V _{CC} =6.0V	14	-	-	ns
t _{su}	Dn to CP set-up time	See Figure 8-7	V _{CC} =2.0V	60	-	-	ns
			V _{CC} =4.5V	12	-	-	ns
			V _{CC} =6.0V	10	-	-	ns
t _h	Dn to CP hold time	See Figure 8-7	V _{CC} =2.0V	5	-	-	ns
			V _{CC} =4.5V	5	-	-	ns
			V _{CC} =6.0V	5	-	-	ns
f _{max}	Maximum frequency	CP input; See Figure 8-6	V _{CC} =2.0V	6.0	-	-	MHz
			V _{CC} =4.5V	30	-	-	MHz
			V _{CC} =5.0V; C _L =15pF	32	-	-	MHz
			V _{CC} =6.0V	35	-	-	MHz
CJ74HCT574							
t _{PLH} , t _{PHL}	CP to Qn propagation delay	See Figure 8-6	V _{CC} =4.5V	-	18	33	ns
			V _{CC} =5.0V; C _L =15pF	-	15	-	ns

t _{PZH} , t _{PZL}	$\overline{OE}$ to Qn enable time	V _{CC} =4.5V; See Figure 8-8		-	19	33	ns
t _{PLZ} , t _{PHZ}	$\overline{OE}$ to Qn disable time	V _{CC} =4.5V; See Figure 8-8		-	16	28	ns
t _{THL} , t _{TLH}	Transition time	Qn; V _{CC} =4.5V; See Figure 8-6		-	5	12	ns
t _W	Pulse width	CP; HIGH or LOW; V _{CC} =4.5V; See Figure 8-7		16	-	-	ns
t _{su}	Dn to CP set-up time	V _{CC} =4.5V; See Figure 8-7		12	-	-	ns
t _h	Dn to CP hold time	V _{CC} =4.5V; See Figure 8-7		5	-	-	ns
f _{max}	Maximum frequency	CP input; See Figure 8-6	V _{CC} =4.5V	30	-	-	MHz
			V _{CC} =5.0V; C _L =15pF	32	-	-	MHz

7.4.5 AC Characteristics 2

$T_{amb}=-40^{\circ}C$ to $+85^{\circ}C$, GND =0V, $C_L=50pF$, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
CJ74HC574							
t _{PLH} , t _{PHL}	CP to Qn propagation delay	See Figure 8-6	V _{CC} =2.0V	-	-	190	ns
			V _{CC} =4.5V	-	-	35	ns
			V _{CC} =6.0V	-	-	33	ns
t _{PZH} , t _{PZL}	OE to Qn enable time	See Figure 8-8	V _{CC} =2.0V	-	-	175	ns
			V _{CC} =4.5V	-	-	35	ns
			V _{CC} =6.0V	-	-	30	ns
t _{PLZ} , t _{PHZ}	OE to Qn disable time	See Figure 8-8	V _{CC} =2.0V	-	-	155	ns
			V _{CC} =4.5V	-	-	31	ns
			V _{CC} =6.0V	-	-	26	ns
t _{THL} , t _{TLH}	Transition time	Qn output; See Figure 8-6	V _{CC} =2.0V	-	-	75	ns
			V _{CC} =4.5V	-	-	15	ns
			V _{CC} =6.0V	-	-	13	ns
t _w	Pulse width	CP; HIGH or LOW; See Figure 8-7	V _{CC} =2.0V	100	-	-	ns
			V _{CC} =4.5V	20	-	-	ns
			V _{CC} =6.0V	17	-	-	ns
t _{su}	Dn to CP set-up time	See Figure 8-7	V _{CC} =2.0V	75	-	-	ns
			V _{CC} =4.5V	15	-	-	ns
			V _{CC} =6.0V	13	-	-	ns
t _h	Dn to CP hold time	See Figure 8-7	V _{CC} =2.0V	5	-	-	ns
			V _{CC} =4.5V	5	-	-	ns
			V _{CC} =6.0V	5	-	-	ns
f _{max}	Maximum frequency	CP input; See Figure 8-6	V _{CC} =2.0V	4.8	-	-	MHz
			V _{CC} =4.5V	24	-	-	MHz
			V _{CC} =6.0V	28	-	-	MHz
CJ74HCT574							

t_{PLH}, t_{PHL}	CP to Qn propagation delay	See Figure 8-6	$V_{CC}=4.5V$	-	-	41	ns
t_{PZH}, t_{PZL}	$\overline{OE}$ to Qn enable time	$V_{CC}=4.5V$; See Figure 8-8		-	-	41	ns
t_{PLZ}, t_{PHZ}	$\overline{OE}$ to Qn disable time	$V_{CC}=4.5V$; See Figure 8-8		-	-	35	ns
t_{THL}, t_{TLH}	Transition time	Qn; $V_{CC}=4.5V$; See Figure 8-6		-	-	15	ns
t_W	Pulse width	CP; HIGH or LOW; $V_{CC}=4.5V$; See Figure 8-7		20	-	-	ns
t_{su}	Dn to CP set-up time	$V_{CC}=4.5V$; See Figure 8-7		15	-	-	ns
t_h	Dn to CP hold time	$V_{CC}=4.5V$; See Figure 8-7		5	-	-	ns
f_{max}	Maximum frequency	CP input; See Figure 8-6	$V_{CC}=4.5V$	24	-	-	MHz

7.4.6 AC Characteristics 3

$T_{amb} = -40^{\circ}C$ to $+125^{\circ}C$, GND = 0V, $C_L = 50pF$, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
CJ74HC574						
t_{PLH}, t_{PHL}	CP to Qn propagation delay	See Figure 8-6	$V_{CC}=2.0V$	-	-	225 ns
			$V_{CC}=4.5V$	-	-	45 ns
			$V_{CC}=6.0V$	-	-	38 ns
t_{PZH}, t_{PZL}	$\overline{OE}$ to Qn enable time	See Figure 8-8	$V_{CC}=2.0V$	-	-	210 ns
			$V_{CC}=4.5V$	-	-	42 ns
			$V_{CC}=6.0V$	-	-	36 ns
t_{PLZ}, t_{PHZ}	$\overline{OE}$ to Qn disable time	See Figure 8-8	$V_{CC}=2.0V$	-	-	190 ns
			$V_{CC}=4.5V$	-	-	38 ns
			$V_{CC}=6.0V$	-	-	32 ns
t_{THL}, t_{TLH}	Transition time	Qn output; See Figure 8-6	$V_{CC}=2.0V$	-	-	90 ns
			$V_{CC}=4.5V$	-	-	18 ns
			$V_{CC}=6.0V$	-	-	15 ns
t_W	Pulse width	CP; HIGH or LOW; See Figure 8-7	$V_{CC}=2.0V$	120	-	- ns
			$V_{CC}=4.5V$	24	-	- ns
			$V_{CC}=6.0V$	20	-	- ns
t_{su}	Dn to CP set-up time	See Figure 8-7	$V_{CC}=2.0V$	90	-	- ns
			$V_{CC}=4.5V$	18	-	- ns
			$V_{CC}=6.0V$	15	-	- ns
t_h	Dn to CP hold time	See Figure 8-7	$V_{CC}=2.0V$	5	-	- ns
			$V_{CC}=4.5V$	5	-	- ns
			$V_{CC}=6.0V$	5	-	- ns
f_{max}	Maximum frequency	CP input; See Figure 8-6	$V_{CC}=2.0V$	4.0	-	- MHz
			$V_{CC}=4.5V$	20	-	- MHz
			$V_{CC}=6.0V$	24	-	- MHz

CJ74HCT574							
t_{PLH}, t_{PHL}	CP to Qn propagation delay	See Figure 8-6	$V_{CC}=4.5V$	-	-	50	ns
t_{PZH}, t_{PZL}	$\overline{OE}$ to Qn enable time	$V_{CC}=4.5V$; See Figure 8-8		-	-	50	ns
t_{PLZ}, t_{PHZ}	$\overline{OE}$ to Qn disable time	$V_{CC}=4.5V$; See Figure 8-8		-	-	42	ns
t_{THL}, t_{TLH}	Transition time	Qn; $V_{CC}=4.5V$; See Figure 8-6		-	-	18	ns
t_W	Pulse width	CP; HIGH or LOW; $V_{CC}=4.5V$; See Figure 8-7		24	-	-	ns
t_{su}	Dn to CP set-up time	$V_{CC}=4.5V$; See Figure 8-7		18	-	-	ns
t_h	Dn to CP hold time	$V_{CC}=4.5V$; See Figure 8-7		5	-	-	ns
f_{max}	Maximum frequency	CP input; See Figure 8-6	$V_{CC}=4.5V$	20	-	-	MHz

8 Detailed Description

8.1 Overview

The CJ74HC/HCT574 is an octal positive-edge triggered D-type flip-flop with 3-state outputs. The device features a clock (CP) and output enable ($\overline{OE}$) inputs. A HIGH on $\overline{OE}$ causes the outputs to assume a high-impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

8.2 Functional Block Diagram

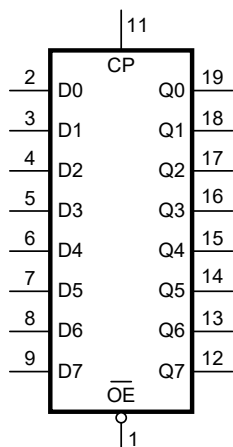


Figure 8-1 Logic symbol

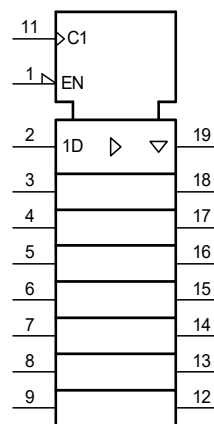


Figure 8-2 IEC logic symbol

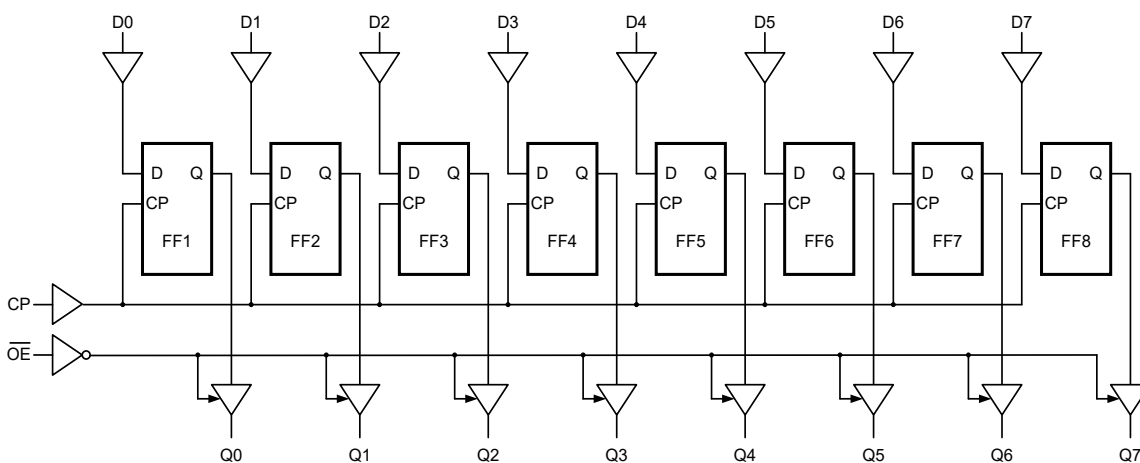


Figure 8-3 Logic diagram

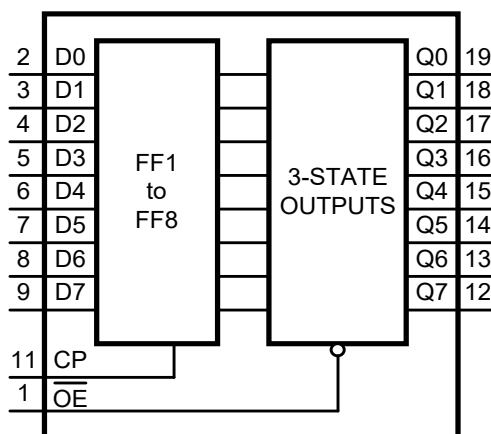


Figure 8-4 Functional diagram

8.3 Function Table⁽¹⁾

OPERATING MODES	INPUT			INTERNAL FLIP-FLOP	OUTPUT Qn
	OE	CP	Dn		
Load and read register	L	↑	l	L	L
	L	↑	h	H	H
Load register and disable outputs	H	↑	l	L	Z
	H	↑	h	H	Z

- (1) H=HIGH voltage level; L=LOW voltage level; Z=high-impedance OFF-state;
 h=HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition;
 l=LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition;
 ↑=LOW-to-HIGH clock transition.

8.4 Testing Circuit

8.4.1 AC Testing Circuit

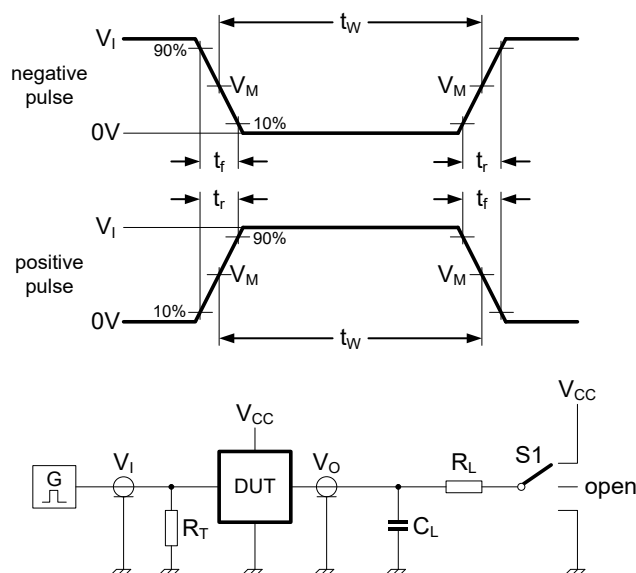


Figure 8-5 Test circuit for measuring switching times

Definitions for test circuit:

R_L =Load resistance.

C_L =Load capacitance including jig and probe capacitance.

R_T =Termination resistance should be equal to the output impedance Z_o of the pulse generator.

S1=Test selection switch.

8.4.2 AC Testing Waveforms

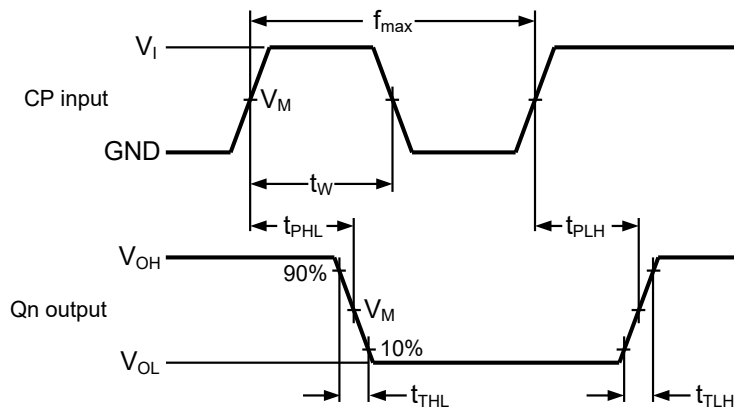


Figure 8-6 Propagation delay input (CP) to output (Qn), output transition time, clock input (CP) pulse width and the maximum frequency (CP)

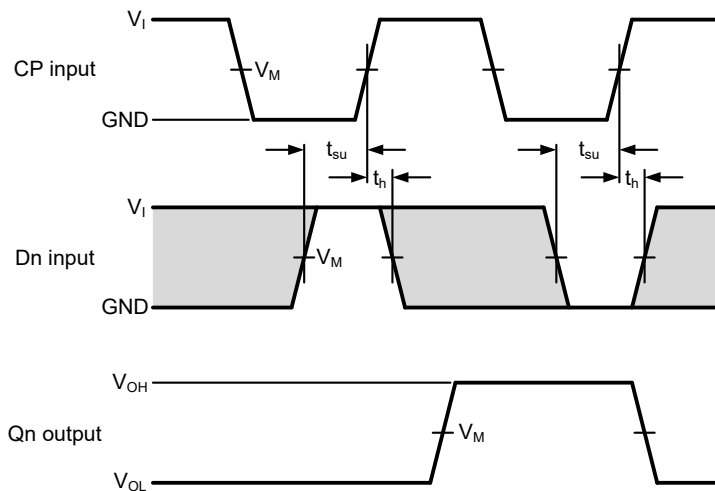


Figure 8-7 The data input (D) to clock input (CP) set-up times and clock input (CP) to data input (D) hold times

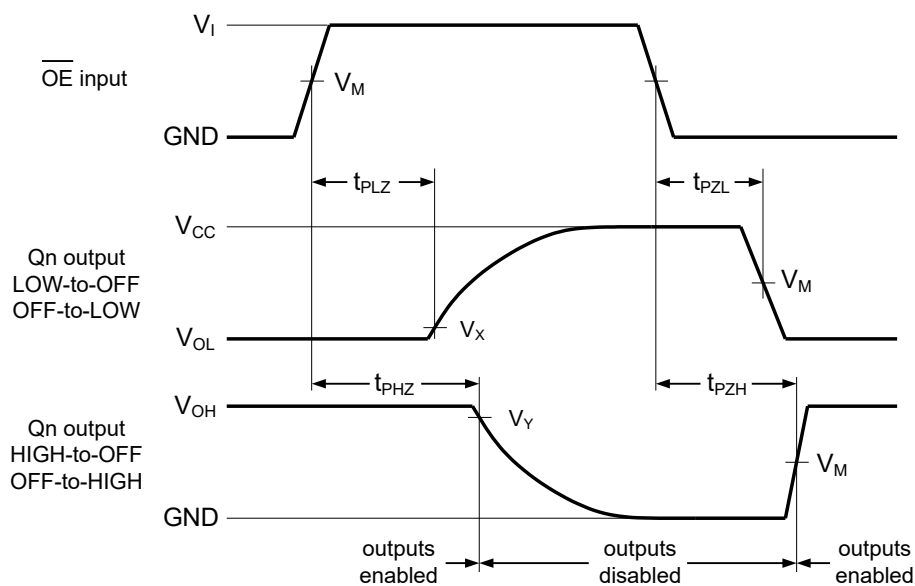


Figure 8-8 Enable and disable times

8.4.3 Measurement Points

TYPE	INPUT	OUTPUT		
	V_M	V_M	V_X	V_Y
CJ74HC574	$0.5V_{CC}$	$0.5V_{CC}$	$0.1V_{CC}$	$0.9V_{CC}$
CJ74HCT574	1.3V	1.3V	$0.1V_{CC}$	$0.9V_{CC}$

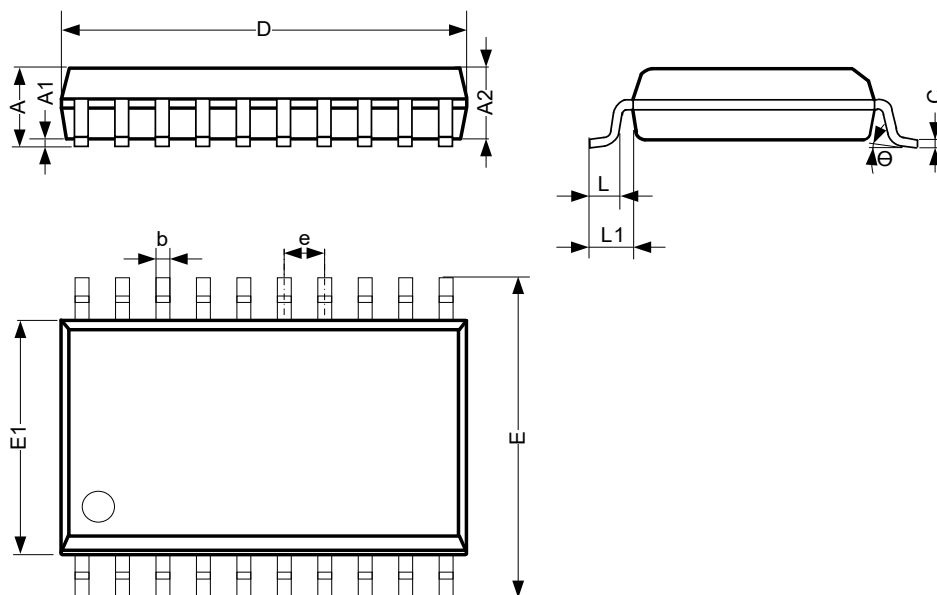
8.4.4 Test Data

TYPE	INPUT		LOAD		S1 POSITION		
	V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
CJ74HC574	V_{CC}	6ns	15pF, 50pF	1k Ω	Open	GND	V_{CC}
CJ74HCT574	3V	6ns	15pF, 50pF	1k Ω	Open	GND	V_{CC}

9 Mechanical Information

9.1 SOP20 Mechanical Information

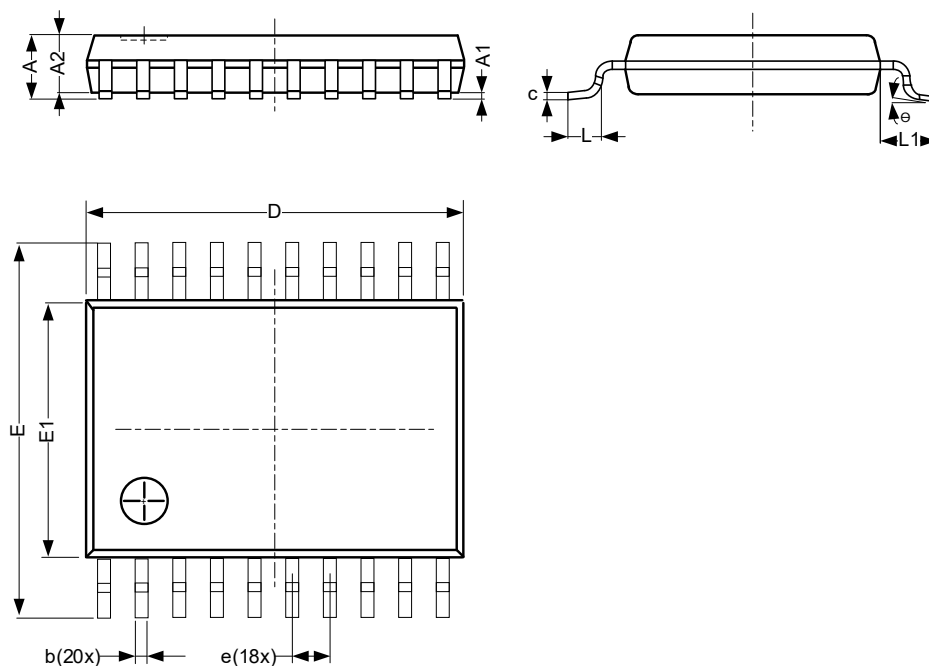
9.1.1 SOP20 Outline Dimensions



SYMBOL	Dimensions In Millimeters		
	Min.	Typ.	Max.
A	2.47	-	2.65
A1	0.05	-	0.30
A2	2.20	-	2.44
b	0.35	-	0.50
c	0.15	-	0.30
D	12.54	-	12.94
E	10.00	-	10.60
E1	7.30	-	7.70
e	1.27 BSC		
L	0.40	-	1.05
L1	1.30	-	1.50
Θ	0°	-	8°
Unit: mm			

9.2 TSSOP20 Mechanical Information

9.2.1 TSSOP20 Outline Dimensions



SYMBOL	Dimensions In Millimeters		
	Min.	Typ.	Max.
A	-	-	1.20
A1	0.05	-	0.15
A2	0.80	-	1.05
b	0.19	-	0.30
c	0.09	-	0.20
D	6.40	-	6.60
E	6.20	-	6.60
E1	4.30	-	4.50
e	0.65 BSC		
L	0.45	-	0.75
L1	-	1.00	-
θ	0°	-	8°
Unit: mm			

10 Notes and Revision History

10.1 Associated Product Family and Others

To view other products of the same type or IC products of other types, click the official website of JSCJ -- <https://www.jscj-elec.com> for more details.

10.2 Notes

Electrostatic Discharge Caution



This IC may be damaged by ESD. Relevant personnel shall comply with correct installation and use specifications to avoid ESD damage to the IC. If appropriate measures are not taken to prevent ESD damage, the hazards caused by ESD include but are not limited to degradation of integrated circuit performance or complete damage of integrated circuit. For some precision integrated circuits, a very small parameter change may cause the whole device to be inconsistent with its published specifications.

DISCLAIMER

IMPORTANT NOTICE, PLEASE READ CAREFULLY

The information in this data sheet is intended to describe the operation and characteristics of our products. JSCJ has the right to make any modification, enhancement, improvement, correction or other changes to any content in this data sheet, including but not limited to specification parameters, circuit design and application information, without prior notice.

Any person who purchases or uses JSCJ products for design shall: 1. Select products suitable for circuit application and design; 2. Design, verify and test the rationality of circuit design; 3. Procedures to ensure that the design complies with relevant laws and regulations and the requirements of such laws and regulations. JSCJ makes no warranty or representation as to the accuracy or completeness of the information contained in this data sheet and assumes no responsibility for the application or use of any of the products described in this data sheet.

Without the written consent of JSCJ, this product shall not be used in occasions requiring high quality or high reliability, including but not limited to the following occasions: medical equipment, military facilities and aerospace. JSCJ shall not be responsible for casualties or property losses caused by abnormal use or application of this product.

Official Website: www.jscj-elec.com

Copyright © JIANGSU CHANGJING ELECTRONICS TECHNOLOGY CO., LTD