先断后合时间外部可调的 HDMI 2.0 或 DP 1.4 双向多路复用器/多路解复用器

特征

- 开关类型：2:1 或 1:2
- 动态特性 （D0 到 D3 通道）
  - 差分带宽（-3dB）
    - 端口 A：典型值 8.5GHz
    - 端口 B：典型值 8.5GHz
  - 串扰（1.7GHz 时）：-30dB
  - 隔离（1.7GHz 时）：-28.5dB
  - 插入损耗（DC）
    - 端口 A：-0.5dB
    - 端口 B：-0.6dB
  - 回波损耗（1.7GHz 时）：-20dB
  - Intra-pair Skew
    - 端口 A：2ps
    - 端口 B：6ps
  - R_{ON}
    - 端口 A：6.1 Ω
    - 端口 B：8.0 Ω
- 工作电压 V_{CC}：1.65V 至 5.0V
- 工作电流 I_{CC}：典型值 26μA
- 工业扩展级的工作温度范围：−40°C 至 105°C
- 先断后合时间 t_{BBM} 可由外部电容值调节
- 封装形式：QFN42L-3.5mm x 9.0mm

应用

- 支持 4K/2K HDMI 2.0 信号开关
- DVI 1.0 信号开关
- DisplayPort 1.4 信号开关
- 通用 TMDS 信号开关
- 通用 LVDS 信号开关
- 通用高速信号开关

概述

ASW3742 是一款 12 通道 1:2 或 2:1 双向多路复用器/多路解复用器。ASW3742 基于有容微无毛刺的模拟开关切换技术，可以实现两个不同信号源的无毛刺切换，实现高质量的音视频信号传输。

ASW3742 由 1.65V 至 5V 的电源供电，可适用于电池供电的应用。该器件的导通电阻（R_{ON}）较低并且 I/O 电容较小，能够实现典型值高达 8.5GHz 的差分带宽。该器件可为 HDMI 和 DisplayPort 应用提供所需的高带宽。

ASW3742 具有断电模式，该模式下所有通道均具有高阻抗（Hi-Z）并且功耗极低。

ASW3742 的先断后合时间 t_{BBM} 可由外部电容值调节，无需额外设计、配置即可满足 HDMI CEC 标准中 HPD 时序的需求。

应用原理框图

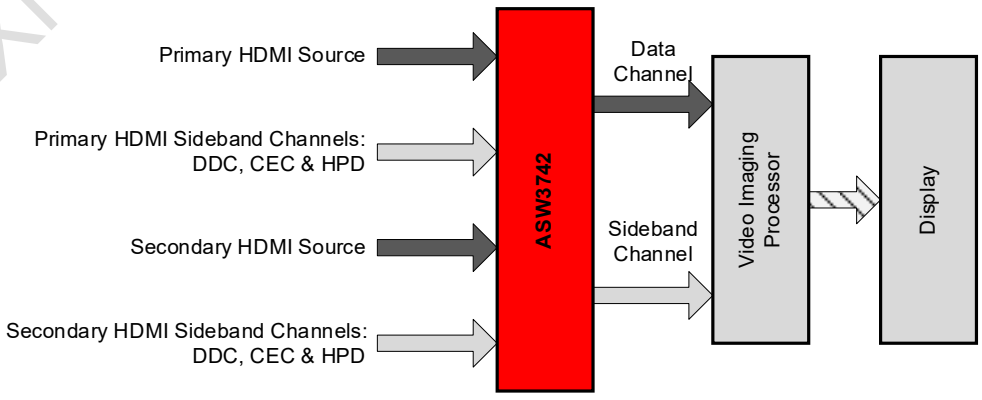


图 1, 简化的应用原理图

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修改历史记录

注：之前版本的页码可能与当前版本有所不同。

版本	修改日期	修改内容
V01	2024/4	初稿。
V02	2025/02/18	1. Pin9 引脚名称由”CSWT”改为”CTBBM”。 2. t_{SWITCH} 改名为 t_{BBM} 。
V03	2025/03/28	更新电性能参数

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PIN DIAGRAM

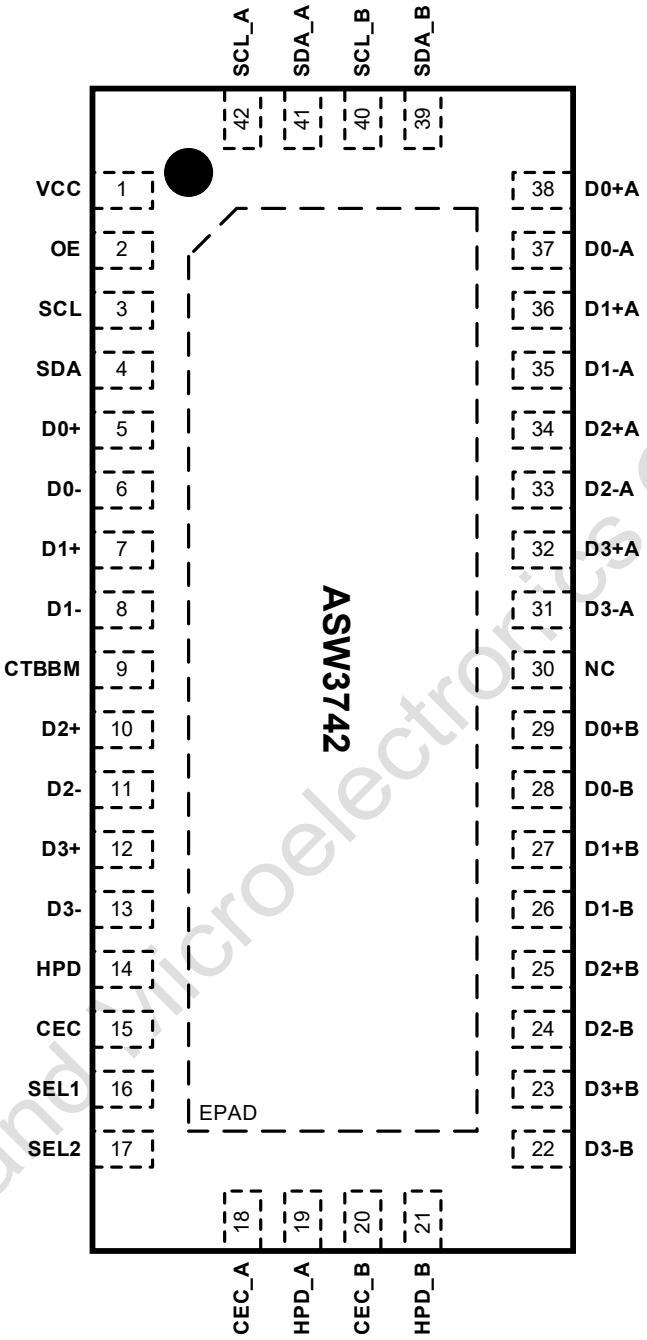


Figure 2，Pin Diagram (Top View)

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PIN DESCRIPTIONS

PIN NO.	PIN NAME	TYPE	PIN DESCRIPTIONS
1	VCC	Power	Power Supply Voltage
2	OE	IN	Output Enable, Active High(1)
3	SCL	IN/OUT	Common Port, DDC Clock
4	SDA	IN/OUT	Common Port, DDC Data
5	D0+	IN/OUT	Common Port, Channel 0, High-Speed Positive Signal
6	D0-	IN/OUT	Common Port, Channel 0, High-Speed Negative Signal
7	D1+	IN/OUT	Common Port, Channel 1, High-Speed Positive Signal
8	D1-	IN/OUT	Common Port, Channel 1, High-Speed Negative Signal
9	CTBBM	IN/OUT	External capacitor to adjust Break-Before-Make (BBM) time. if the external capacitor is unconnected, the Break-Before-Make time is minimum and about 4.7μs.
10	D2+	IN/OUT	Common Port, Channel 2, High-Speed Positive Signal
11	D2-	IN/OUT	Common Port, Channel 2, High-Speed Negative Signal
12	D3+	IN/OUT	Common Port, Channel 3, High-Speed Positive Signal
13	D3-	IN/OUT	Common Port, Channel 3, High-Speed Negative Signal
14	HPD	IN/OUT	Common Port, Hot Plug Detects
15	CEC	IN/OUT	Common Port, Consumer Electronics Control
16	SEL1	IN	Select Input 1(1)
17	SEL2	IN	Select Input 2(1)
18	CEC_A	IN/OUT	Port A, Consumer Electronics Control
19	HPD_A	IN/OUT	Port A, Hot Plug Detects
20	CEC_B	IN/OUT	Port B, Consumer Electronics Control
21	HPD_B	IN/OUT	Port B, Hot Plug Detects
22	D3-B	IN/OUT	Port B, Channel 3, High-Speed Negative Signal
23	D3+B	IN/OUT	Port B, Channel 3, High-Speed Positive Signal
24	D2-B	IN/OUT	Port B, Channel 2, High-Speed Negative Signal
25	D2+B	IN/OUT	Port B, Channel 2, High-Speed Positive Signal
26	D1-B	IN/OUT	Port B, Channel 1, High-Speed Negative Signal
27	D1+B	IN/OUT	Port B, Channel 1, High-Speed Positive Signal
28	D0-B	IN/OUT	Port B, Channel 0, High-Speed Negative Signal
29	D0+B	IN/OUT	Port B, Channel 0, High-Speed Positive Signal
30	NC	NC	No Connected
31	D3-A	IN/OUT	Port A, Channel 3, High-Speed Negative Signal
32	D3+A	IN/OUT	Port A, Channel 3, High-Speed Positive Signal
33	D2-A	IN/OUT	Port A, Channel 2, High-Speed Negative Signal
34	D2+A	IN/OUT	Port A, Channel 2, High-Speed Positive Signal
35	D1-A	IN/OUT	Port A, Channel 1, High-Speed Negative Signal
36	D1+A	IN/OUT	Port A, Channel 1, High-Speed Positive Signal
37	D0-A	IN/OUT	Port A, Channel 0, High-Speed Negative Signal
38	D0+A	IN/OUT	Port A, Channel 0, High-Speed Positive Signal
39	SDA_B	IN/OUT	Port B, DDC Data
40	SCL_B	IN/OUT	Port B, DDC Clock
41	SDA_A	IN/OUT	Port A, DDC Data
42	SCL_A	IN/OUT	Port A, DDC Clock
43	EPAD	Ground	Ground

Note:
(1) The control inputs must be held HIGH or LOW, they must not be floating.

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ABSOLUTE MAXIMUM RATINGS

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

SYMBOL	PARAMETERS	MIN.	MAX.	UNIT
V_{CC}	Supply Voltage	-0.5	5.5	V
V_{SW-HS}(2)	High Speed Differential I/O Pin Voltage Range	-0.5	2.1	V
V_{SW-LS}(2)	Low Speed I/O Pin Voltage Range (Sideband Channels)	-0.5	5.5	V
V_{IN}	Digital Input Voltage Range (SEL1, SEL2, OE)	-0.5	5.5	V
$I_{I/OK}$	Analog Port Diode Current, $V_{I/O}$ <0		-50	mA
I_{IK}	Digital Input Clamp Current, V_{IN} <0		-50	mA
I_{SW}	On-State Switch Current	-128	128	mA
ESD	HBM Model		±2.0	KV
	CDM Model		±1.0	KV
T_{STG}	Storage Temperature	-65	+150	°C

Note:
(1) The input and output negative ratings may be exceeded if the input and output diode current ratings are observed.
(2) V_{SW} refers to analog data switch paths.

RECOMMENDED OPERATING CONDITIONS

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. GrandMicro does not recommend exceeding them to designing to Absolute Maximum Ratings.

SYMBOL	PARAMETERS	MIN.	MAX.	UNIT
V_{CC}	Supply Voltage	1.65	5.0	V
$t_{RAMP(VCC)}$	Power Supply Slew Rate	100	1000	μs/V
V_{IN}	Control Input Voltage (SEL1, SEL2, OE)(3)	-0.5	5.0	V
V_{SW-HS}	High Speed Differential I/O Pin Voltage	-0.5	2.0	V
V_{SW-LS}	Low Speed I/O Pin Voltage	-0.5	5.0	V
T_A	Operating Temperature	-40	+105	°C

Note:
(3) The control inputs must be held HIGH or LOW, they must not float.

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DC ELECTRICALS

All typical values are at T_A=25°C unless otherwise specified.

SYMBOL	PARAMETER		TEST CONDITION(4)	MIN	TYP	MAX	UNIT
PORT A							
R_{ON}	ON-state Resistance	D0 to D3	V_{CC} = 3.3V, 0V ≤ $V_{I/O}$ ≤ 2V, $I_{I/O}$ = -10mA		6.1		Ω
		SCL, SDA, HPD, CEC	V_{CC} = 3.3V, 0V ≤ $V_{I/O}$ ≤ V_{CC}, $I_{I/O}$ = -10mA		5.0		Ω
$R_{ON(flat)}$(5)	ON-state resistance flatness	D0 to D3	V_{CC} = 3.3V, 0V ≤ $V_{I/O}$ ≤ 2V, $I_{I/O}$ = -10mA		0.2		Ω
		SCL, SDA, HPD, CEC	V_{CC} = 3.3V, 0V ≤ $V_{I/O}$ ≤ V_{CC}, $I_{I/O}$ = -10mA		0.2		Ω
$\triangle R_{ON}$(6)	ON-state resistance match between high-speed channels	D0 to D3	V_{CC} = 3.3V, 0V ≤ $V_{I/O}$ ≤ 2V, $I_{I/O}$ = -10mA		0.6		Ω
	ON-state resistance match between sideband channels	SCL, SDA, HPD, CEC	V_{CC} = 3.3V, 0V ≤ $V_{I/O}$ ≤ V_{CC}, $I_{I/O}$ = -10mA		0.4	0.7	Ω
I_{OFF}	Leakage under power off	D0 to D3	V_{CC} = 0V, $V_{I/O}$ = 0V to 2V, V_{IN} = 0V to 5.5V			±1	μA
		SCL, SDA, HPD, CEC	V_{CC} = 0V, $V_{I/O}$ = 0V to 3.6V, V_{IN} = 0V to 5.5V			±1	μA
PORT B							
R_{ON}	ON-state Resistance	D0 to D3	V_{CC} = 3.3V, 0V ≤ $V_{I/O}$ ≤ 2V, $I_{I/O}$ = -10mA		8.0		Ω
		SCL, SDA, HPD, CEC	V_{CC} = 3.3V, 0V ≤ $V_{I/O}$ ≤ V_{CC}, $I_{I/O}$ = -10mA		5.4		Ω
$R_{ON(flat)}$(5)	ON-state resistance flatness	D0 to D3	V_{CC} = 3.3V, 0V ≤ $V_{I/O}$ ≤ 2V, $I_{I/O}$ =-10mA		0.2		Ω
		SCL, SDA, HPD, CEC	V_{CC} = 3.3V, 0V ≤ $V_{I/O}$ ≤ V_{CC}, $I_{I/O}$ =-10mA		0.2		Ω
$\triangle R_{ON}$(6)	ON-state resistance match between high-speed channels	D0 to D3	V_{CC} = 3.3V, 0V ≤ $V_{I/O}$ ≤ 2V, $I_{I/O}$ =-10mA		0.6		Ω
	ON-state resistance match between sideband channels	SCL, SDA, HPD, CEC	V_{CC} = 3.3V, 0V ≤ $V_{I/O}$ ≤ V_{CC}, $I_{I/O}$ = -10mA		0.3	0.7	Ω
I_{OFF}	Leakage under power off	D0 to D3	V_{CC} = 0V, $V_{I/O}$ = 0V to 2V, V_{IN} = 0V to 5.5V			±1	μA
		SCL, SDA, HPD, CEC	V_{CC} = 0V, $V_{I/O}$ = 0V to 3.6V, V_{IN} = 0V to 5.5V			±1	μA
DIGITAL INPUTS (SEL1, SEL2, OE)							
V_{IH}	Control Input Voltage High	SEL1, SEL2, OE		1.1			V
V_{IL}	Control Input Voltage Low	SEL1, SEL2, OE				1.0	V
I_{IH}	Digital Input High Leakage Current	SEL1, SEL2, OE	V_{CC} = 3.6V, V_{IN} = V_{CC}			±1	μA
I_{IL}	Digital Input Low Leakage Current	SEL1, SEL2, OE	V_{CC} = 3.6V, V_{IN} = GND			±1	μA
SUPPLY							
I_{CC}	VCC Supply Current		V_{CC} = 3.6V, $I_{I/O}$ = 0, Normal Operation Model, OE = H		26		μA
$I_{CC,PD}$	VCC Supply Current in Power-Down Mode		V_{CC} = 3.6V, $I_{I/O}$ = 0, Power-Down Model, OE = L		0.1		μA

Note:
(4) V_I, V_O, I_I and I_O refer to I/O pins, and V_{IN} refers to the control pins.
(5) $R_{ON(FLAT)}$ is the difference of R_{ON} in a given channel at specified voltages.
(6) $\triangle R_{ON}$ is the difference of R_{ON} from center port to any other ports.

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AC ELECTRICALS OF HIGH-SPEED CHANNELS

All typical values are at T_A=25°C, V_{CC} = 3.3V unless otherwise specified.

SYMBOL	PARAMETER		TEST CONDITION		MIN	TYP	MAX	UNIT
C_{IN}	Digital Input Capacitance		f = 1MHz, V_{IN} = 0V			6.0		pF
C_{OFF}	Switch OFF Capacitance		f = 1GHz, $V_{I/O}$ = 0V, Output is open, Switch is OFF			0.3		pF
C_{ON}	Switch ON Capacitance		f = 1GHz, $V_{I/O}$ = 0V, Output is open, Switch is ON			0.5		pF
X_{TALK}	Differential Crosstalk		R_L = 50 Ω at 1.7GHz, See Figure 16	Port A		-30		dB
				Port B		-33		
			R_L = 50 Ω at 2.7GHz, See Figure 16	Port A		-28		
				Port B		-31		
			R_L = 50 Ω at 4.05GHz, See Figure 16	Port A		-26		
				Port B		-31		
O_{ISO}	Differential OFF Isolation		R_L = 50 Ω at 1.7GHz, See Figure 17			-28.5		dB
			R_L = 50 Ω at 2.7GHz, See Figure 17			-22		
			R_L = 50 Ω at 4.05GHz, See Figure 17			-19.5		
IL	Insertion Loss		Port A at DC			-0.5		dB
			Port B at DC			-0.6		
BW	Differential Bandwidth (-3dB)	Port A	R_L = 50 Ω, All Channels, See Figure 18		7.0	8.5		GHz
		Port B	R_L = 50 Ω, All Channels, See Figure 18		7.2	8.5		

AC ELECTRICALS OF SIDEBAND CHANNELS

All typical values are at T_A=25°C, V_{CC} = 3.3V unless otherwise specified.

SYMBOL	PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
C_{IN}	Digital Input Capacitance		f = 1MHz, V_{IN} = 0V		6.0		pF
C_{OFF}	Switch OFF Capacitance		f = 1MHz, $V_{I/O}$ = 0V, Output is open, Switch is OFF		2.0		pF
C_{ON}	Switch ON Capacitance		f = 1MHz, $V_{I/O}$ = 0V, Output is open, Switch is ON		3.5		pF
X_{TALK}	Differential Crosstalk		R_L = 50 Ω at 250MHz, See Figure 16		-15		dB
O_{ISO}	Differential OFF Isolation		R_L = 50 Ω at 250MHz, See Figure 17		-40		dB
IL	Insertion Loss		Port A at DC		-0.5		dB
			Port B at DC		-0.5		
BW	Differential Bandwidth (-3dB)	Port A	R_L = 50 Ω, All Channels, See Figure 18		1.1		GHz
		Port B	R_L = 50 Ω, All Channels, See Figure 18		1.1		

SWITCHING ELECTRICALS

All typical values are at T_A=25°C, V_{CC} = 3.3V unless otherwise specified.

SYMBOL	PARAMETER			TEST CONDITION	MIN	TYP	MAX	UNIT
t_{ON}(7)	Switch Turn-ON Time		D0 to D3	See Figure 13		1.0		µs
			SCL, SDA, HPD, CEC			20		
t_{BBM}(8)	Break-Before-Make time when CTBBM is floating		All I/O	See Figure 14		4.7	5	µs
	Break-Before-Make time between channels when CTBBM is 4.7uF		All I/O	See Figure 14		530	580	ms
t_{pd}	Propagation Delay	Port A	D0 to D3	See Figure 15		30		ps
			SCL, SDA, HPD, CEC			30		
		Port B	D0 to D3			40		
			SCL, SDA, HPD, CEC			30		
t_{SKEW}	Inter-pair Skew	Port A	D0 to D3	Between +ve and –ve signals of each channel		2.0		ps
		Port B				2.0		
	Intra-pair Skew	Port A		Between channel 0, 1, 2, 3		2.0		
		Port B				6.0		

Note:
(7) t_{ON} is the time it takes the output to recover after enabling switches.
(8) t_{BBM} is the time when the existing connection is broken (opened) before a new connection is made (closed).

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TYPICAL PERFORMANCES OF HIGH-SPEED CHANNELS

All typical values are at T_A=25°C, V_{CC} = 3.3V unless otherwise specified.

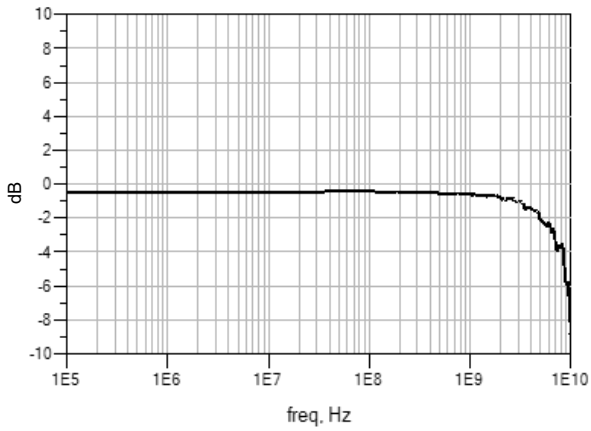


Figure 3, Differential S21 vs Frequency for Port A

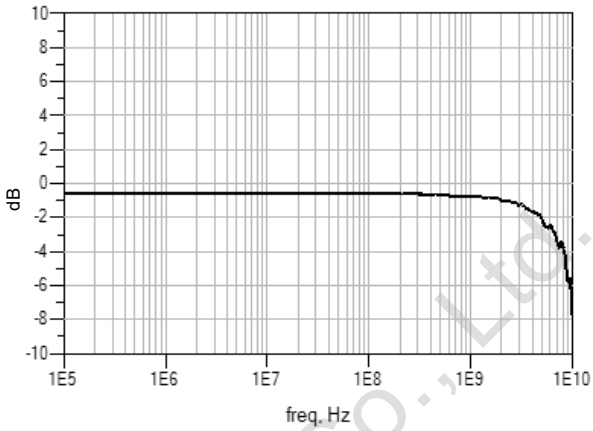


Figure 4, Differential S21 vs Frequency for Port B

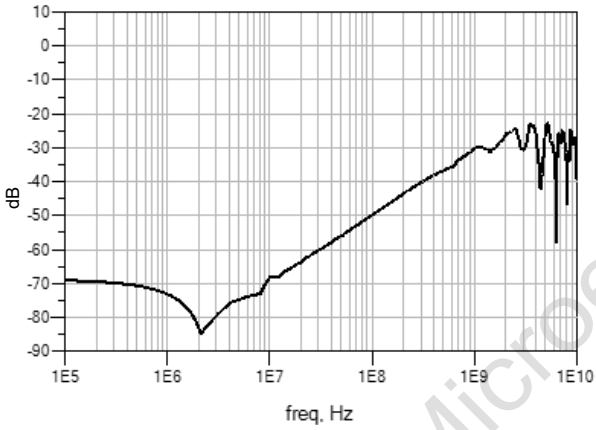


Figure 5, XTALK for Port A

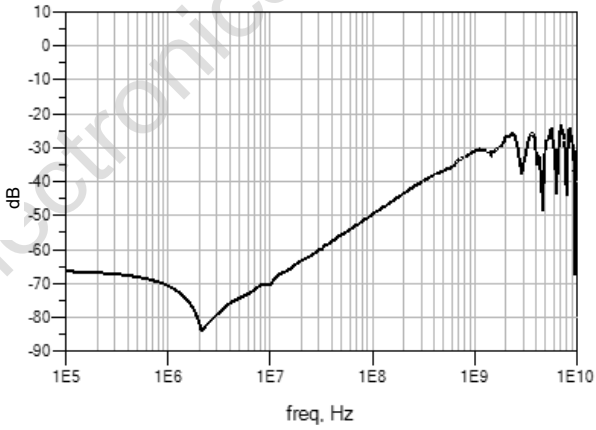


Figure 6, XTALK for Port B

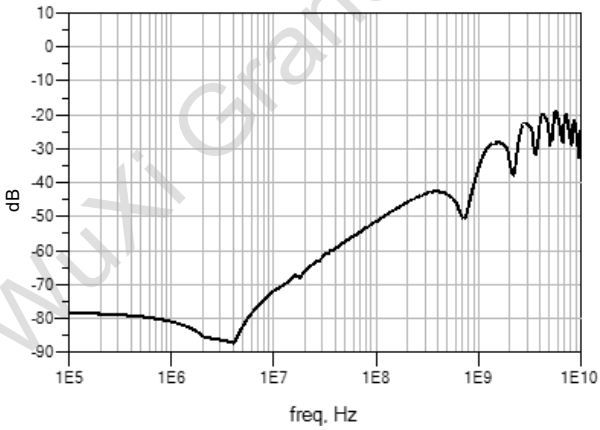


Figure 7, Off-State Isolation (OISO) for Port A

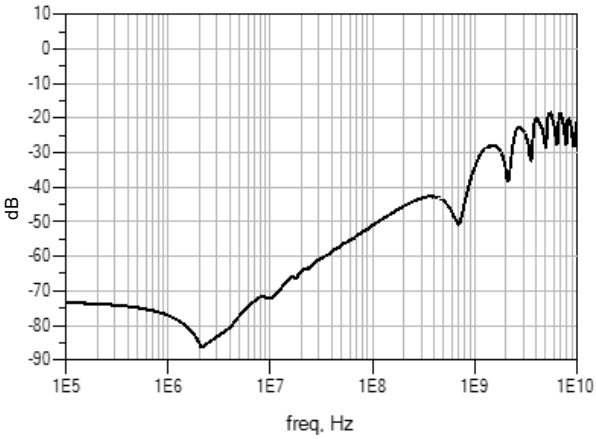


Figure 8, Off-State Isolation (OISO) for Port B

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TYPICAL PERFORMANCES OF HIGH-SPEED CHANNELS (CONT.)

All typical values are at T_A=25°C, V_{CC} = 3.3V unless otherwise specified.

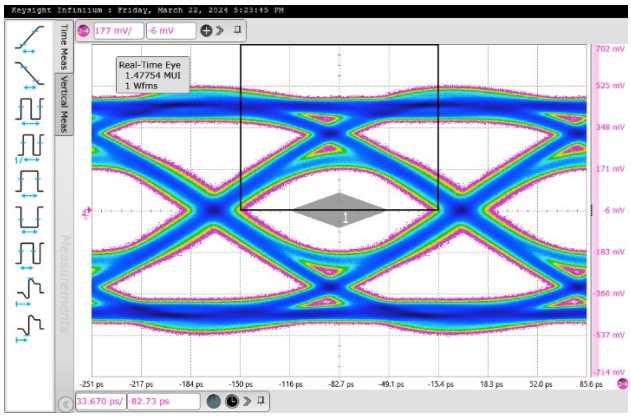


Figure 9, Eye Pattern: HDMI2.0 test, 1 Data Lane, No Device through Path

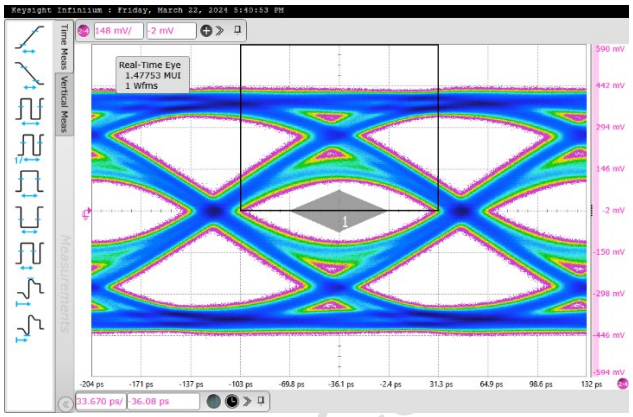


Figure 10, Eye Pattern: HDMI2.0 test, 1 Data Lane, With Device

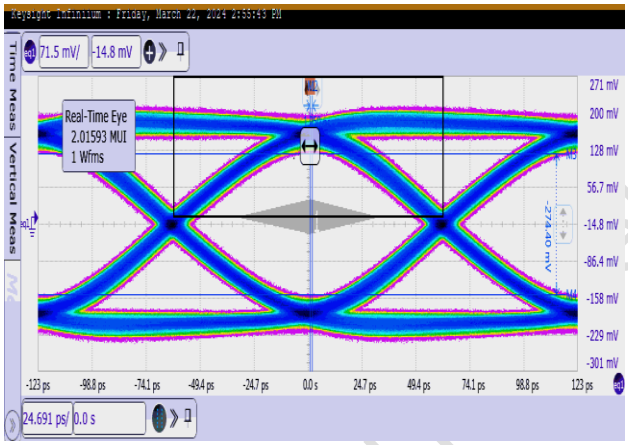


Figure 11, Eye Pattern: DP1.4 test, 1 Data Lane, TPS4 No Device through Path

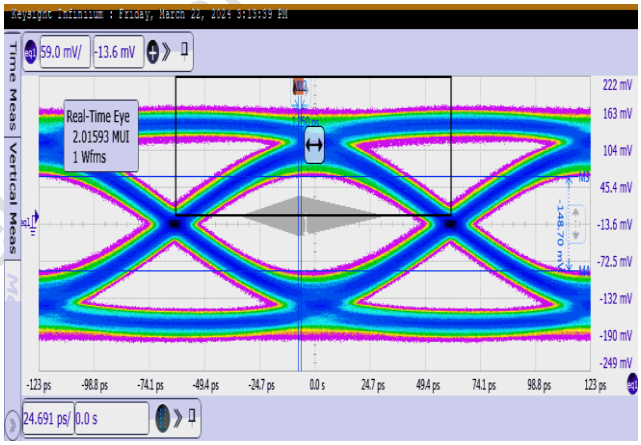


Figure 12, Eye Pattern: DP1.4 test, 1 Data Lane, TPS4 With Device

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TEST CIRCUITS

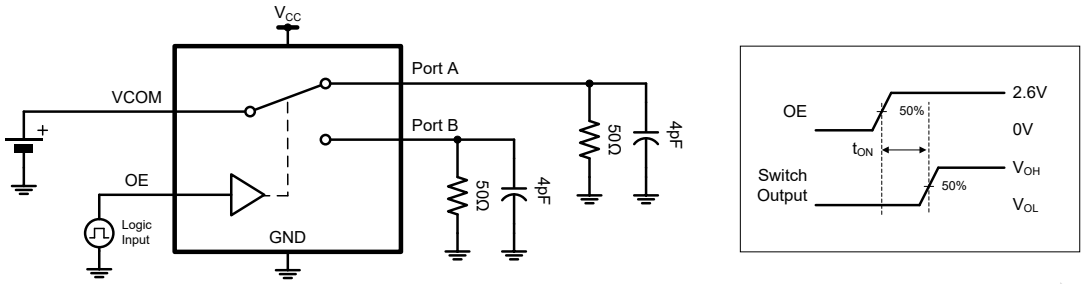


Figure 13, Switch Turn-On Time (t_{ON})

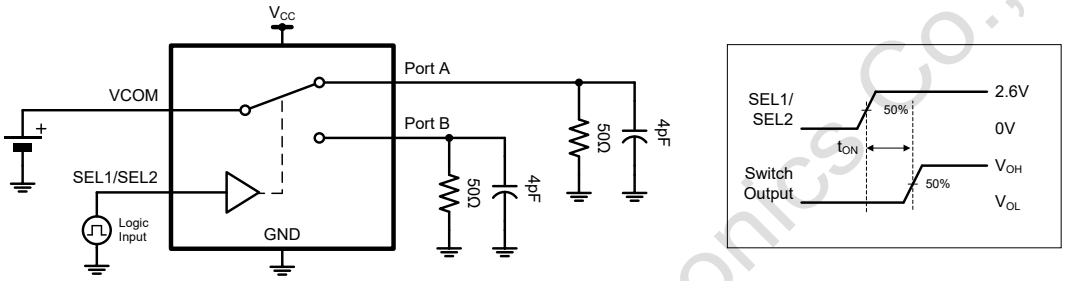
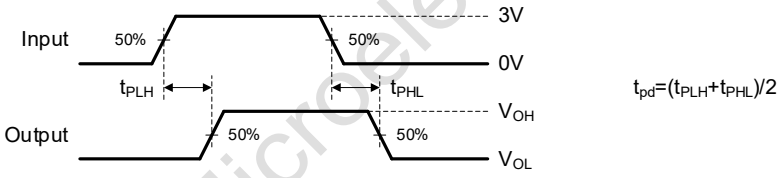


Figure 14, Break-Before-Make Time (t_{BBM})



$t_{pd}=(t_{PLH}+t_{PHL})/2$

Figure 15, Propagation Delay (t_{pd})

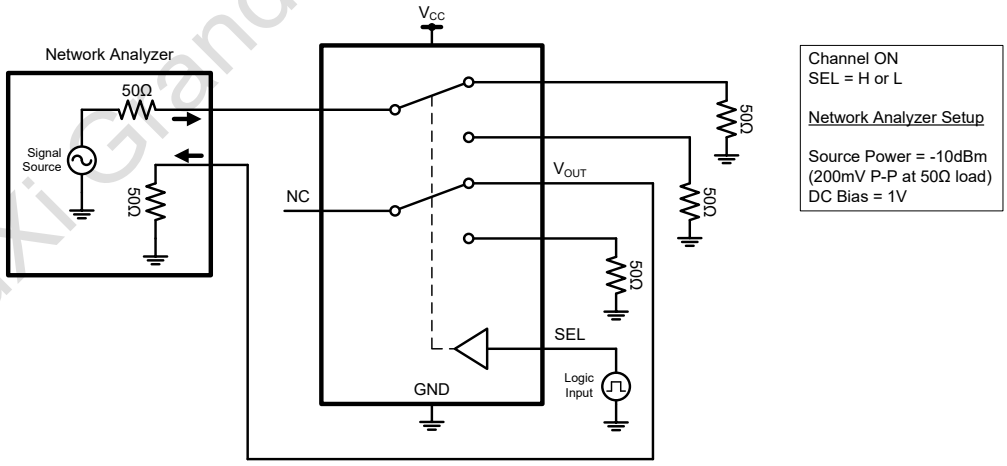


Figure 16, Crosstalk (X_{TALK})

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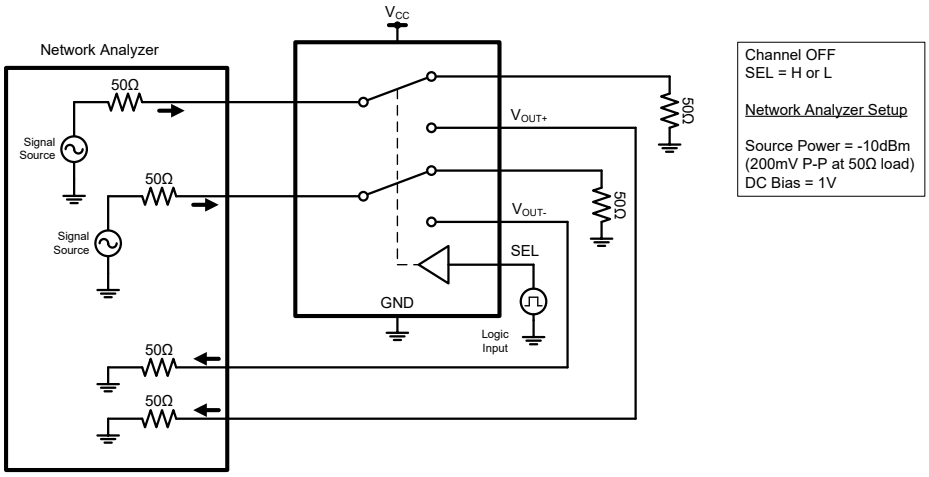


Figure 17, Differential Off-Isolation (O_{ISO})

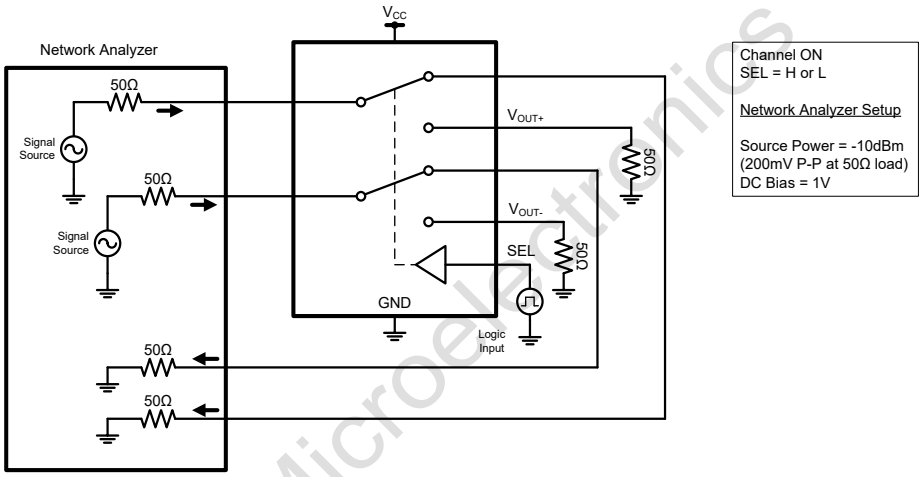


Figure 18, -3dB Differential Bandwidth (BW)

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FUNCTION DESCRIPTIONS

1. Overview

ASW3742 is a 12-channel 1:2 or 2:1 bidirectional multiplexer/de-multiplexer. The ASW3742 operates from a 1.65V to 5.0V supply, making it suitable for battery-powered applications. It offers low and flat on-state resistance as well as low I/O capacitance which allows it to achieve a typical bandwidth of up to 8.5GHz of high-speed channels, and 1.1GHz of sideband channels. The device provides the high bandwidth necessary for HDMI and DisplayPort applications.

2. Functional Block Diagram

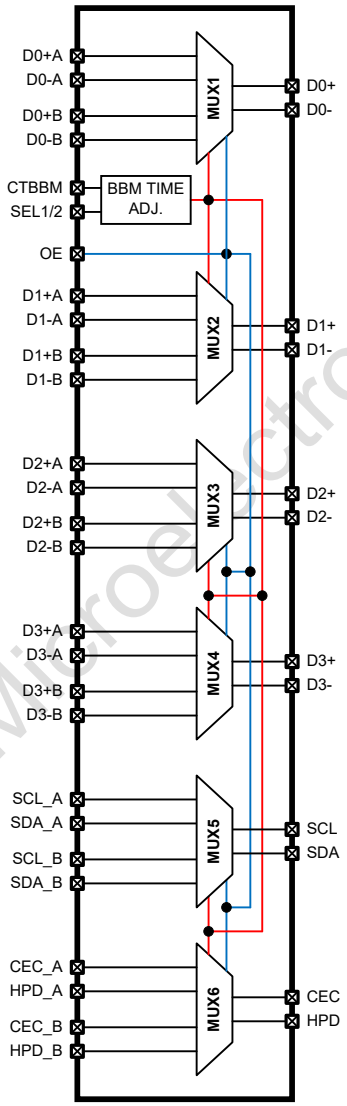


Figure 19, Functional Block Diagram

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3. Feature Description

The ASW3742 uses FET switches driven by a high-voltage generated from an integrated charge-pump to achieve a low on-state resistance. ASW3742 has 12-channel bidirectional switches with a high bandwidth (~8.5GHz) for high-speed channels and a low bandwidth (~1.1GHz) for sideband channel. ASW3742 uses an extremely low power technology and consumes only 26μA current in active mode. The device has integrated ESD that can support up to 2kV Human-Body-Model (HBM) and 1kV Charge Device Model (CDM). ASW3742 can support high-speed analog I/O signal in -0.5V to 2V range and low-speed analog I/O signal in -0.5V to 5.0V range.

ASW3742 also has a special feature that prevents the device from back-powering when the V_{CC} supply is unavailable and an analog signal is applied on the I/O pin. In this situation this special feature prevents leakage current in the device.

4. Device Functional Models

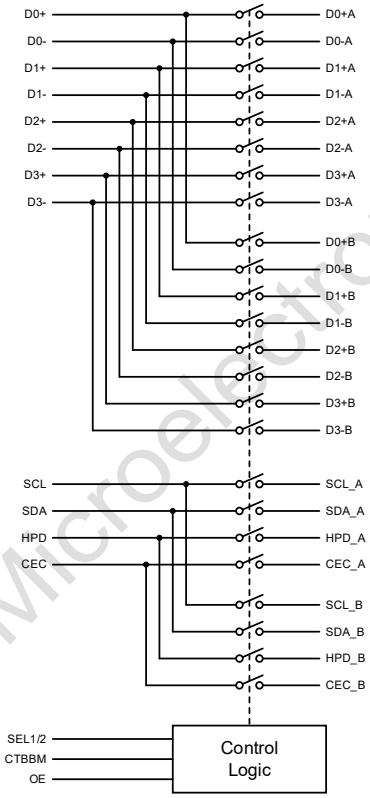


Figure 20, Logic Diagram

Table 1, Functional Table

Table 1 lists the device functions for the ASW3742 device.

OE	SEL1	SEL2	FUNCTION
L	X	X	Switch disabled. All channels are Hi-Z.
H	L	L	Channel D0+/D0- to D0+A/D0-A is ON. All the other channels (D1+/D1-, D2+/D2-, D3+/D3-, SCL, SDA, HPD, CEC) are Hi-Z.
H	L	H	Channel D0+/D0- to D0+B/D0-B is ON. All the other channels (D1+/D1-, D2+/D2-, D3+/D3-, SCL, SDA, HPD, CEC) are Hi-Z.
H	H	L	All A channels are enabled. All B channels are Hi-Z.
H	H	H	All B channels are enabled. All A channels are Hi-Z.

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5. Break-Before-Make time between all A channels and all B channels

The Break-Before-Make time between all A channels and all B channels is determined by the external capacitor connected to CTBBM pin. When ASW3742 detects the change of SEL2 pin, it will charge the external capacitor connected to CTBBM pin with a current of about 10uA, once if the voltage on CTBBM pin reaches threshold voltage of about 1V, all A/B channels will change from ON/Hi-Z to Hi-Z/ON. During the Break-Before-Make time, all A/B channels will be Hi-Z/Hi-Z shown in figure 21 for details. If SEL2 changes from HIGH to LOW and the change time of SEL2 is smaller than the Break-Before-Make time, then all A channels will be Hi-Z always shown in figure 22. If SEL2 changes from LOW to HIGH and the change time of SEL2 is smaller than the Break-Before-Make time, then all B channels will be Hi-Z always shown in figure 23.

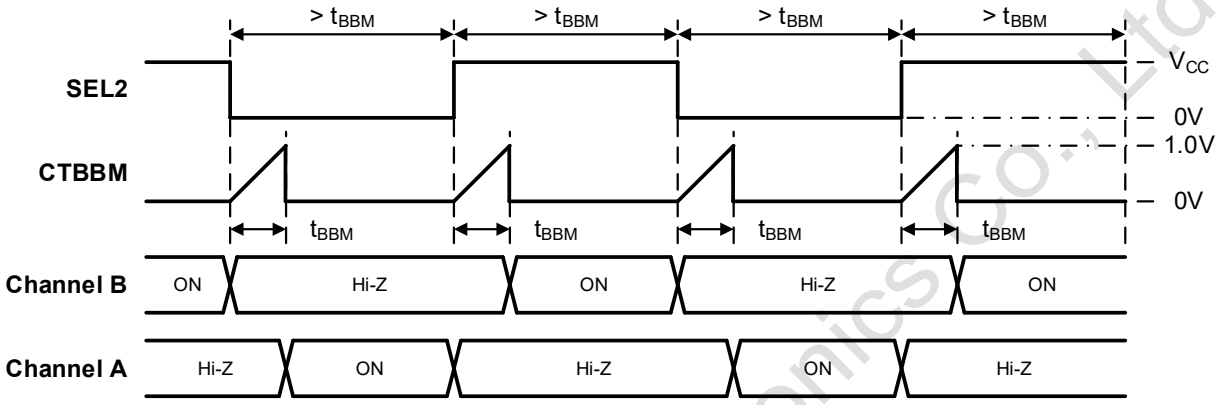


Figure 21, the change time of SEL2 is bigger than t_{BBM}

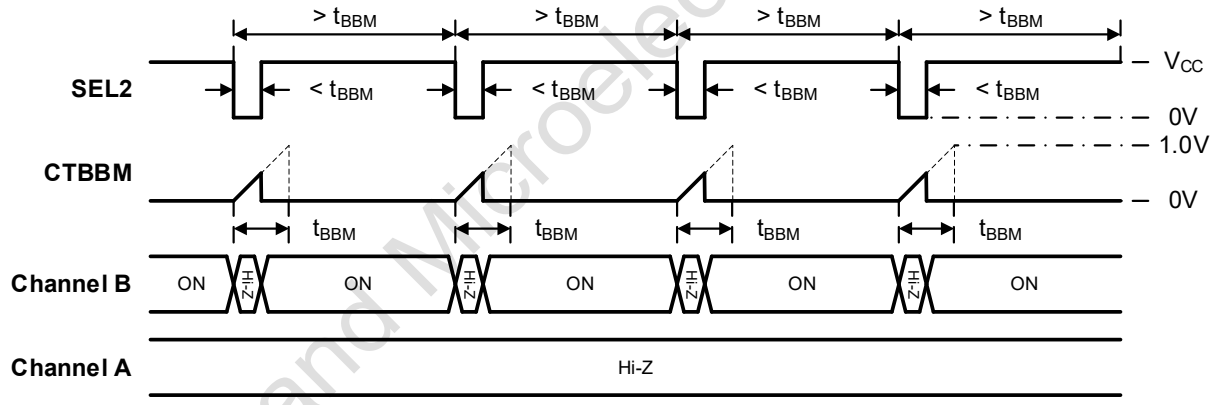


Figure 22, SEL2 changes from HIGH to LOW and the change time is smaller than t_{BBM}

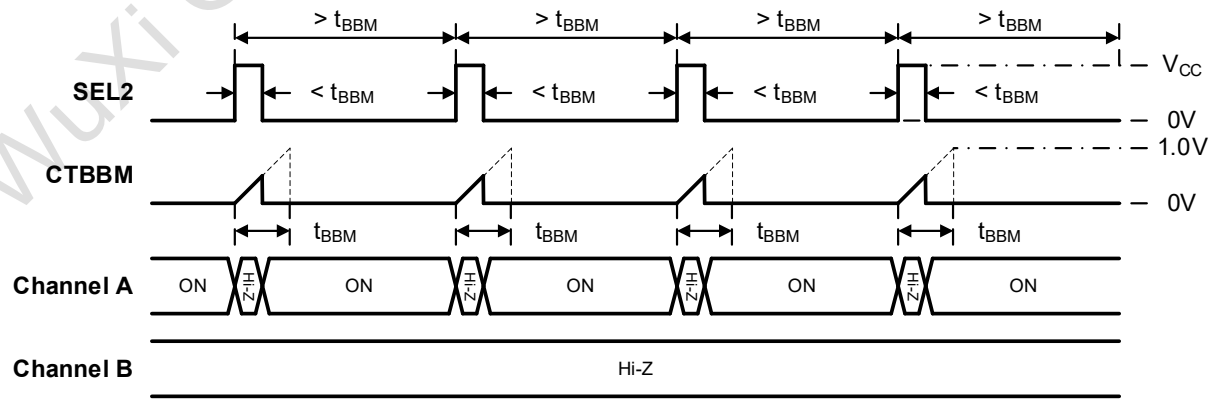


Figure 23, SEL2 changes from LOW to HIGH and the change time is smaller than t_{BBM}

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The t_{BBM} time can be calculated as below:

$$t_{BBM} = \frac{CTBBM \times 1V}{10uA} \quad \text{.....(1)}$$

Figure 24 shows the linear relationship between the t_{BBM} and the capacitor on CTBBM pin, and the appropriate capacitor value can be selected according to the requirements. When the CTBBM pin is floating, the t_{BBM} is about 4.7μs, while the CTBBM pin is connected with a capacitor of 4.7μF, the t_{BBM} is about 530ms.

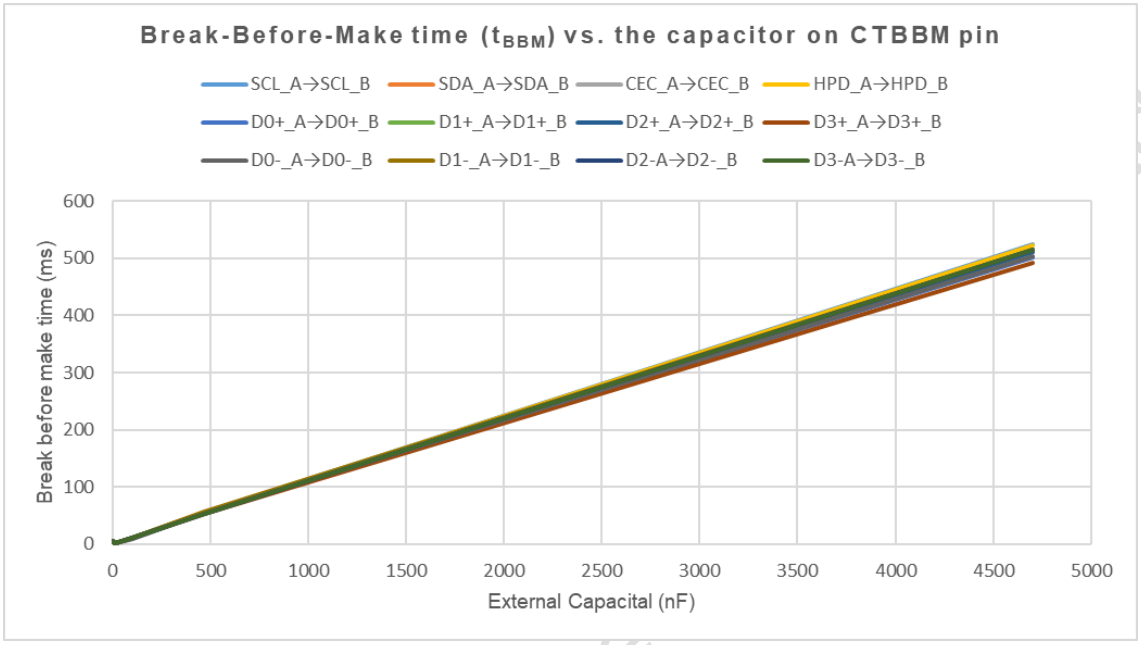


Figure 24, Break-Before-Make time (t_{BBM}) vs. the capacitor on CTBBM pin

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TYPICAL APPLICATION DIAGRAM

1. HDMI Application

HDMI Application with ASW3742 used to switch signals from a single graphic and memory controller to two HDMI connectors.

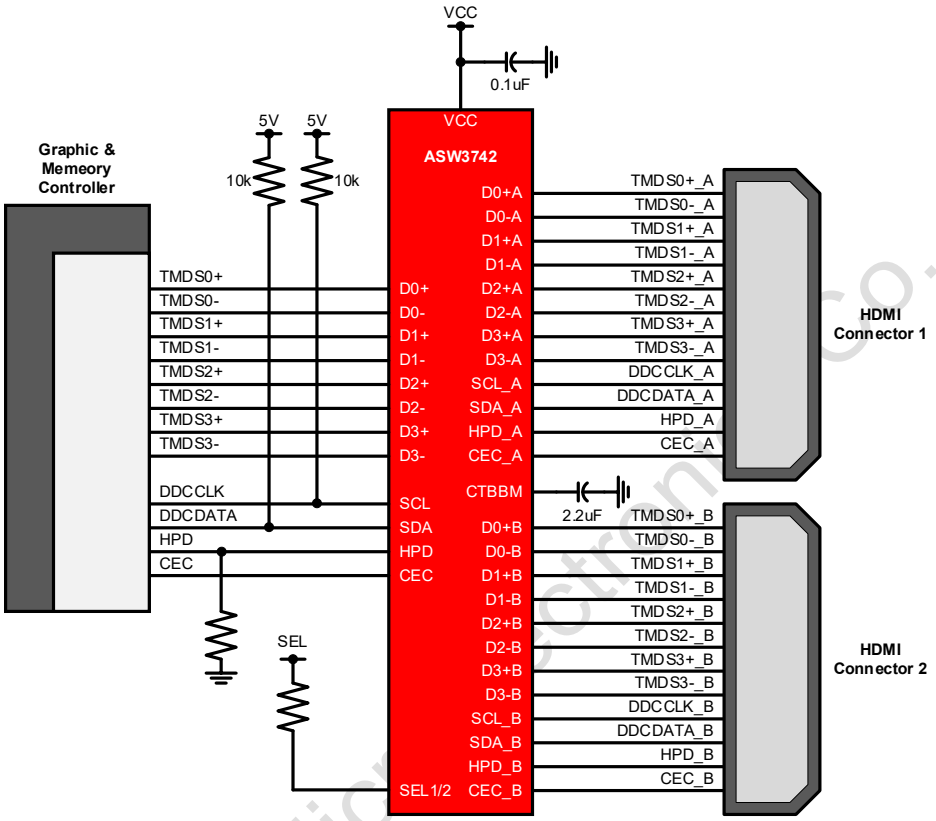


Figure 25，HDMI Application Diagram

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2.DisplayPort (DP) Application

DisplayPort (DP) application with ASW3742 used to switch between two different graphic and memory controllers on a single DP connector.

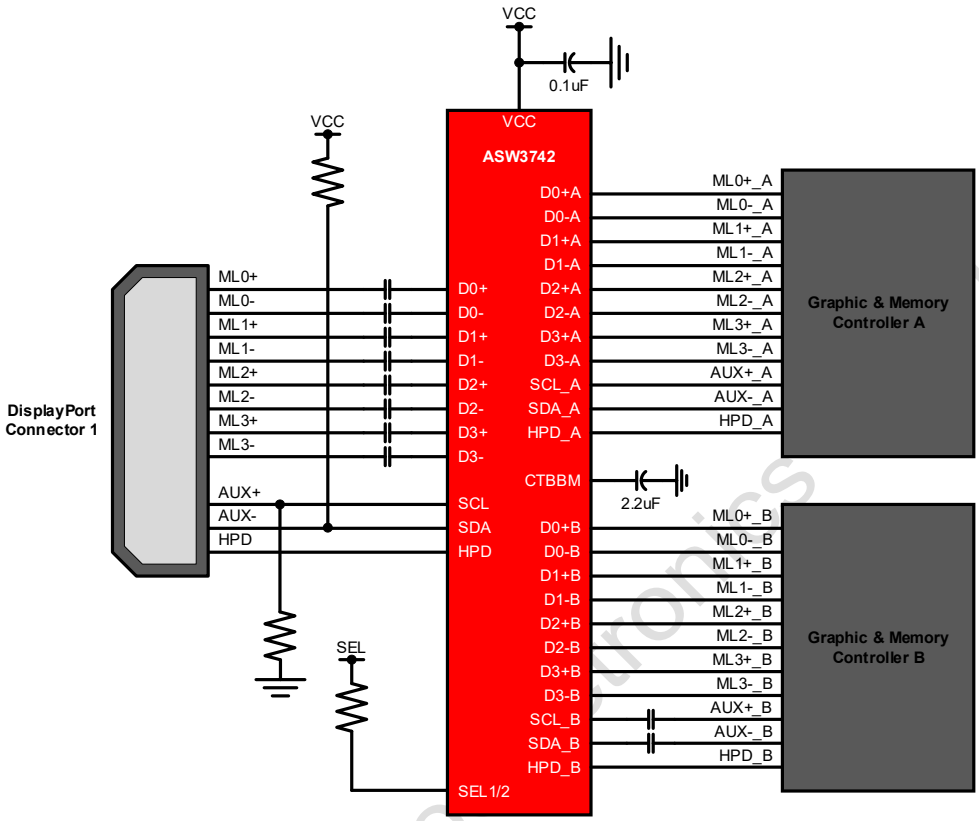
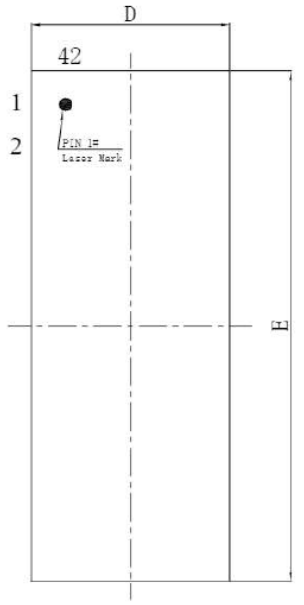


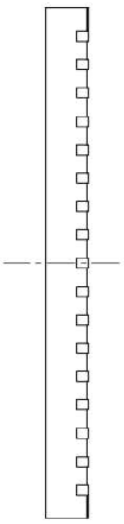
Figure 26，DP Application Diagram

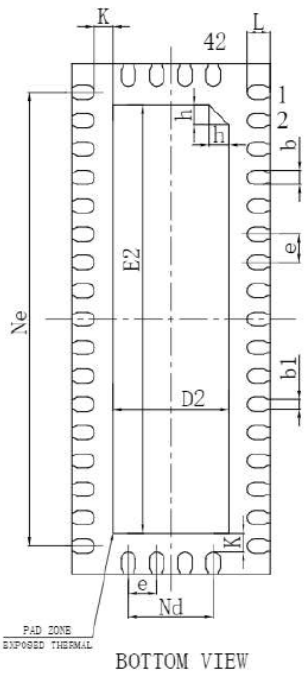
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PACKAGE OUTLINES (QFN42L-3.5x9.0x0.75)



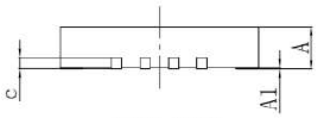
TOP VIEW





BOTTOM VIEW

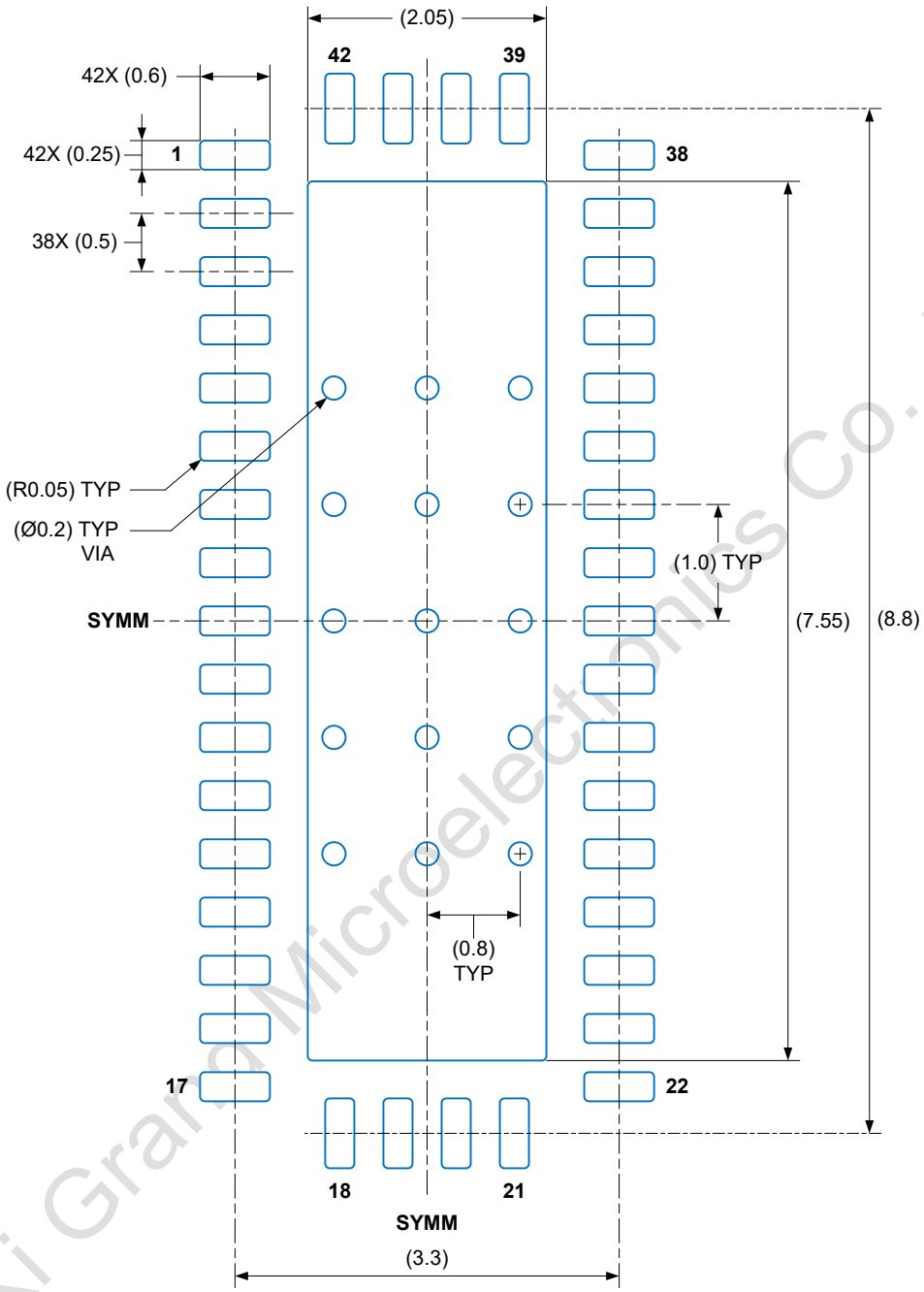
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.20	0.25	0.30
b1	0.18REF		
c	0.203REF		
D	3.40	3.50	3.60
D2	1.95	2.05	2.15
e	0.50BSC		
Nd	1.50BSC		
E	8.90	9.00	9.10
E2	7.45	7.55	7.65
Ne	8.00BSC		
L	0.35	0.40	0.45
h	0.30	0.35	0.40
K	0.325REF		



SIDE VIEW

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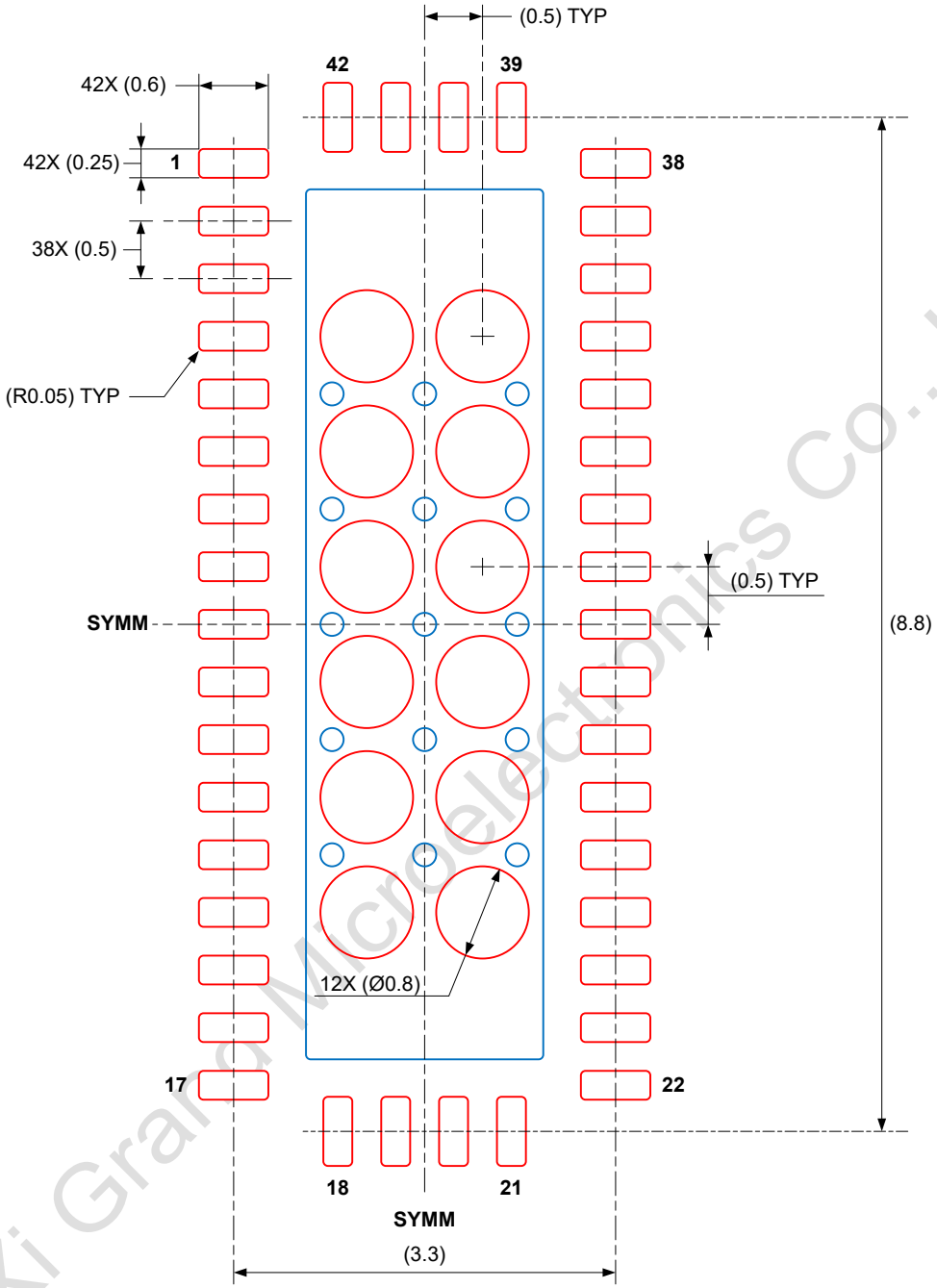
LAND PATTERN EXAMPLE



Notes:
1. All dimensions are in millimeters.
2. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

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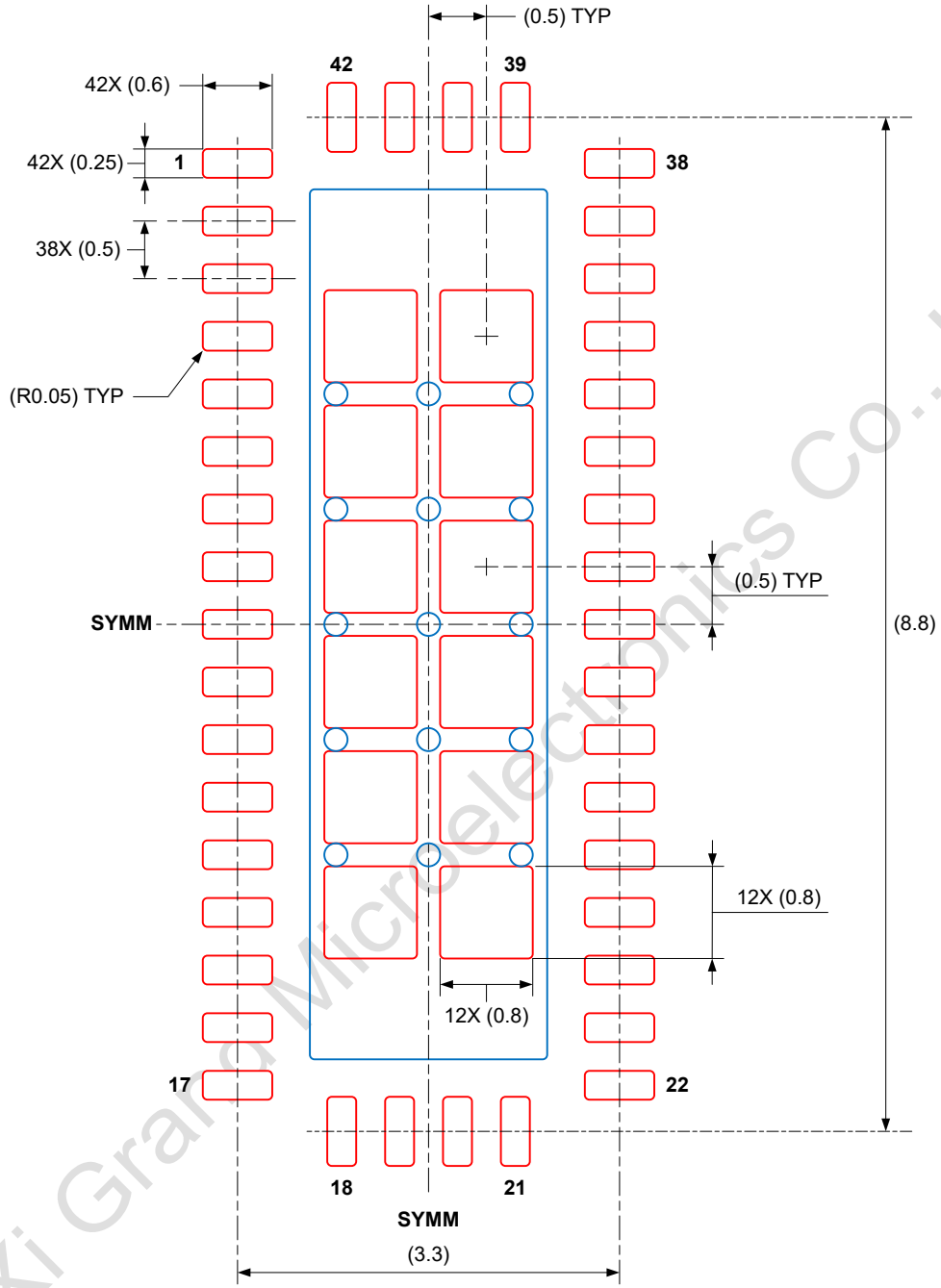
SOLDER PASTE EXAMPLE 1



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Notes:
3. All dimensions are in millimeters.

SOLDER PASTE EXAMPLE 2



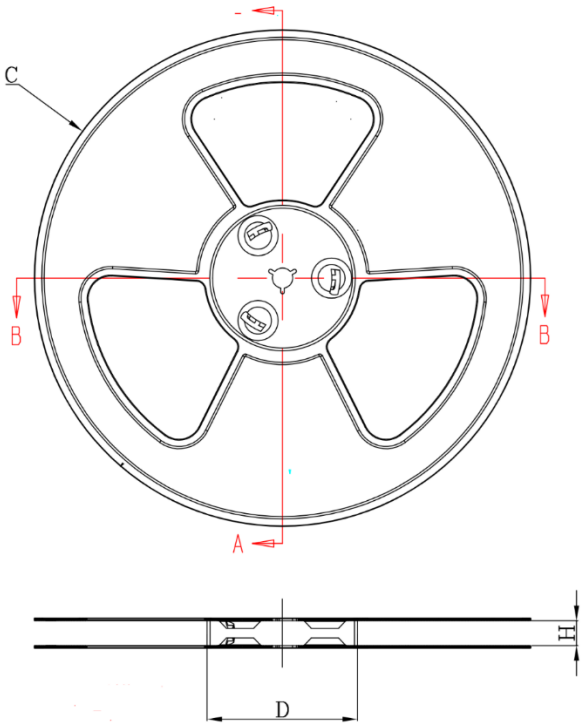
Notes:
4. All dimensions are in millimeters.

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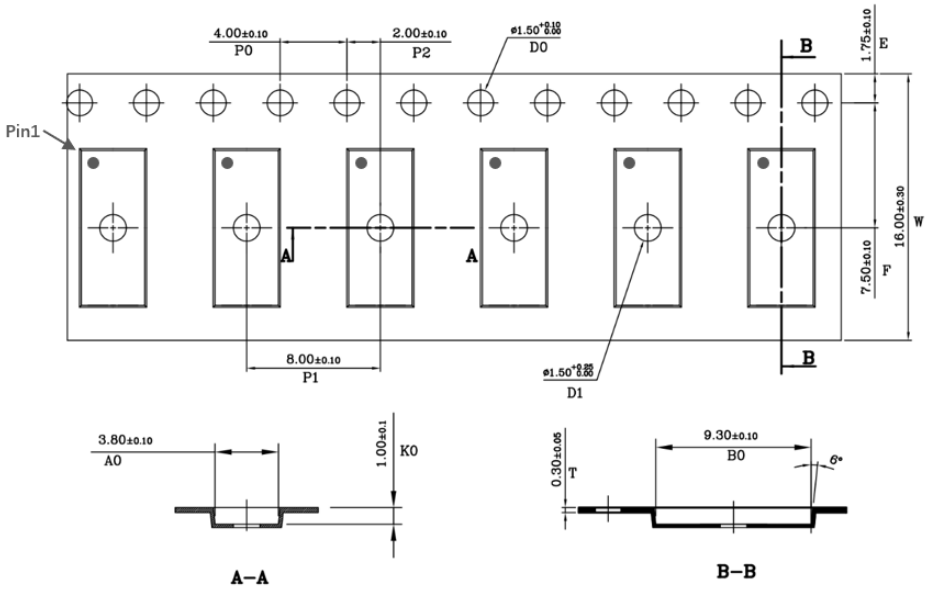
TAPE AND REEL INFORMATION

REEL

尺 寸 规 格 (UNIT:mm)									
项 目	H	D	C						
标 准	$16.50^{+0.4}_{-0.4}$	ø100±2.0	ø330±1.0						



TAPE



Note:
1. All Dimension Unit in mm.

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PRODUCT ORDERING INFORMATIONS

Part Number	Package Drawing	Operating Temperature	Package Information	Moisture Sensitivity Level	Package Method
ASW3742QNG		-40°C to +105°C	QFN42L-3.5x9.0	MSL-3	Tape & Reel (3000 Per Tape)

Note: (1) XXXXXXXXX means wafer lot ID. (2) YY means year, and WW means week. (3) ZZ means manufacturer code.

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