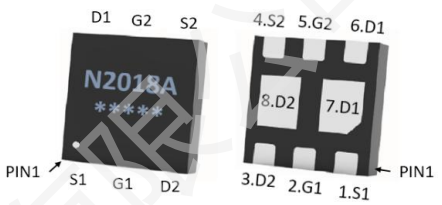
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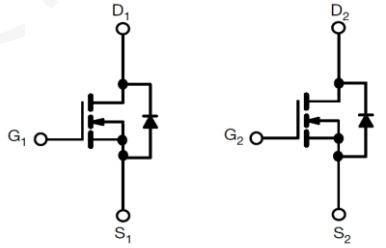
The LWN2018AD2D uses trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications. The package form is DFN2*2-6L, which accords with the ROHS standard and Halogen Free standard.

V_{DSS}	20	V
I_D	5.0	A
P_D	1.7	W
$R_{DS(ON)\ TYPE}$	12	mΩ

Marking and Pin Assignment



Inner Equivalent Principium Chart



Features:

- Fast Switching
- Low Gate Charge and $R_{DS(ON)}$
- Low Reverse transfer capacitances

Applications:

- DC-DC Converter
- Portable Equipment
- Power Management

100% DVDS Tested

100% Avalanche Tested

RoHS HF

Package Marking and Ordering Information:

Marking	Part Number	Package	Packing	Qty.
N2018A/D.C.	LWN2018AD2D	DFN2*2-6L	Reel	3000 Pcs

Absolute Maximum Ratings:

Symbol	Parameter		Value	Units
V_{DSS}	Drain-to-Source Voltage		20	V
I_D	Continuous Drain Current	T_A=25℃	5.0	A
	Continuous Drain Current	T_A=100℃	3.1	A
I_{DM}[a1]	Pulsed Drain Current		20	A
E_{AS}[a2]	Single pulse avalanche energy		25	mJ
V_{GS}	Gate-to-Source Voltage		±10	V
P_D	Power Dissipation		1.7	W
T_J, T_{STG}	Operating Junction and Storage Temperature Range		150, -55 to 150	℃
T_L	Maximum Temperature for Soldering		260	℃

Thermal Characteristics:

Symbol	Parameter	Value	Units
$R_{\theta JA}$[a3]	Thermal Resistance, Junction-to-Ambient	73.5	℃/W

Electrical Characteristic (T_J = 25 °C, unless otherwise specified):

Static Characteristics						
Symbol	Parameter	Test Conditions	Value			Units
			Min.	Typ.	Max.	
V_{DSS}	Drain to Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	20	--	--	V
I_{DSS}	Drain to Source Leakage Current	V_{DS}=20V, V_{GS}=0V	--	--	1.0	μA
$I_{GSS(F)}$	Gate to Source Forward Leakage	V_{GS}=+10V, V_{DS}=0V	--	--	100	nA
$I_{GSS(R)}$	Gate to Source Reverse Leakage	V_{GS}=-10V, V_{DS}=0V	--	--	-100	nA
$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250μA	0.4	0.7	1.0	V
$R_{DS(ON)1}$	Drain-to-Source On-Resistance	V_{GS}=4.5V, I_D=5.0A	--	12	15	mΩ
$R_{DS(ON)2}$	Drain-to-Source On-Resistance	V_{GS}=2.5V, I_D=3.0A	--	16	24	mΩ

Dynamic Characteristics						
Symbol	Parameter	Test Conditions	Value			Units
			Min.	Typ.	Max.	
C_{iss}	Input Capacitance	V_{GS} =0V V_{DS} =10V f =1.0MHz	--	609	--	pF
C_{oss}	Output Capacitance		--	115	--	
C_{rss}	Reverse Transfer Capacitance		--	105	--	
R_G	Gate resistance	V_{GS}=0V,V_{DS}=0V,f=1MHz	--	2.4	--	Ω

Resistive Switching Characteristics						
Symbol	Parameter	Test Conditions	Value			Units
			Min.	Typ.	Max.	
$t_{d(ON)}$	Turn-on Delay Time	I_D =5.0A V_{DS} =10V V_{GS} =4.5V R_G =3.0Ω	--	10	--	ns
t_r	Rise Time		--	23	--	
$t_{d(OFF)}$	Turn-Off Delay Time		--	16	--	
t_f	Fall Time		--	6.0	--	
Q_g	Total Gate Charge	V_{GS} =4.5V V_{DS} =10V I_D =5.0A	--	8.9	--	nC
Q_{gs}	Gate to Source Charge		--	0.9	--	
Q_{gd}	Gate to Drain Charge		--	2.8	--	

Source-Drain Diode Characteristics						
Symbol	Parameter	Test Conditions	Value			Units
			Min.	Typ.	Max.	
I_S	Diode Forward Current	T_A=25 °C	--	--	5.0	A
V_{SD}	Diode Forward Voltage	I_S=5.0A, V_{GS}=0V	--	--	1.2	V

a1：Repetitive rating; pulse width limited by maximum junction temperature

a2：V_{DD}=15V, L=0.1mH, R_G=25Ω, Starting T_J=25 ℃

a3：Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm^2 (one layer, 70 μm thick) copper area for drain connection.

Characteristics Curve：

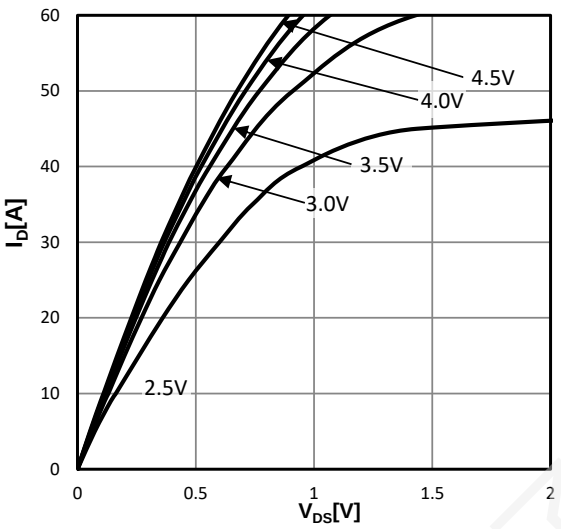
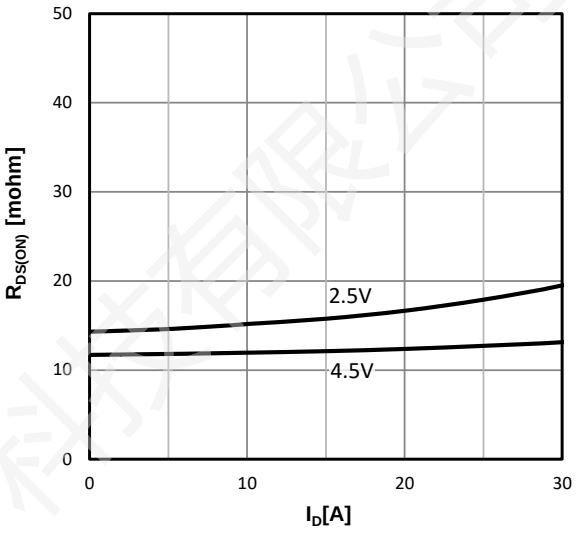
Figure 1: Typ. output characteristics	Figure 2: Typ. drain-source on resistance
	
$I_D=f(V_{DS})$, T_j=25 °C; parameter: V_{GS}	$R_{DS(on)}=f(I_D)$, T_j=25 °C; parameter: V_{GS}

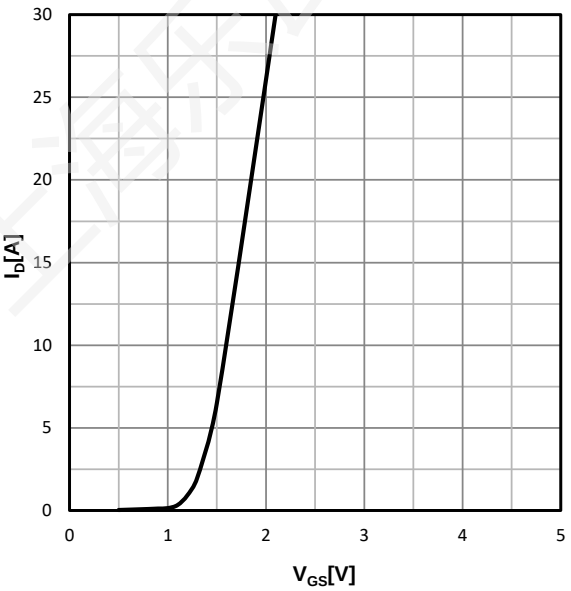
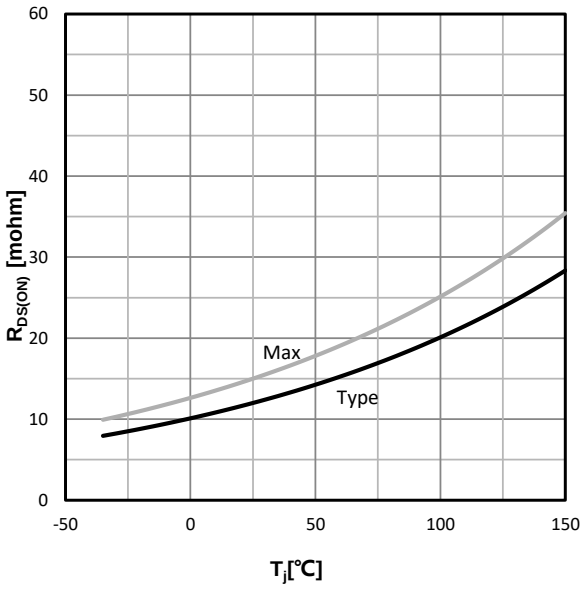
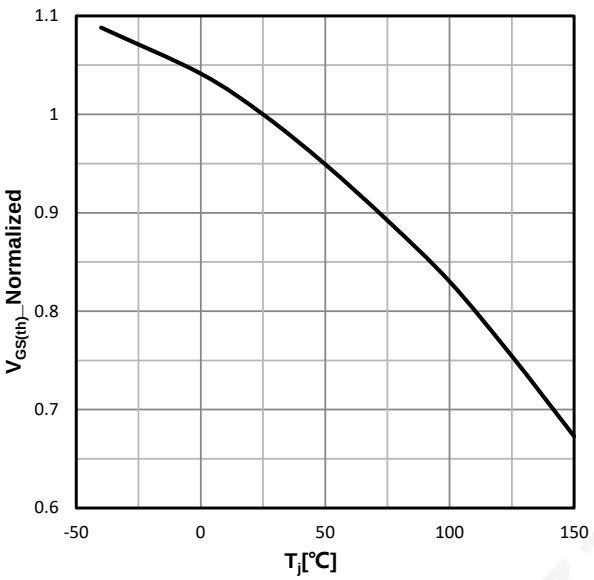
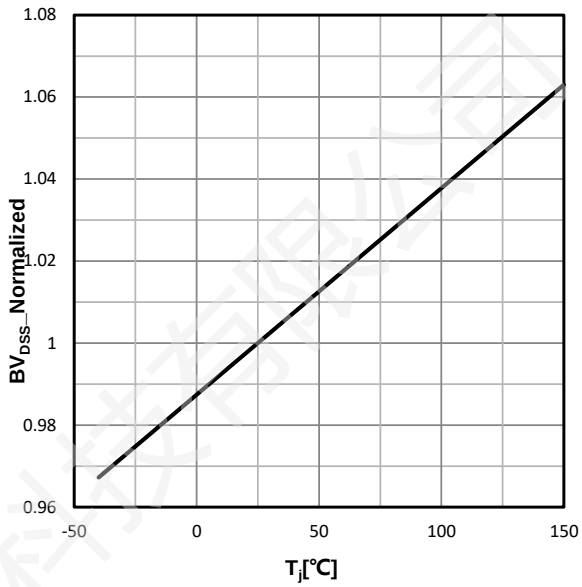
Figure 3: Typ. transfer characteristics	Figure 4: drain-source on resistance
	
$I_D=f(V_{GS})$, $\|V_{DS}\|>2\|I_D\|R_{DS}(on)max$;	$R_{DS(on)}=f(T_j)$, I_D=5.0A, V_{GS}=4.5V;

Figure 5: Typ. gate threshold voltage



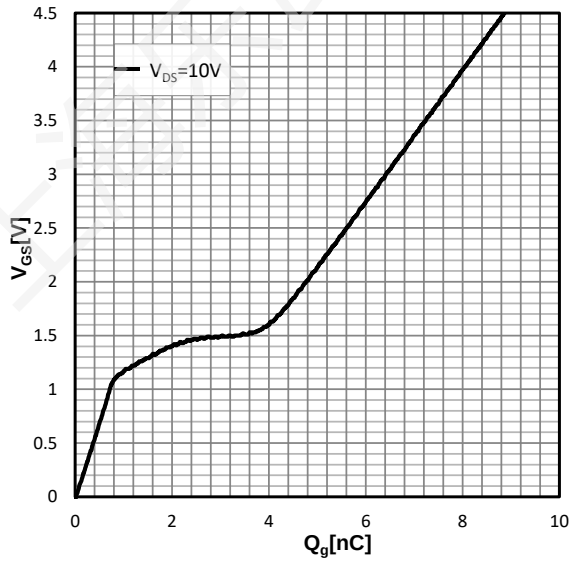
$V_{GS}=f(T_j)$,$V_{GS}=V_{DS,}I_D=250\mu A$;

Figure 6: Drain-source breakdown voltage



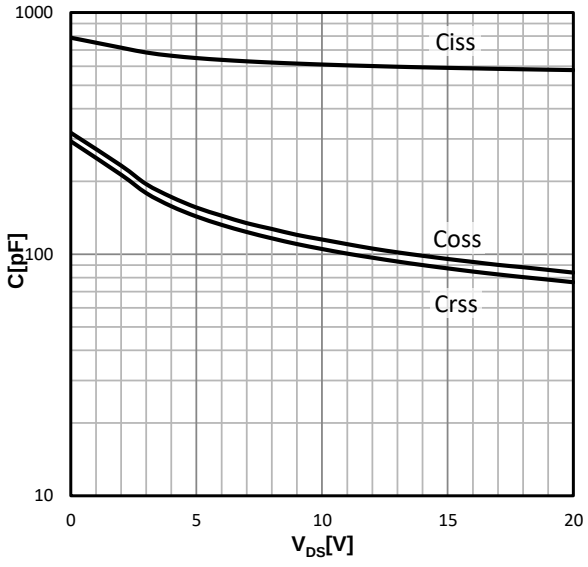
$V_{BR(DSS)}=f(T_j)$; $I_D=250\mu A$;

Figure 7: Typ. gate charge



$V_{GS}=f(Q_g)$, $I_D=5.0A$, $T_j=25$ °C; parameter: V_{DS}

Figure 8: Typ. Capacitances



$C=f(V_{DS})$; $V_{GS}=0V$; f=1.0 MHz;

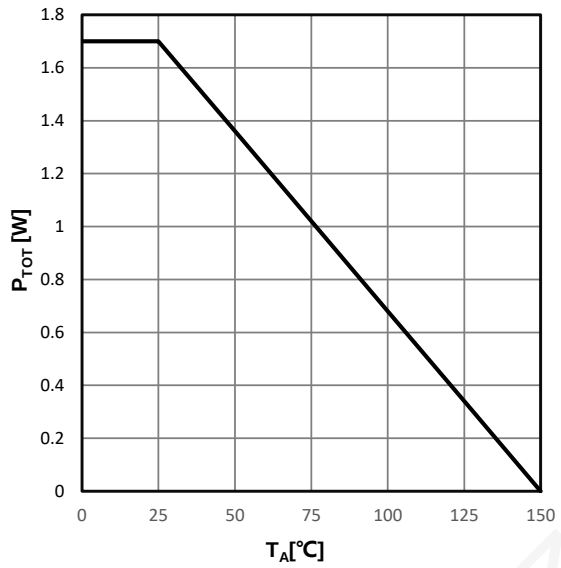
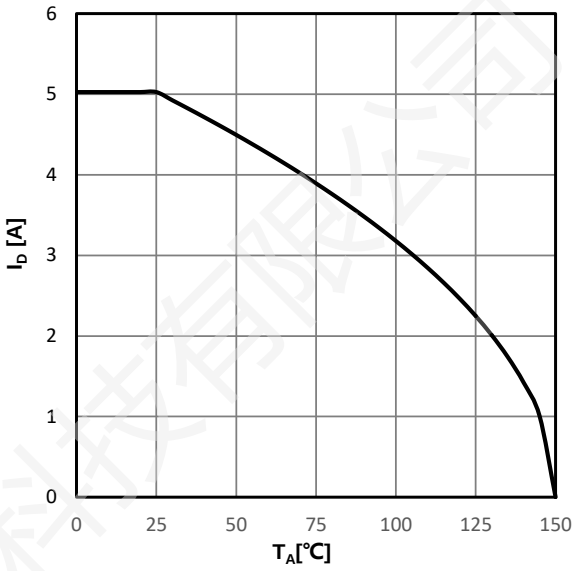
Figure 9: Power dissipation	Figure 10:Drain current
	
$P_{tot}=f(T_A)$;	$I_D=f(T_A)$;

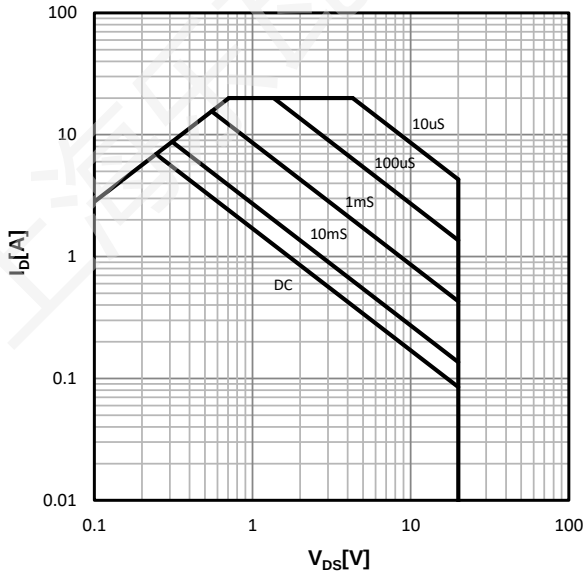
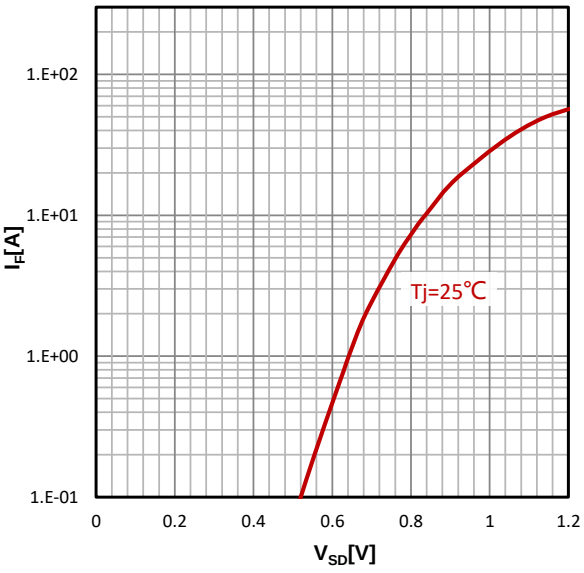
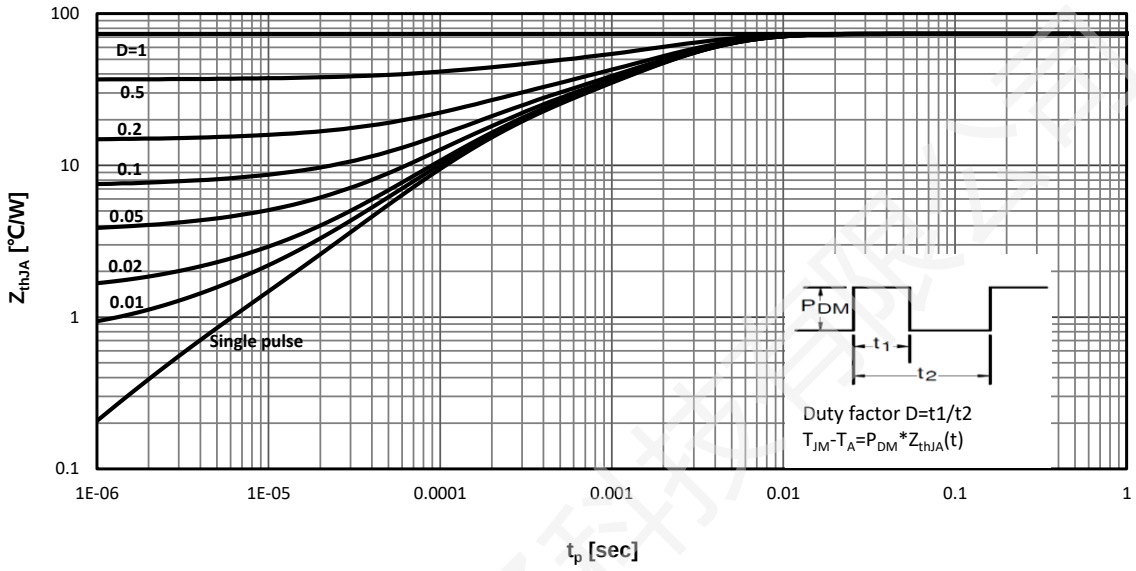
Figure 11: Safe operating area	Figure 12: Typ. forward characteristics
	
$I_D=f(V_{DS})$; T_A=25 °C; D=0; parameter: tp	$I_F=f(V_{SD})$;

Figure 13: Max. Transient Thermal Impedance



$Z_{thJA}=f(t_p)$; parameter: D

Test Circuit & Waveform:

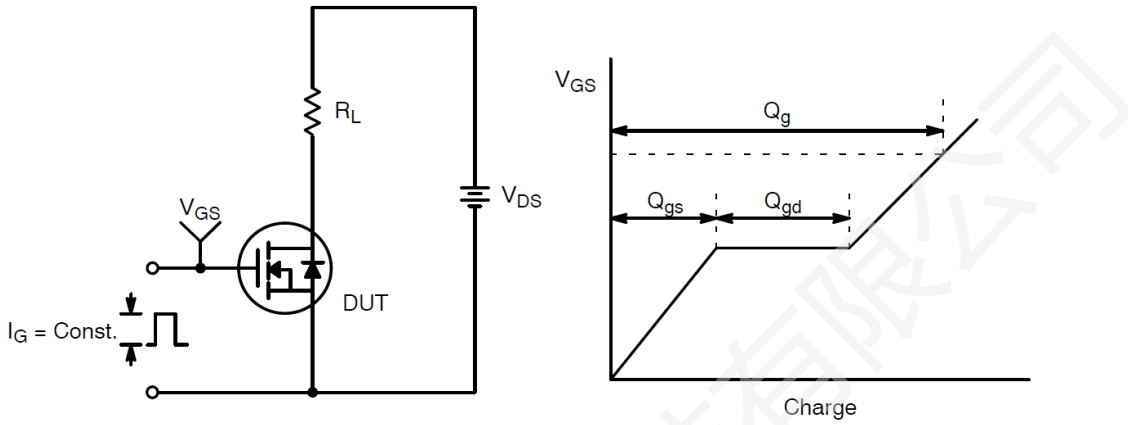


Figure 14: Gate Charge Test Circuit & Waveform

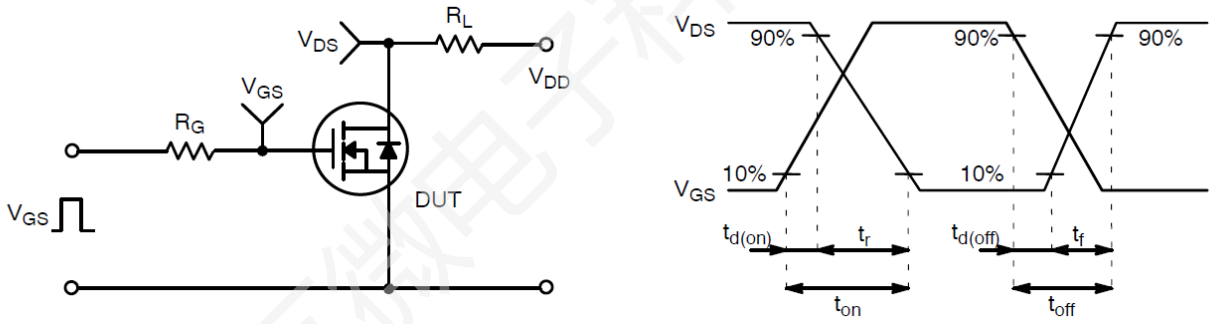


Figure 15: Resistive Switching Test Circuit & Waveforms

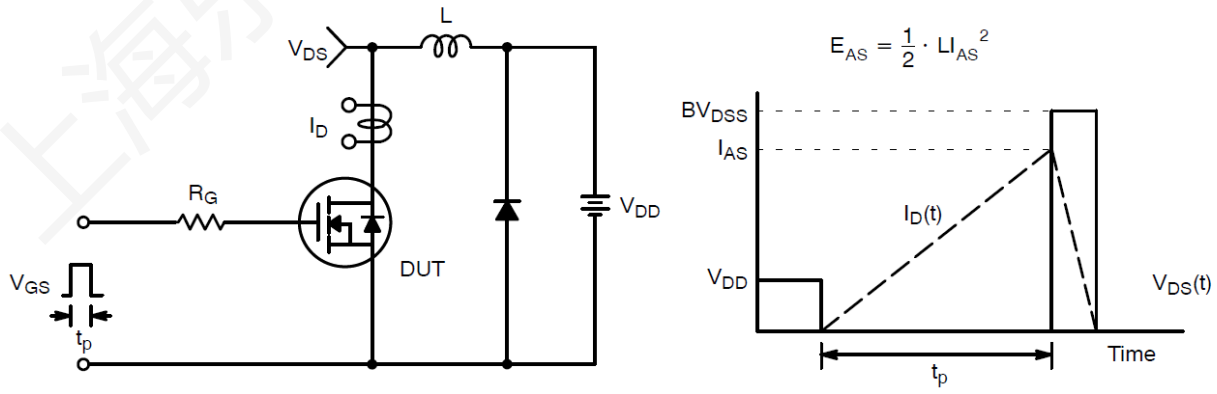
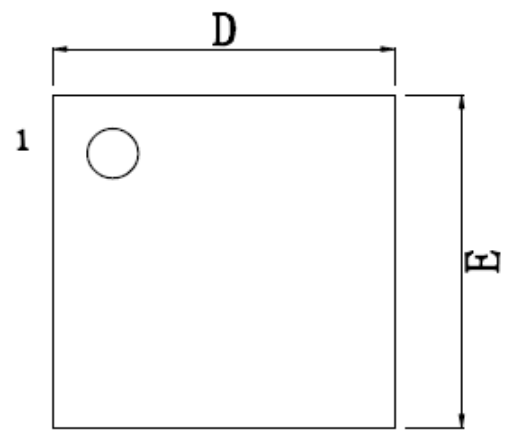
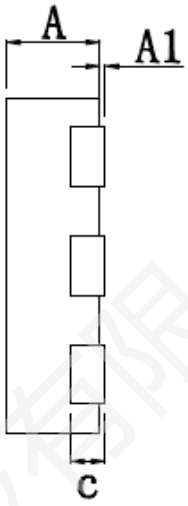
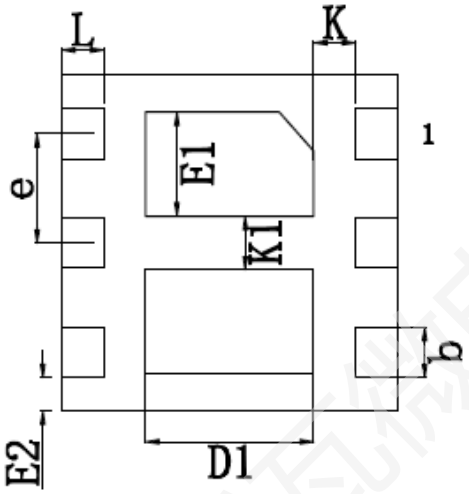


Figure 16: Unclamped Inductive Switching Test Circuit & Waveforms

Package Outline:







Symbol	MILIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	——	0.05
b	0.25	0.30	0.35
b1	0.15	0.20	0.25
c	0.203 TYP		
D	1.95	2.00	2.05
D1	0.90	1.00	1.10
E	1.95	2.00	2.05
E1	0.52	0.62	0.72
E2	0.20 REF		
Nd	1.30 BSC		
e	0.65 BSC		
K	0.25 REF		
K1	0.32 REF		
L	0.20	0.25	0.30

上海乐瓦微电子科技有限公司

Revision History:

Revison	Date	Descriptions
Rev 1.1	July.2025	Initial Version

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