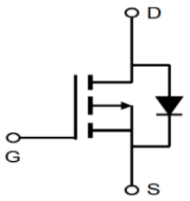
General Description:

The LWP2003AD5 uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications. The package form is PDFN5*6-8L, which accords with the ROHS standard and Halogen Free standard.

V_{DSS}	-20	V
I_D	-80	A
P_D	139	W
$R_{DS(ON)\ TYPE}$	2.0	mΩ

Marking and Pin Assignment

Inner Equivalent Principium Chart



Features:

- Fast Switching
- Low Gate Charge and $R_{DS(ON)}$
- Low Reverse transfer capacitances

Applications:

- Battery switching application
- Hard switched and high frequency circuits
- Power Management

100% DVDS Tested

100% Avalanche Tested

Package Marking and Ordering Information:

Marking	Part Number	Package	Packing	Qty.
P2003A/LW D5/D.C.	LWP2003AD5	PDFN5*6-8L	Reel	5000 Pcs

Absolute Maximum Ratings:

Symbol	Parameter		Value	Units
V_{DSS}	Drain-to-Source Voltage		-20	V
I_D	Continuous Drain Current	T_C=25℃	-80	A
	Continuous Drain Current	T_C=100℃	-51	A
I_{DM}[a1]	Pulsed Drain Current		-320	A
E_{AS}[a2]	Single pulse avalanche energy		271	mJ
V_{GS}	Gate-to-Source Voltage		±10	V
P_D	Power Dissipation		139	W
T_J, T_{STG}	Operating Junction and Storage Temperature Range		150, -55 to 150	℃
T_L	Maximum Temperature for Soldering		260	℃

Thermal Characteristics:

Symbol	Parameter	Value	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	0.9	℃/W
$R_{\theta JA}$[a3]	Thermal Resistance, Junction-to-Ambient	45	℃/W

Electrical Characteristic (T_J = 25 °C, unless otherwise specified):

Static Characteristics						
Symbol	Parameter	Test Conditions	Value			Units
			Min.	Typ.	Max.	
V_{DSS}	Drain to Source Breakdown Voltage	V_{GS}=0V, I_D=-250μA	-20	--	--	V
I_{DSS}	Drain to Source Leakage Current	V_{DS}=-20V, V_{GS}=0V	--	--	-1.0	μA
$I_{GSS(F)}$	Gate to Source Forward Leakage	V_{GS}=-10V, V_{DS}=0V	--	--	-100	nA
$I_{GSS(R)}$	Gate to Source Reverse Leakage	V_{GS}=+10V, V_{DS}=0V	--	--	100	nA
$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=-250μA	-0.45	-0.6	-1.0	V
$R_{DS(ON)1}$	Drain-to-Source On-Resistance	V_{GS}=-4.5V, I_D=-20A	--	2.0	2.5	mΩ
$R_{DS(ON)2}$	Drain-to-Source On-Resistance	V_{GS}=-2.5V, I_D=-16A	--	2.8	3.5	mΩ
$R_{DS(ON)3}$	Drain-to-Source On-Resistance	V_{GS}=-1.8V, I_D=-12A	--	4.5	5.5	mΩ

Dynamic Characteristics						
Symbol	Parameter	Test Conditions	Value			Units
			Min.	Typ.	Max.	
C_{iss}	Input Capacitance	V_{GS} =0V V_{DS} =-10V f =1.0MHz	--	8071	--	pF
C_{oss}	Output Capacitance		--	2029	--	
C_{rss}	Reverse Transfer Capacitance		--	1866	--	
R_G	Gate resistance	V_{GS}=0V,V_{DS}=0V,f=1MHz	--	7.3	--	Ω

Resistive Switching Characteristics						
Symbol	Parameter	Test Conditions	Value			Units
			Min.	Typ.	Max.	
$t_{d(ON)}$	Turn-on Delay Time	I_D =-10A V_{DS} =-10V V_{GS} =-4.5V R_G =3.0Ω	--	16	--	ns
t_r	Rise Time		--	38	--	
$t_{d(OFF)}$	Turn-Off Delay Time		--	360	--	
t_f	Fall Time		--	210	--	
Q_g	Total Gate Charge	V_{GS} =-4.5V V_{DS} =-10V I_D =-12A	--	111	--	nC
Q_{gs}	Gate to Source Charge		--	10	--	
Q_{gd}	Gate to Drain Charge		--	38	--	

Source-Drain Diode Characteristics						
Symbol	Parameter	Test Conditions	Value			Units
			Min.	Typ.	Max.	
I_S	Diode Forward Current	T_C =25 °C	--	--	-80	A
V_{SD}	Diode Forward Voltage	I_S=-20A, V_{GS}=0V	--	--	-1.2	V

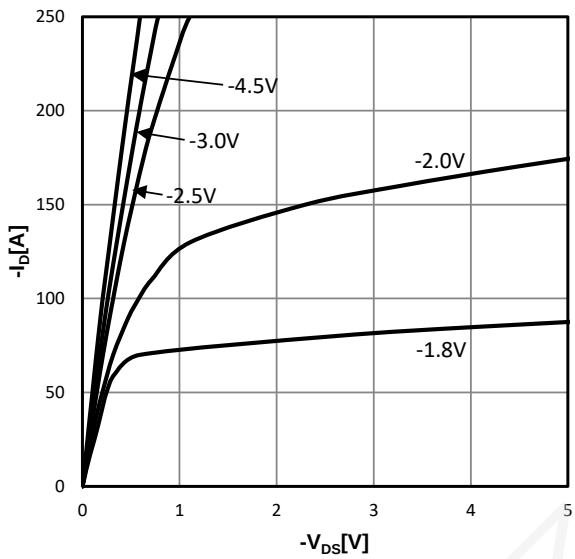
a1：Repetitive rating; pulse width limited by maximum junction temperature

a2：V_{DD}=-20V, L=0.1mH, R_G=25Ω, Starting T_J=25 ℃

a3：Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm^2 (one layer, 70 μm thick) copper area for drain connection.

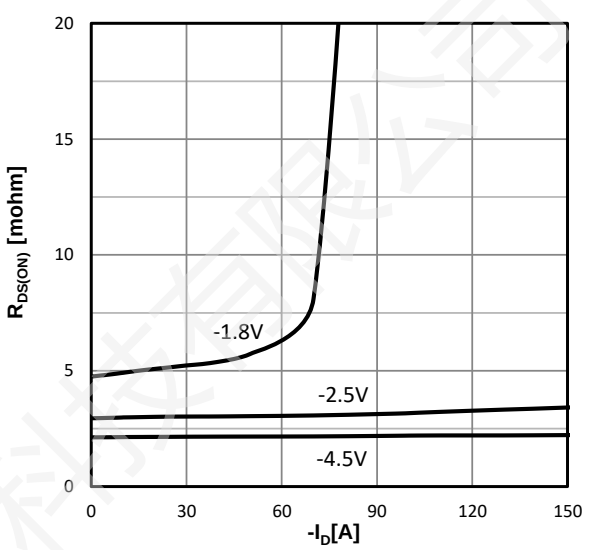
Characteristics Curve：

Figure 1: Typ. output characteristics



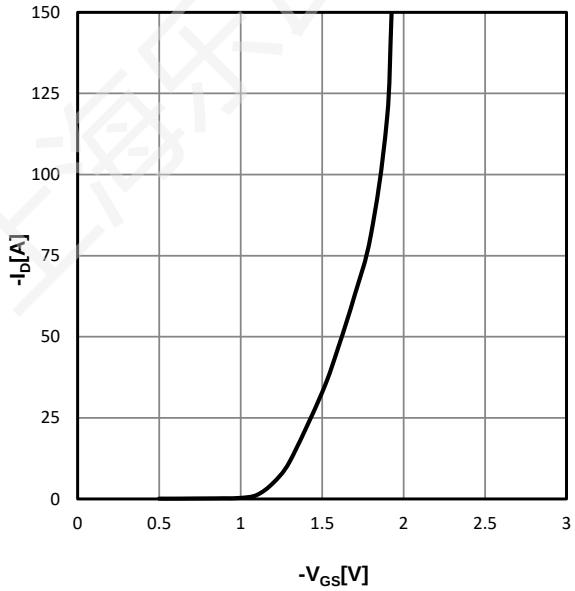
$I_D=f(V_{DS})$, T_j=25 °C; parameter: V_{GS}

Figure 2: Typ. drain-source on resistance



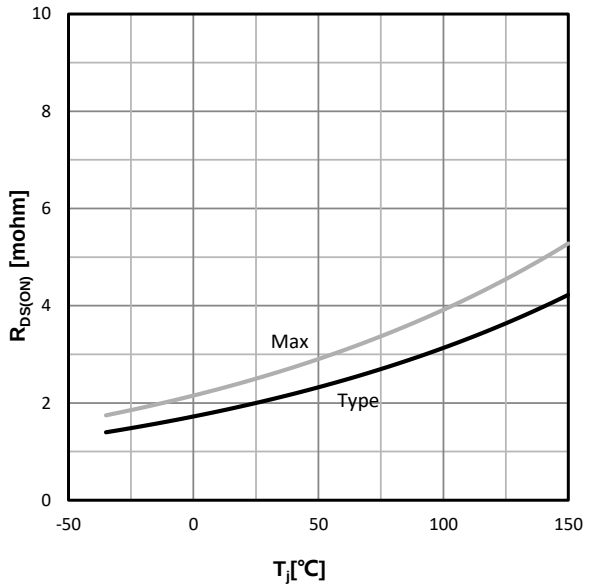
$R_{DS(on)}=f(I_D)$, T_j=25 °C; parameter: V_{GS}

Figure 3: Typ. transfer characteristics



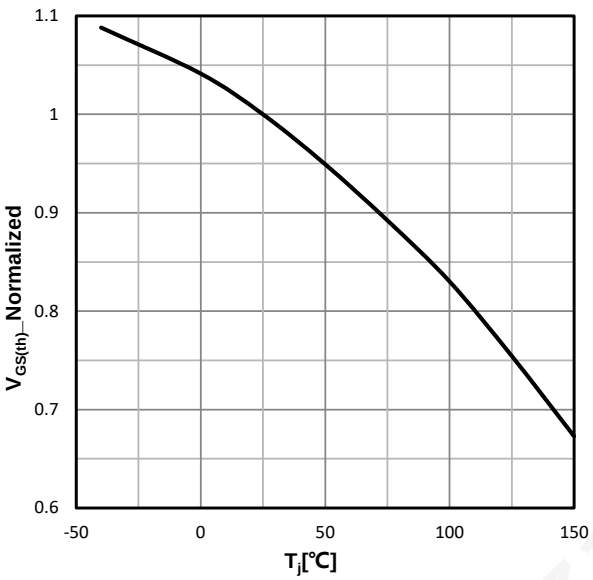
$I_D=f(V_{GS})$, $|V_{DS}|>2|I_D|R_{DS}(on)max$;

Figure 4: drain-source on resistance



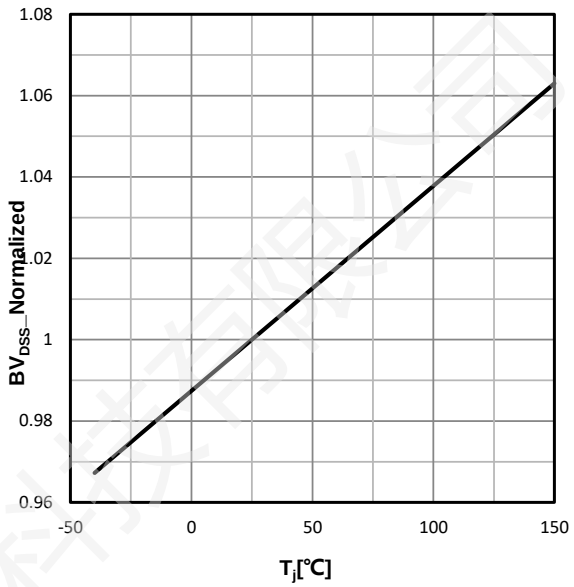
$R_{DS(on)}=f(T_j)$, I_D=-20A, V_{GS}=-4.5V;

Figure 5: Typ. gate threshold voltage



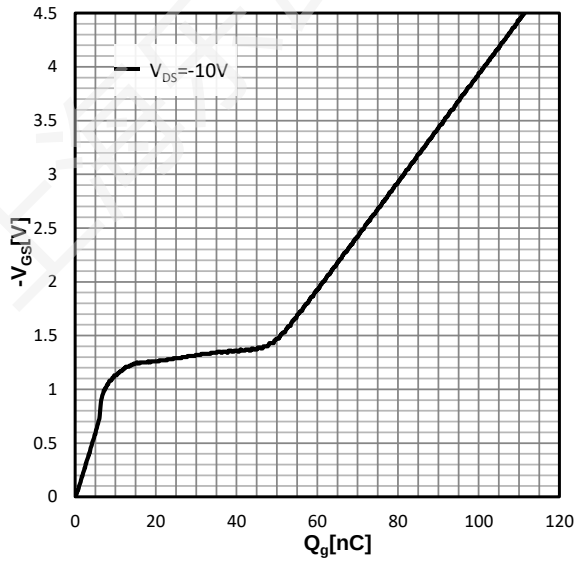
$V_{GS}=f(T_j)$, $V_{GS}=V_{DS,}$ I_D=-250μA;

Figure 6: Drain-source breakdown voltage



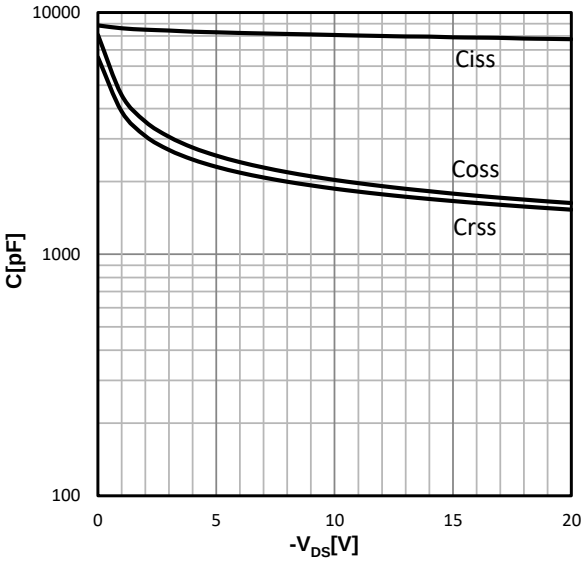
$V_{BR(DSS)}=f(T_j)$; I_D=-250μA;

Figure 7: Typ. gate charge



$V_{GS}=f(Q_g)$, I_D=-12A, T_j=25 °C; parameter: V_{DS}

Figure 8: Typ. Capacitances



$C=f(V_{DS})$; V_{GS}=0V; f=1.0 MHz;

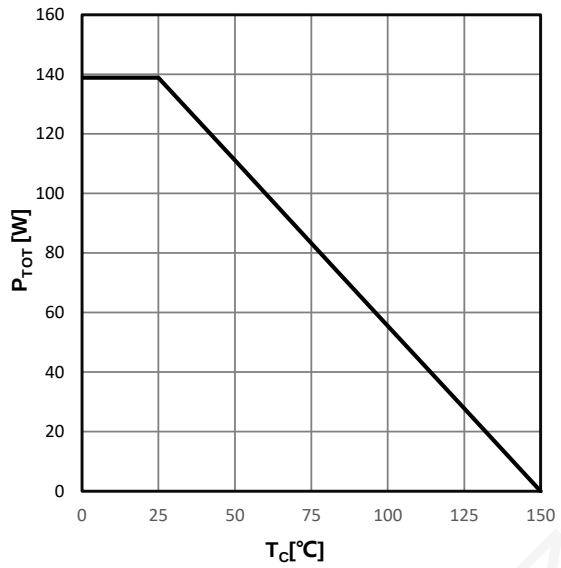
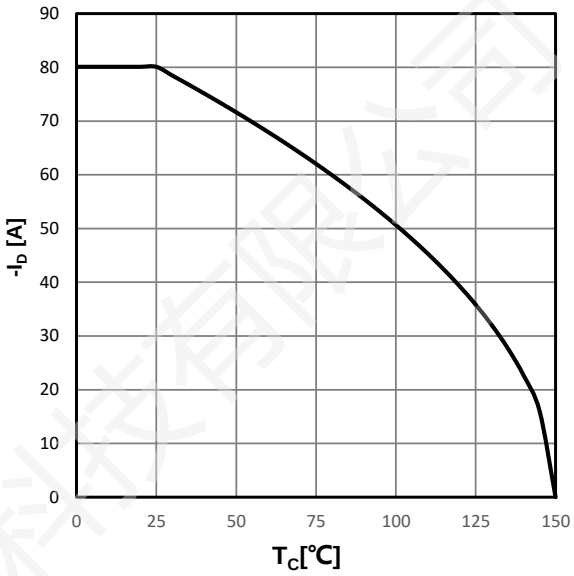
Figure 9: Power dissipation	Figure 10:Drain current
	
$P_{tot}=f(T_C)$;	$I_D=f(T_C)$;

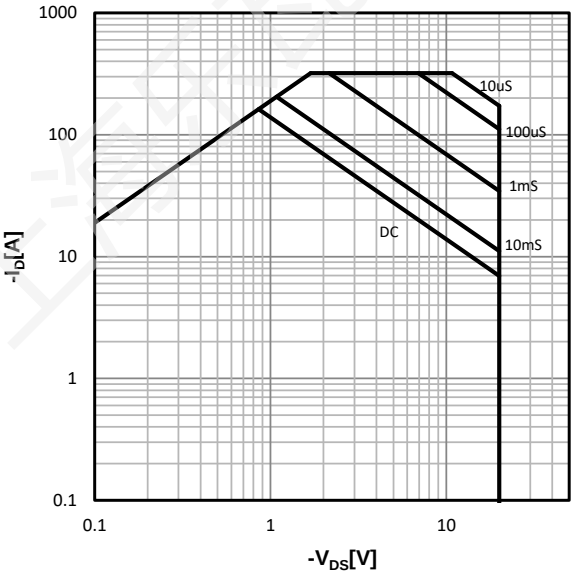
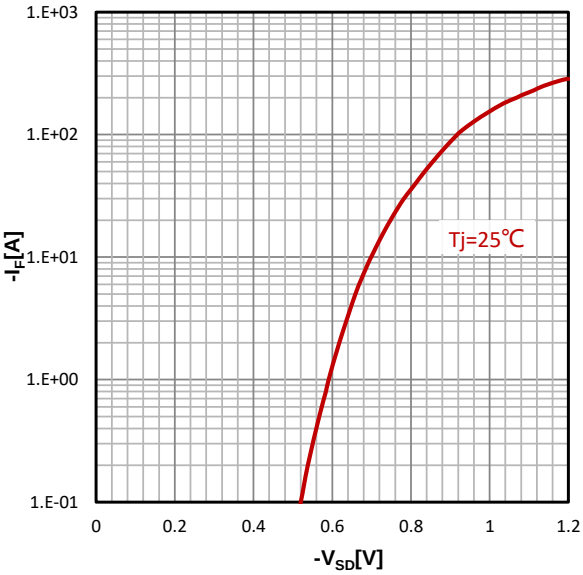
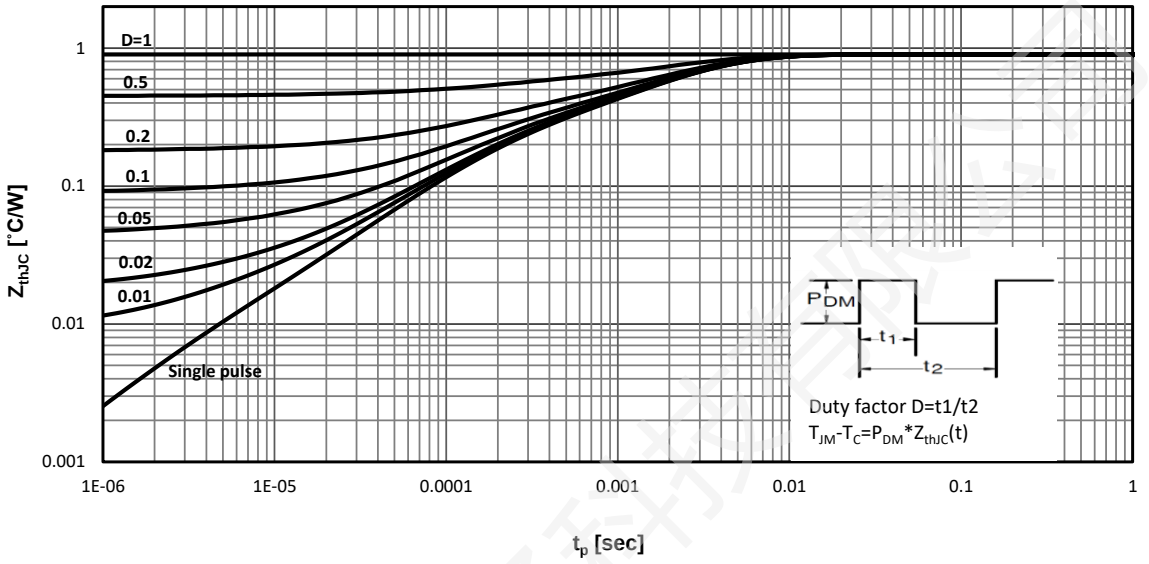
Figure 11: Safe operating area	Figure 12: Typ. forward characteristics
	
$I_D=f(V_{DS})$; T_C=25 °C; D=0; parameter: tp	$I_F=f(V_{SD})$;

Figure 13: Max. Transient Thermal Impedance



$Z_{thJC}=f(t_p)$; parameter: D

Test Circuit & Waveform:

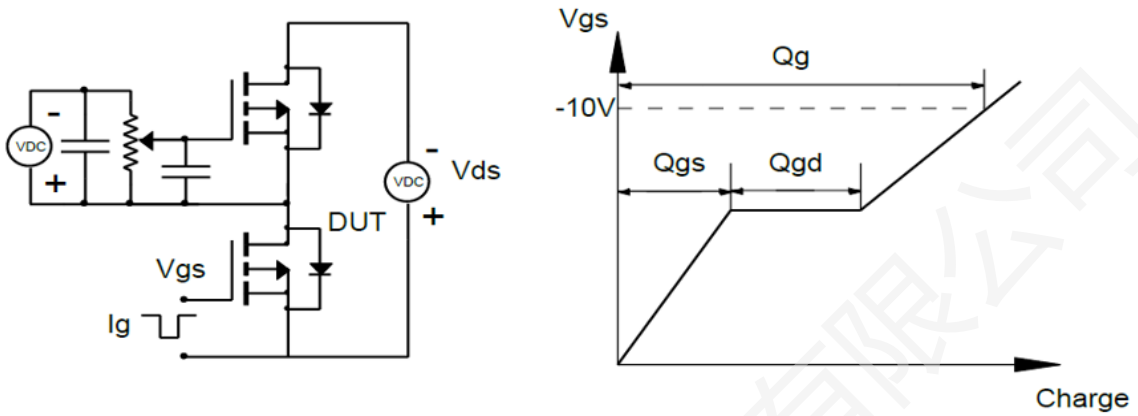


Figure 14: Gate Charge Test Circuit & Waveform

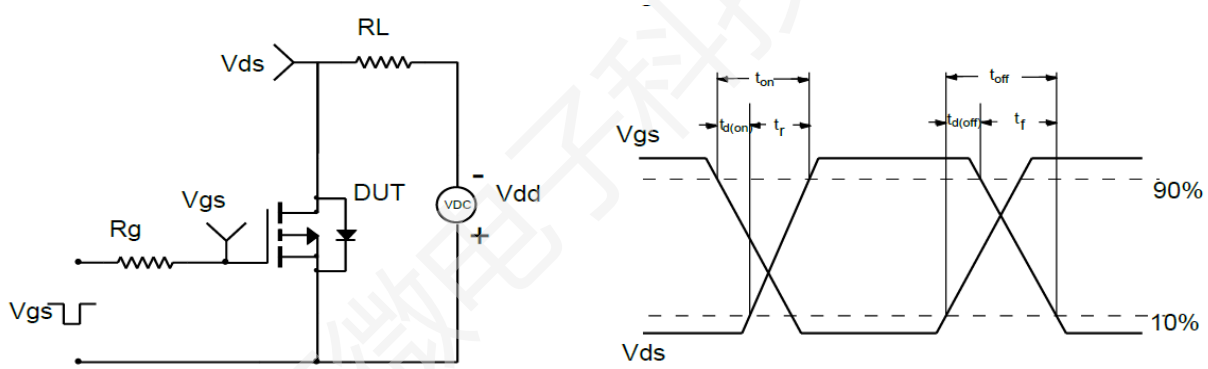


Figure 15: Resistive Switching Test Circuit & Waveforms

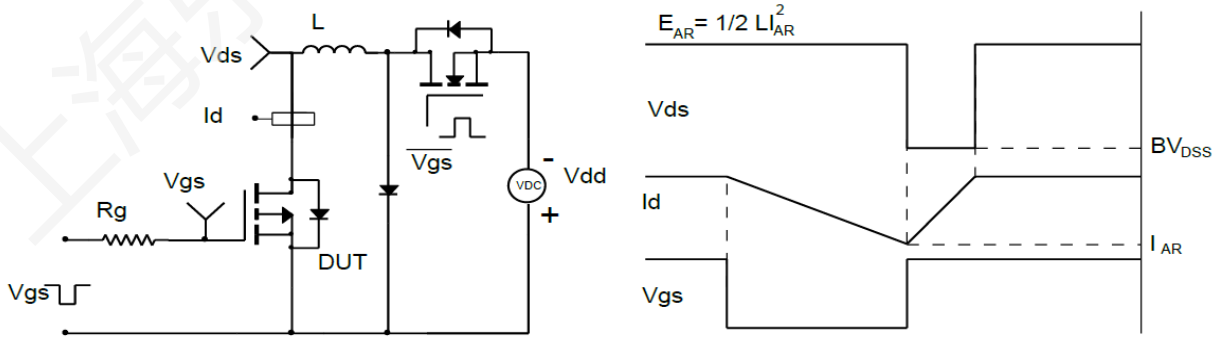
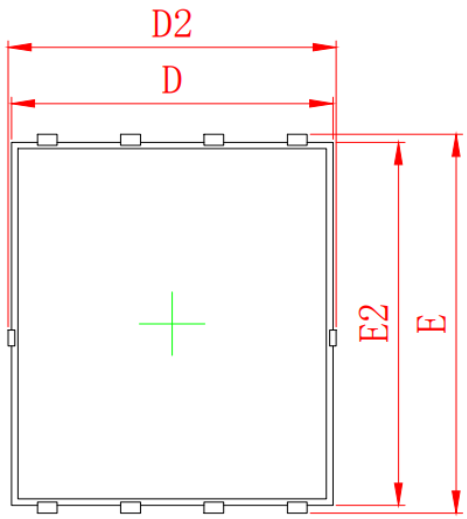
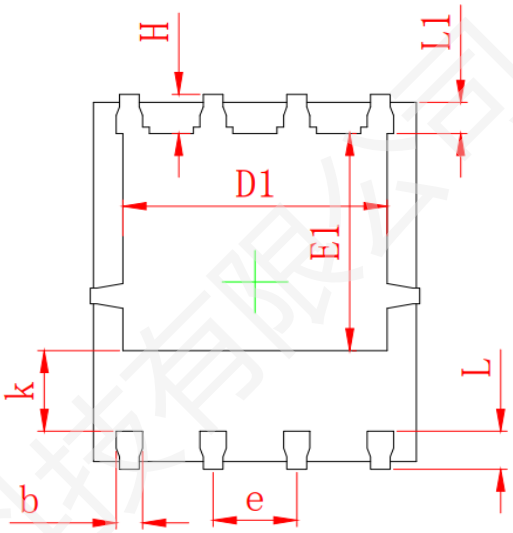
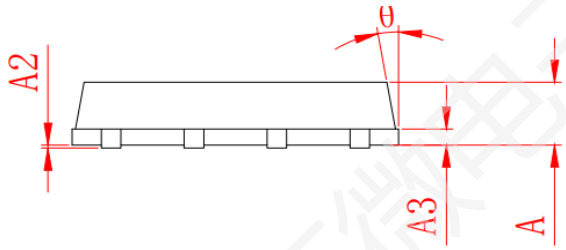


Figure 16: Unclamped Inductive Switching Test Circuit & Waveforms

Package Outline:







Symbol	MILLIMETER	
	Min	Max
A	0.900	1.200
A1	0.254 REF	
A2	0~0.050	
D	4.824	4.976
D1	3.910	4.110
D2	4.944	5.076
E	5.924	6.076
E1	3.375	3.575
E2	5.674	5.826
b	0.350	0.450
e	1.270 TYP	
L	0.534	0.686
L1	0.424	0.576
k	1.190	1.390
H	0.549	0.701
θ	8°	12°

Revision History:

Revison	Date	Descriptions
Rev 1.1	July.2025	Initial Version

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