PDFN5060 Plastic-Encapsulate MOSFETS

Features

- V_{DS}=80V
- I_D=110A
- $R_{DS(on)}$@V_{GS}=10V ＜ 5.2mΩ
- High density cell design for ultra low Rdson
- Advanced Split Gate Trench Technology
- Fast Switching Speedze

Drain-source Voltage
80 V
Drain Current
110 Ampere

Applications

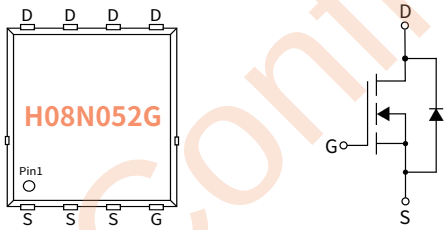
- DC-DC Converters
- Uninterruptible power supply
- Power switching application

PDFN5060

Mechanical Data

- Case: PDFN5060
  Molding compound meets UL 94V-0 flammability rating, RoHS-compliant,halogen-free
- Terminals: Solder plated, solderable per MIL-STD-750,Method 2026

Function Diagram



Ordering Information

PACKAGE	PACKAGE CODE	UNIT WEIGHT(g)	REEL(pcs)	BOX(pcs)	CARTON(pcs)	DELIVERY MODE
PDFN5060	R3	0.09	5000	10000	80000	13''

Maximum Ratings (Ta=25°C Unless otherwise specified)

PARAMETER	SYMBOL	UNIT	VALUE
Drain-source Voltage	V_{DS}	V	80
Gate-source Voltage	V_{GS}	V	±20
Drain Current	I_D	A	110
Pulsed Drain Current (1)	I_{DM}	A	440
Total Power Dissipation	P_D	W	120
Single pulse avalanche energy(2)	EAS	mJ	272
Junction temperature	T_J	°C	-55 ~+150
Storage temperature	T_{stg}	°C	-55 ~+150
Thermal Resistance Junction-to-Case	$R_{\theta JC}$	°C / W	1.04

Static Parameter Characteristics (Tj=25°C Unless otherwise specified)

PARAMETER	SYMBOL	Condition	UNIT	Min	Typ	Max
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}= 0V, I_D=250μA	V	80	—	—
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=80V, V_{GS}=0V	μA	—	—	1.0
Gate-Body Leakage Current	I_{GSS}	V_{GS}= ±20V, V_{DS}=0V	nA	—	—	±100
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D=250μA	V	2	3	4
Static Drain-Source On-Resistance (3)	$R_{DS(ON)}$	V_{GS}= 10V, I_D=20A	mΩ	—	4.2	5.2

Dynamic Parameters

PARAMETER	SYMBOL	Condition	UNIT	Min	Typ	Max
Input Capacitance	C_{iss}	V_{DS}=40V, V_{GS}=0V, f=1MHZ	pF	—	3818	—
Output Capacitance	C_{oss}			—	515	—
Reverse Transfer Capacitance	C_{rss}			—	21	—

Switching Parameters

PARAMETER	SYMBOL	Condition	UNIT	Min	Typ	Max
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=10V, V_{DD}=40V, I_D=50A ,R_{GEN}=3Ω	nS	—	17	—
Turn-on Rise Time	t_r		nS	—	39	—
Turn-off Delay Time	$t_{D(off)}$		nS	—	64	—
Turn-off fall Time	t_f		nS	—	42	—
Total Gate Charge	Q_g	V_{DS}=40V, I_D=50A V_{GS}=10V	nC	—	42	—
Gate-Source Charge	Q_{gs}		nC	—	15	—
Gate-Drain Charge	Q_{gd}		nC	—	20	—

Drian-Source Diode Characteristics

PARAMETER	SYMBOL	Condition	UNIT	Min	Typ	Max
Diode Forward Voltage	V_{SD}	I_S=110A, V_{GS}=0V	V	—	—	1.2
Maximum Body-Diode Continuous Current	I_S	—	A	—	—	110
Reverse Recovery time	T_{rr}	I_{SD}=110A di/dt=100A/us	nS	—	45	—
Reverse Recovery Charge	Q_{rr}		nC	—	56	—

Note :
(1)Repetitive Rating: Pulse width limited by maximum junction temperature.
(2)EAS condition : Tj=25°C ,VDD=40V,VG=10V,L=0.5mH,IAS=33A,Rg=25Ω.
(3)Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.

Ratings And Characteristics Curves (Ta=25°C Unless otherwise specified)

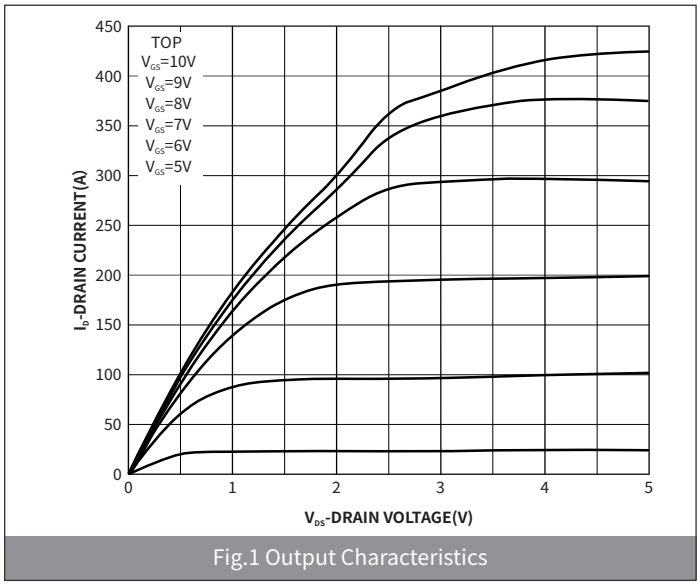


Fig.1 Output Characteristics

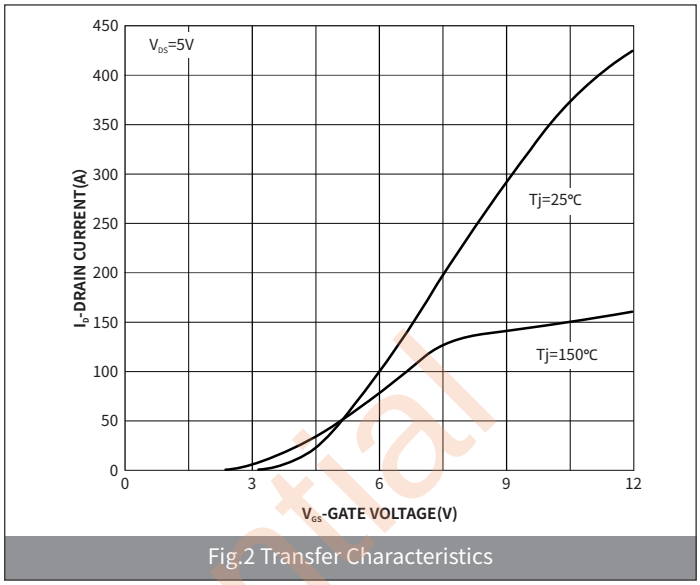


Fig.2 Transfer Characteristics

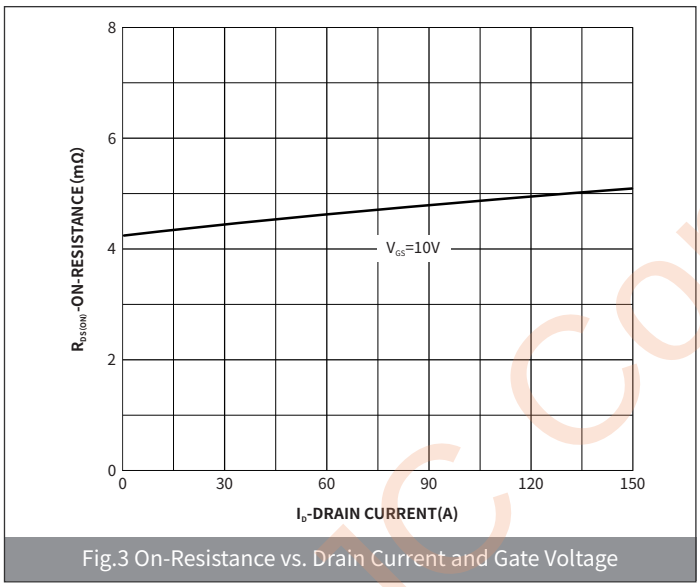


Fig.3 On-Resistance vs. Drain Current and Gate Voltage

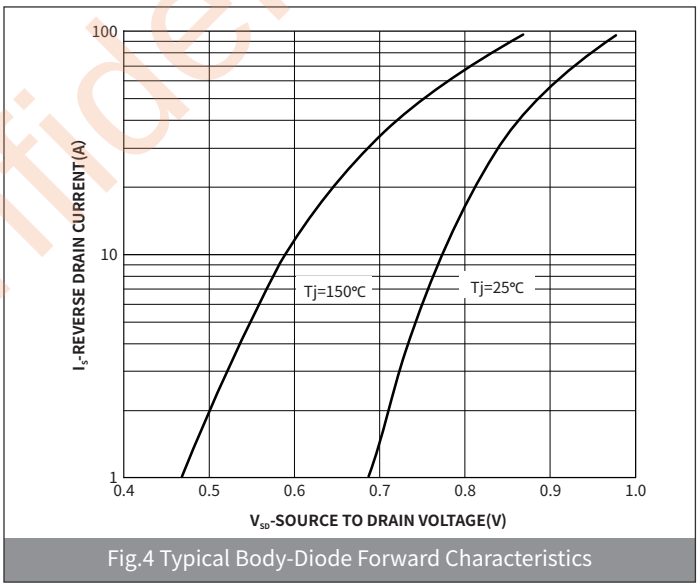


Fig.4 Typical Body-Diode Forward Characteristics

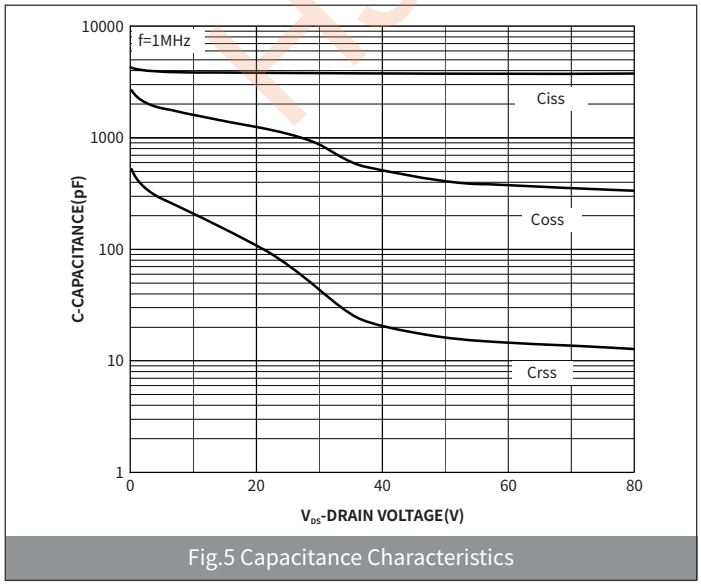


Fig.5 Capacitance Characteristics

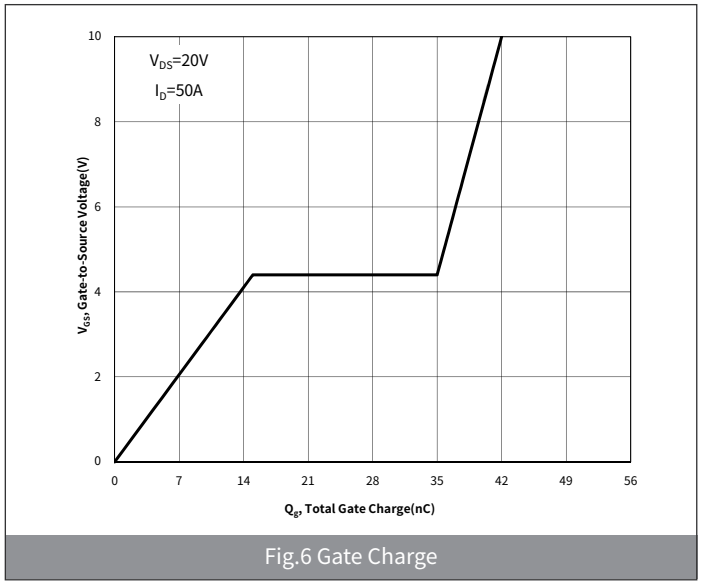


Fig.6 Gate Charge

Ratings And Characteristics Curves (Ta=25°C Unless otherwise specified)

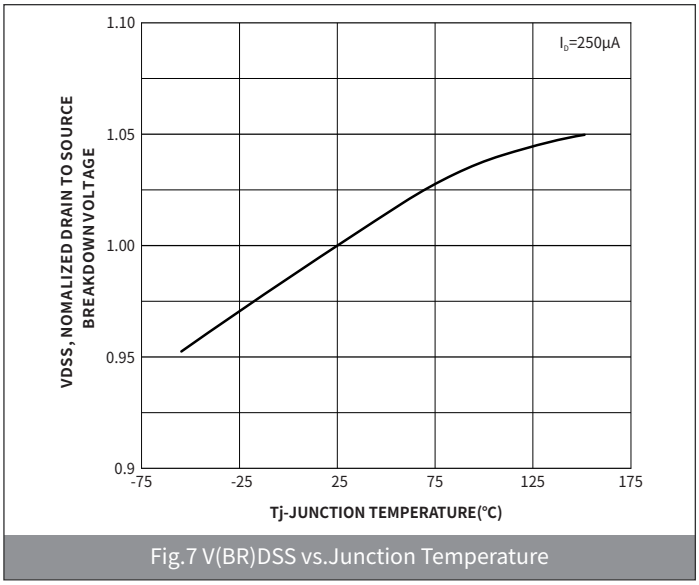


Fig.7 V(BR)DSS vs.Junction Temperature

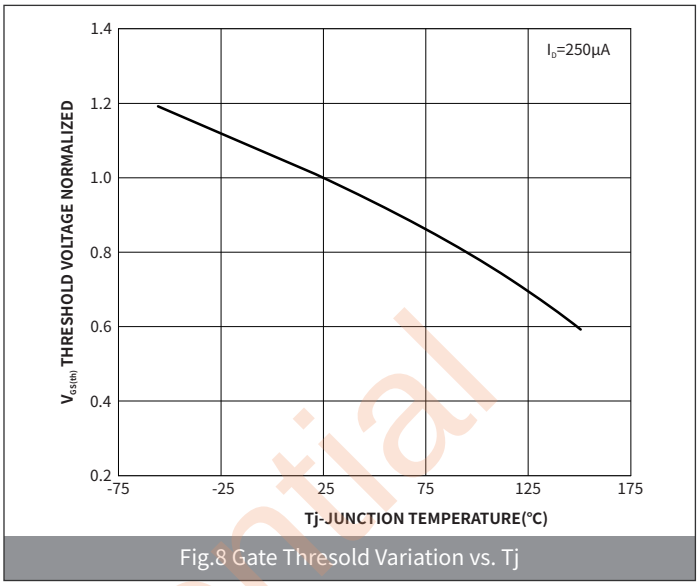


Fig.8 Gate Thresold Variation vs. Tj

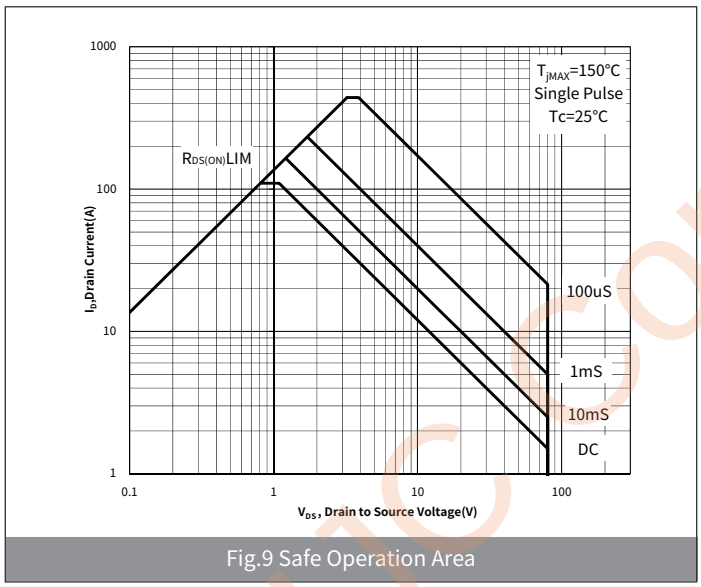


Fig.9 Safe Operation Area

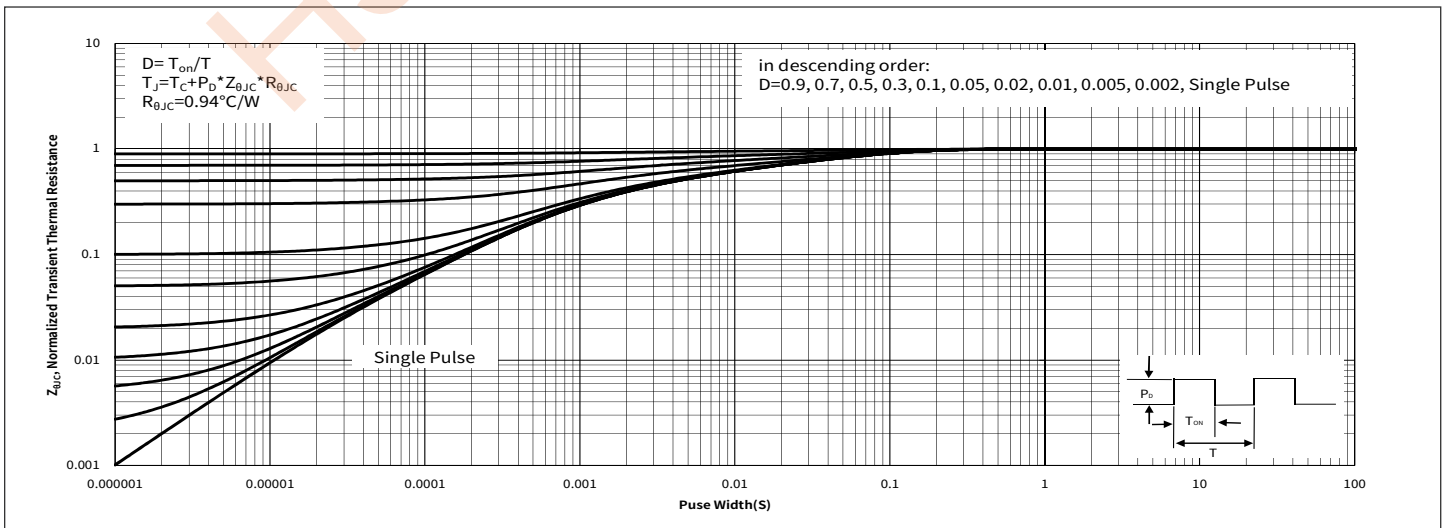
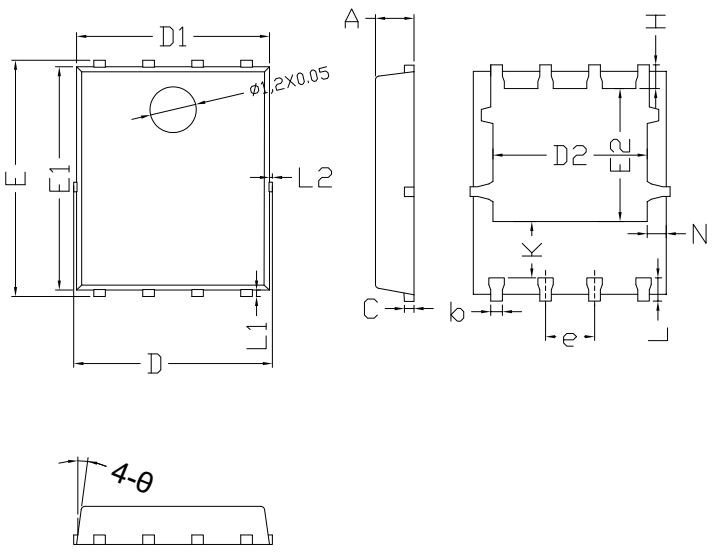


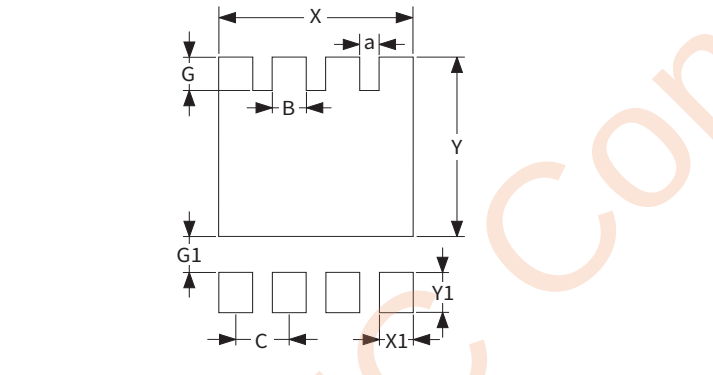
Fig.10 Normalized Maximum Transient Thermal Impedance

Package Outline Dimensions (PDFN5060)



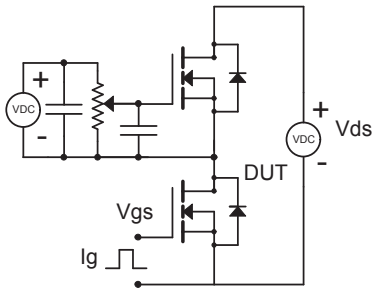
Symbol	Dimensions			
	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	0.90	1.05	0.035	0.041
b	0.35	0.45	0.014	0.018
C	0.20	0.30	0.008	0.012
D	4.944	5.09	0.195	0.201
D1	4.82	4.97	0.190	0.196
D2	3.90	4.20	0.154	0.165
e	1.17	1.37	0.046	0.054
E	5.97	6.13	0.236	0.241
E1	5.67	5.82	0.223	0.229
E2	3.35	3.65	0.132	0.144
H	0.57	0.72	0.023	0.029
K	1.19	1.39	0.047	0.056
L	0.56	0.71	0.022	0.028
L1	0.06	0.20	0.002	0.008
L2	-	0.12	-	0.005
N	0.40	0.60	0.016	0.024
θ	9°	13°	9°	13°

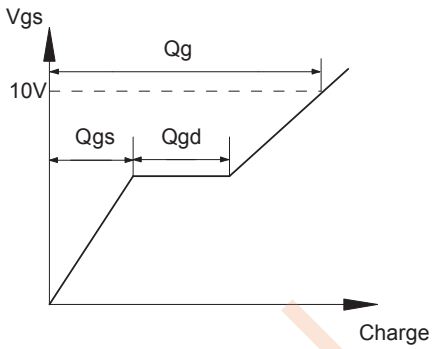
Suggested Pad Layout



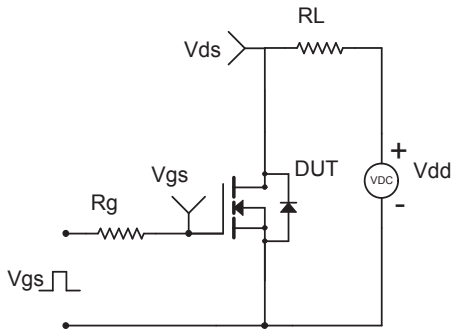
Symbol	Dimensions			
	Millimeters		Inches	
	Min.	Max.	Min.	Max.
a	0.46	0.48	0.0184	0.0192
B	0.70	0.90	0.028	0.036
C	1.17	1.37	0.0468	0.0548
G	0.75	0.95	0.03	0.038
G1	0.80	1.00	0.032	0.04
X	4.50	4.70	0.180	0.188
X1	0.70	0.90	0.028	0.036
Y	4.40	4.60	0.176	0.184
Y1	0.90	1.10	0.036	0.044

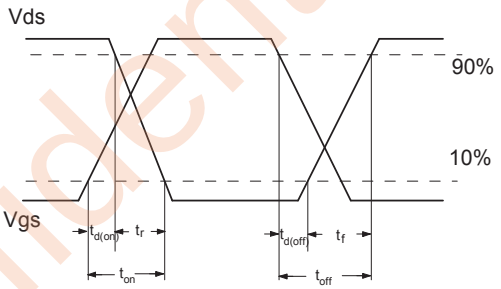
1.Gate Charge Test Circuit & Waveforms



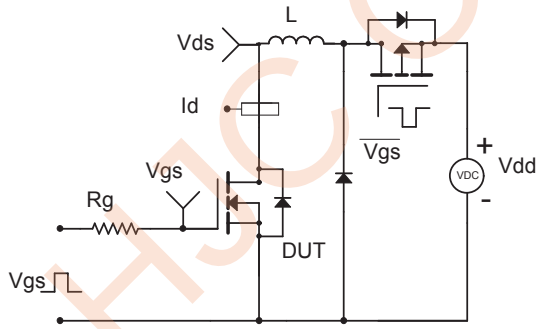


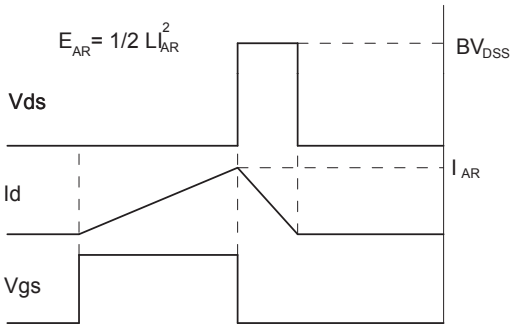
2. Resistive Switching Test Circuit & Waveforms





3.Unclamped Inductive Switching (UIS) Test Circuit & Waveforms





4.Diode Recovery Test Circuit & Waveforms