CREE

C3M0060065J

Silicon Carbide Power MOSFET
C3M™ MOSFET Technology

N-Channel Enhancement Mode

V_{DS}	650 V
$I_{D\ @\ 25^{\circ}C}$	36 A
$R_{DS(on)}$	60 mΩ

Features

- 3rd Generation SiC MOSFET technology
- Low inductance package with driver source pin
- 7mm of creepage distance between drain and source
- High blocking voltage with low on-resistance
- High speed switching with low capacitances
- Fast intrinsic diode with low reverse recovery (Qrr)
- Halogen free, RoHS compliant

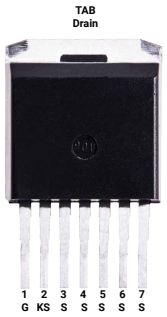
Benefits

- Higher system efficiency
- Reduced cooling requirements
- Increased power density
- Increased system switching frequency
- Easy to parallel and simple to drive
- Enable new hard switching PFC topologies (Totem-Pole)

Applications

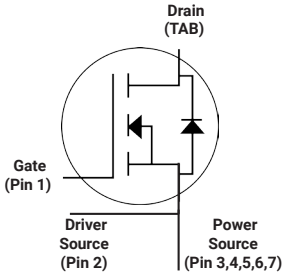
- EV charging
- Server power supplies
- Solar PV inverters
- UPS
- DC/DC converters

Package



Halogen-Free

RoHS



Part Number	Package	Marking
C3M0060065J	TO-263-7	C3M0060065J

Maximum Ratings

Symbol	Parameter	Value	Unit	Note
V_{DSS}	Drain - Source Voltage, T_C = 25 ˚C	650	V	
V_{GS}	Gate - Source voltage (Under transient events < 100 ns)	-8/+19	V	Fig. 28
I_D	Continuous Drain Current, V_{GS} = 15 V, T_C = 25˚C	36	A	Fig. 19
	Continuous Drain Current, V_{GS} = 15 V, T_C = 100˚C	26		
$I_{D(pulse)}$	Pulsed Drain Current, Pulse width t_P limited by T_{jmax}	99	A	
P_D	Power Dissipation, T_C=25˚C, T_J = 175 ˚C	136	W	Fig. 20
T_J , T_{stg}	Operating Junction and Storage Temperature	-40 to +175	˚C	
T_L	Solder Temperature, 1.6mm (0.063”) from case for 10s	260	˚C	

Electrical Characteristics (T_C = 25˚C unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions	Note
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	650			V	V_{GS} = 0 V, I_D = 100 µA	
V_{GSon}	Gate-Source Recommended Turn-On Voltage		15		V	Static	Fig. 28
V_{GSoff}	Gate-Source Recommended Turn-Off Voltage		-4		V		
$V_{GS(th)}$	Gate Threshold Voltage	1.8	2.3	3.6	V	V_{DS} = V_{GS}, I_D = 5 mA	Fig. 11
			1.9		V	V_{DS} = V_{GS}, I_D = 5 mA, T_J = 175ºC	
I_{DSS}	Zero Gate Voltage Drain Current		1	50	µA	V_{DS} = 650 V, V_{GS} = 0 V	
I_{GSS}	Gate-Source Leakage Current		10	250	nA	V_{GS} = 15 V, V_{DS} = 0 V	
$R_{DS(on)}$	Drain-Source On-State Resistance	42	60	79	mΩ	V_{GS} = 15 V, I_D = 13.2 A	Fig. 4, 5,6
			80			V_{GS} = 15 V, I_D = 13.2 A, T_J = 175ºC	
g_{fs}	Transconductance		10		S	V_{DS}= 20 V, I_{DS}= 13.2 A	Fig. 7
			9			V_{DS}= 20 V, I_{DS}= 13.2 A, T_J = 175ºC	
C_{iss}	Input Capacitance		1020		pF	V_{GS} = 0 V, V_{DS} = 600 V f = 1 MHz V_{AC} = 25 mV	Fig. 17, 18
C_{oss}	Output Capacitance		80				
C_{rss}	Reverse Transfer Capacitance		9				
$C_{o(er)}$	Effective Output Capacitance (Energy Related)		95		pF	V_{GS} = 0 V, V_{DS} = 0V to 400 V	Note 1
$C_{o(tr)}$	Effective Output Capacitance (Time Related)		132				
E_{oss}	C_{oss} Stored Energy		15		µJ	V_{DS} = 600 V, 1 MHz	Fig. 16
E_{ON}	Turn-On Switching Energy (Body Diode)		41		µJ	V_{DS} = 400 V, V_{GS} = -4 V/15 V, I_D = 13.2 A, $R_{G(ext)}$ = 2.5Ω, L= 135 µH, T_J = 175ºC FWD = Internal Body Diode of MOSFET	Fig. 25
E_{OFF}	Turn Off Switching Energy (Body Diode)		5				
$t_{d(on)}$	Turn-On Delay Time		9		ns	V_{DD} = 400 V, V_{GS} = -4 V/15 V I_D = 13.2 A, $R_{G(ext)}$ = 2.5 Ω, L= 135 µH Timing relative to V_{DS} Inductive load	Fig. 26
t_r	Rise Time		8				
$t_{d(off)}$	Turn-Off Delay Time		17				
t_f	Fall Time		6				
$R_{G(int)}$	Internal Gate Resistance		3		Ω	f = 1 MHz, V_{AC} = 25 mV	
Q_{gs}	Gate to Source Charge		14		nC	V_{DS} = 400 V, V_{GS} = -4 V/15 V I_D = 13.2 A Per IEC60747-8-4 pg 21	Fig. 12
Q_{gd}	Gate to Drain Charge		14				
Q_g	Total Gate Charge		46				

Note (1): $C_{o(er)}$, a lumped capacitance that gives same stored energy as Coss while Vds is rising from 0 to 400V
$C_{o(tr)}$, a lumped capacitance that gives same charging time as Coss while Vds is rising from 0 to 400V

Reverse Diode Characteristics (T_C = 25˚C unless otherwise specified)

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions	Note
V_{SD}	Diode Forward Voltage	5.1		V	V_{GS} = -4 V, I_{SD} = 6.6 A, T_J = 25 °C	Fig. 8, 9, 10
		4.8		V	V_{GS} = -4 V, I_{SD} = 6.6 A, T_J = 175 °C	
I_S	Continuous Diode Forward Current		21	A	V_{GS} = -4 V, T_C = 25˚C	
$I_{S,\ pulse}$	Diode pulse Current		99	A	V_{GS} = -4 V, pulse width t_P limited by T_{jmax}	
t_{rr}	Reverse Recover time	8		ns	V_{GS} = -4 V, I_{SD} = 13.2 A, V_R = 400 V dif/dt = 3600 A/µs, T_J = 175 °C	
Q_{rr}	Reverse Recovery Charge	75		nC		
I_{rrm}	Peak Reverse Recovery Current	15		A		
t_{rr}	Reverse Recover time	10		ns	V_{GS} = -4 V, I_{SD} = 13.2 A, V_R = 400 V dif/dt = 2300 A/µs, T_J = 175 °C	
Q_{rr}	Reverse Recovery Charge	62		nC		
I_{rrm}	Peak Reverse Recovery Current	10		A		

Thermal Characteristics

Symbol	Parameter	Typ.	Unit	Test Conditions	Note
$R_{\theta JC}$	Thermal Resistance from Junction to Case	1.1	°C/W		Fig. 21
$R_{\theta JA}$	Thermal Resistance From Junction to Ambient	40			

Typical Performance

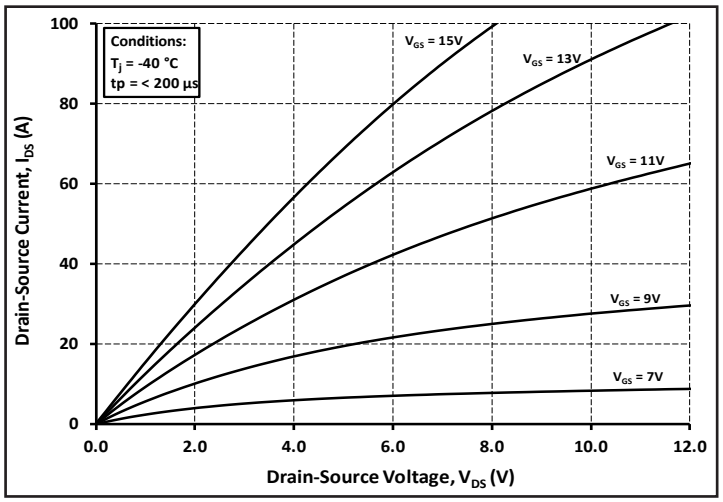


Figure 1. Output Characteristics T_J = -40 ºC

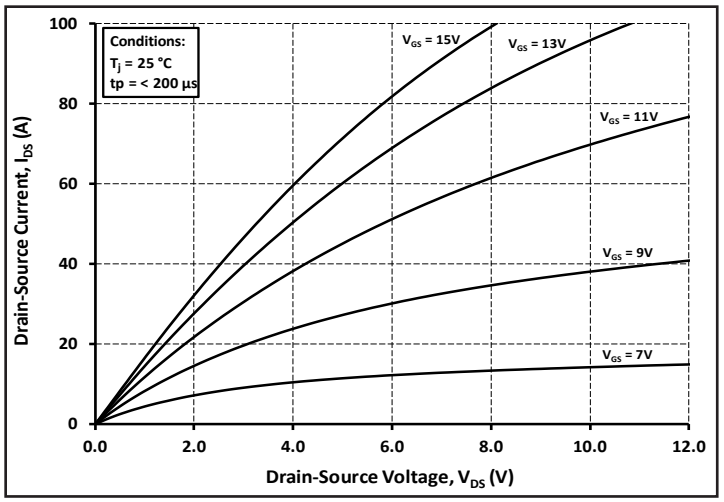


Figure 2. Output Characteristics T_J = 25 ºC

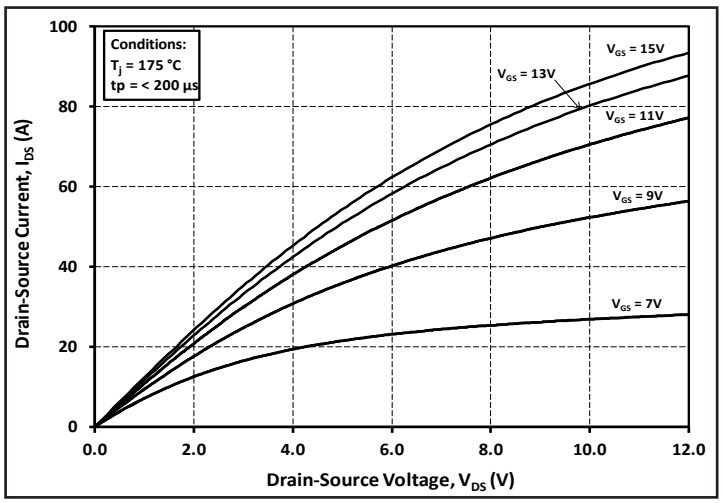


Figure 3. Output Characteristics T_J = 175 ºC

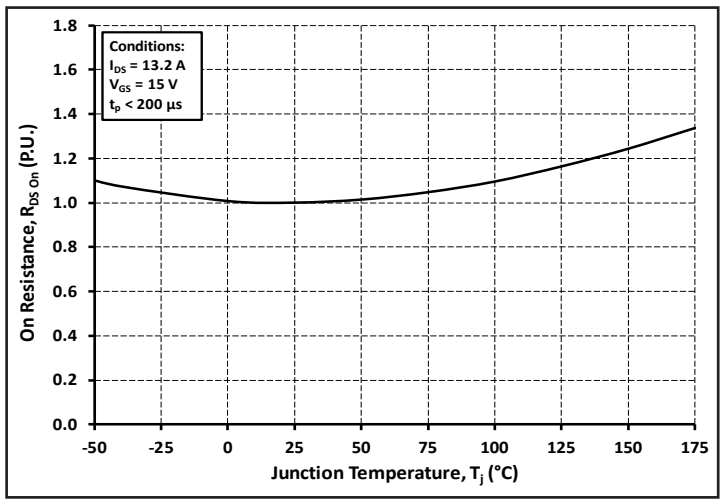


Figure 4. Normalized On-Resistance vs. Temperature

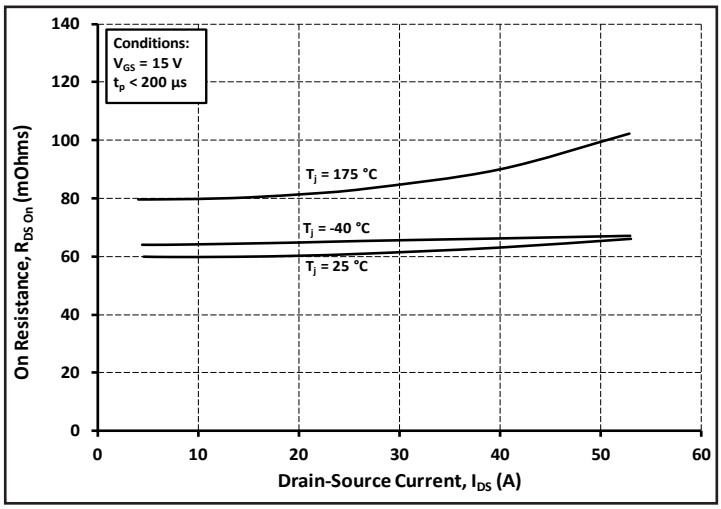


Figure 5. On-Resistance vs. Drain Current
For Various Temperatures

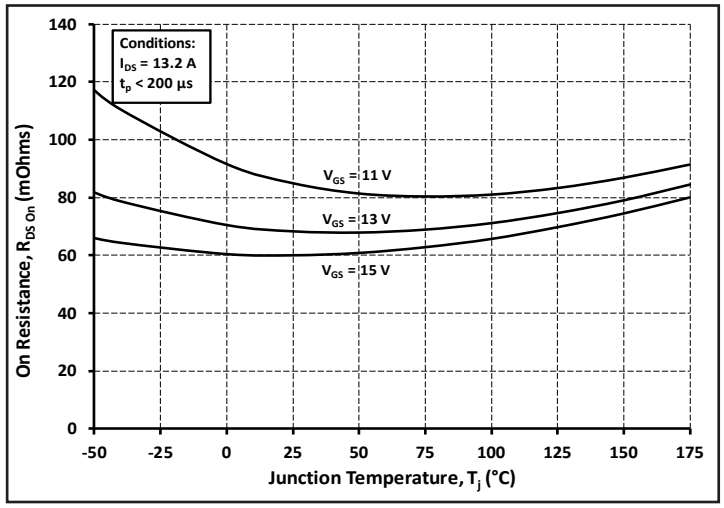


Figure 6. On-Resistance vs. Temperature
For Various Gate Voltage

Typical Performance

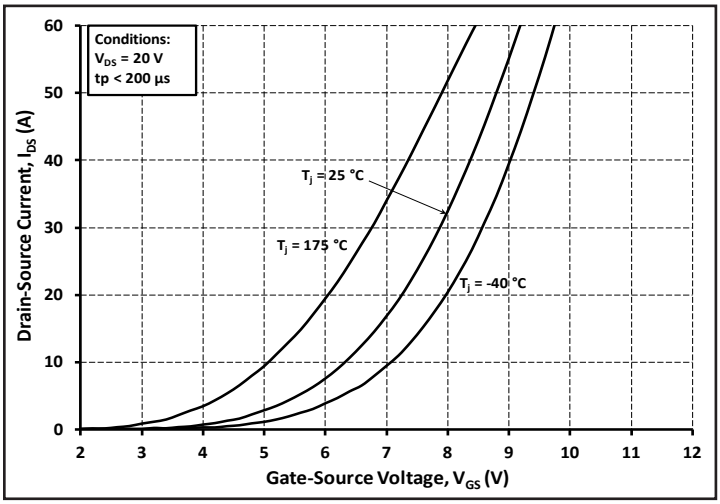


Figure 7. Transfer Characteristic for Various Junction Temperatures

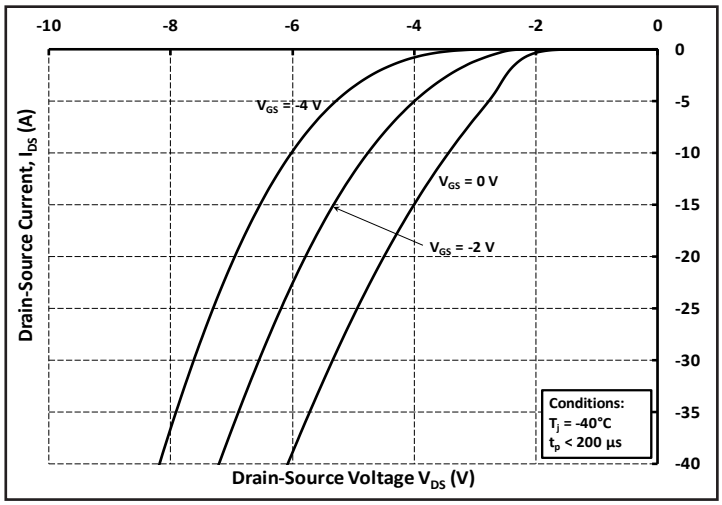


Figure 8. Body Diode Characteristic at -40 °C

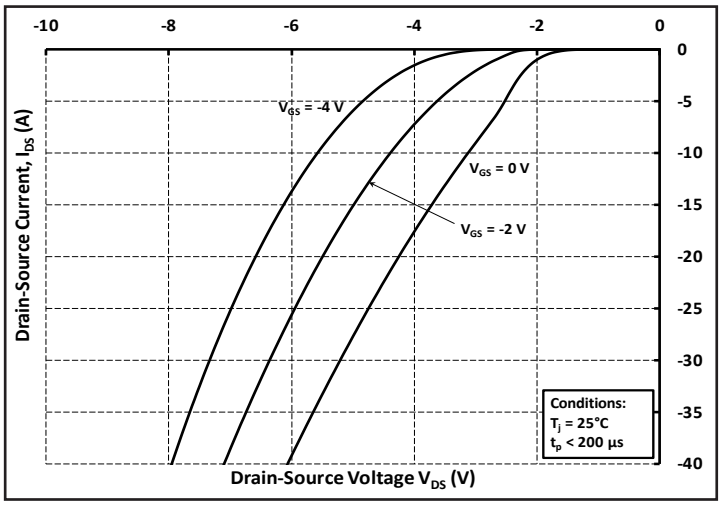


Figure 9. Body Diode Characteristic at 25 °C

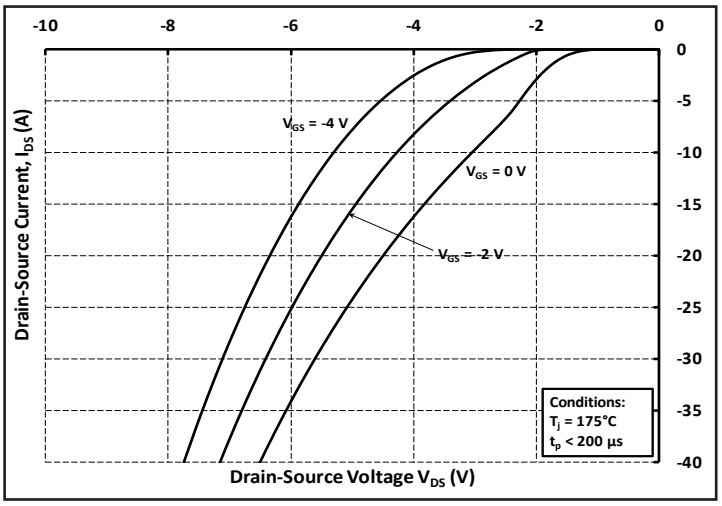


Figure 10. Body Diode Characteristic at 175 °C

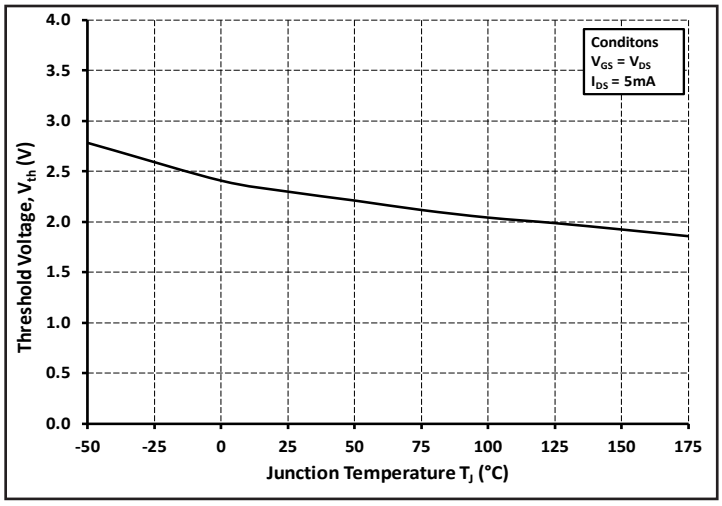


Figure 11. Threshold Voltage vs. Temperature

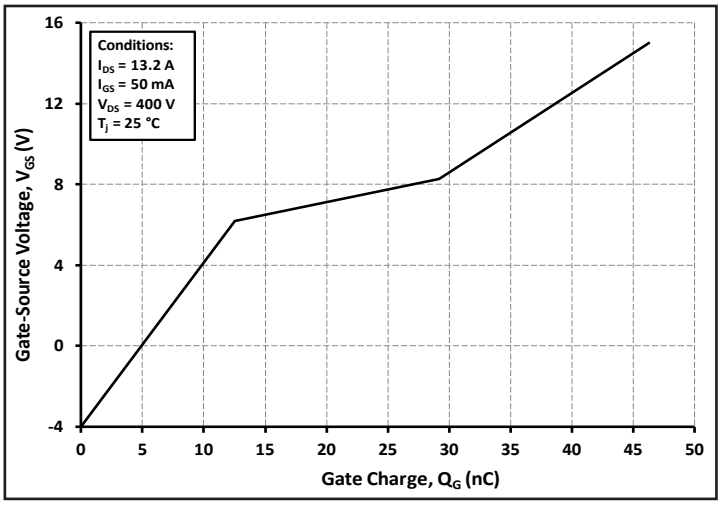


Figure 12. Gate Charge Characteristics

Typical Performance

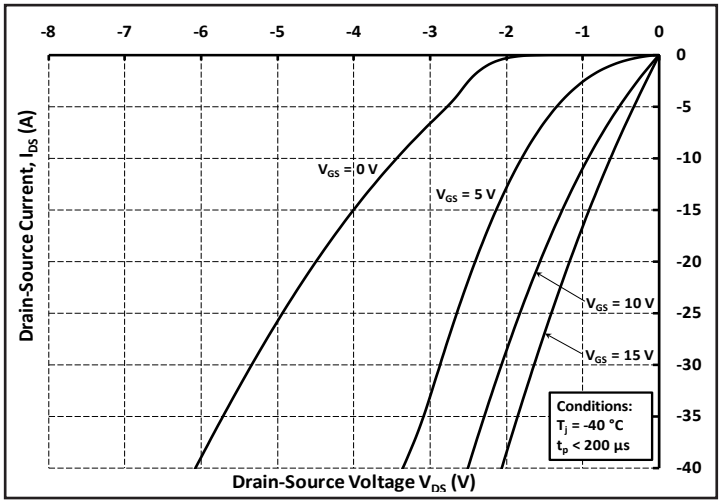


Figure 13. 3rd Quadrant Characteristic at -40 °C

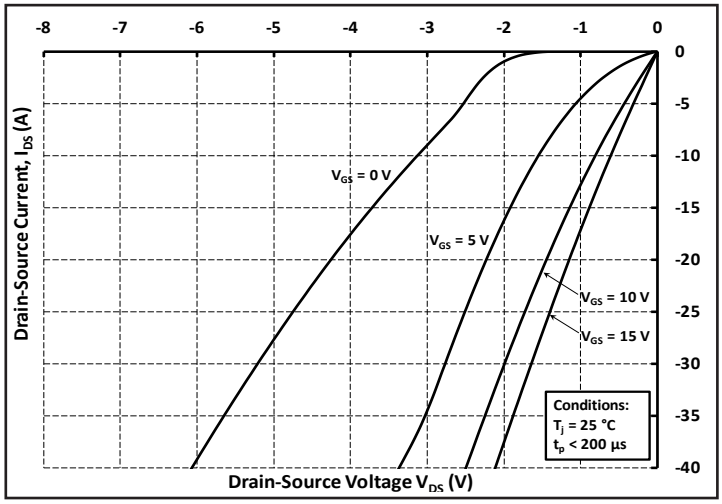


Figure 14. 3rd Quadrant Characteristic at 25 °C

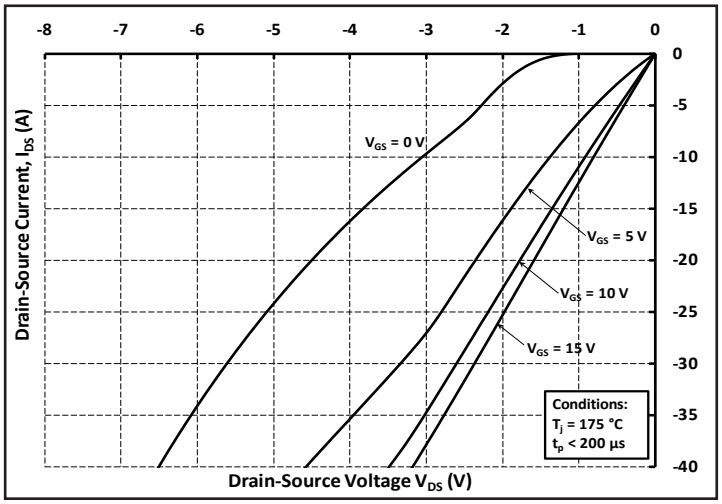


Figure 15. 3rd Quadrant Characteristic at 175 °C

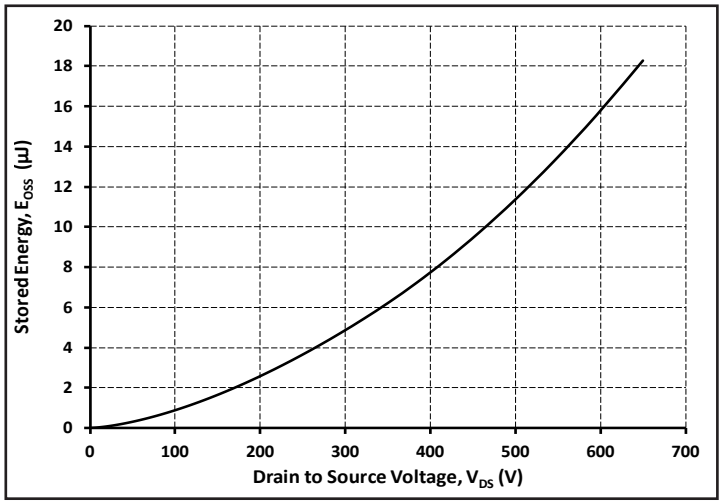


Figure 16. Output Capacitor Stored Energy

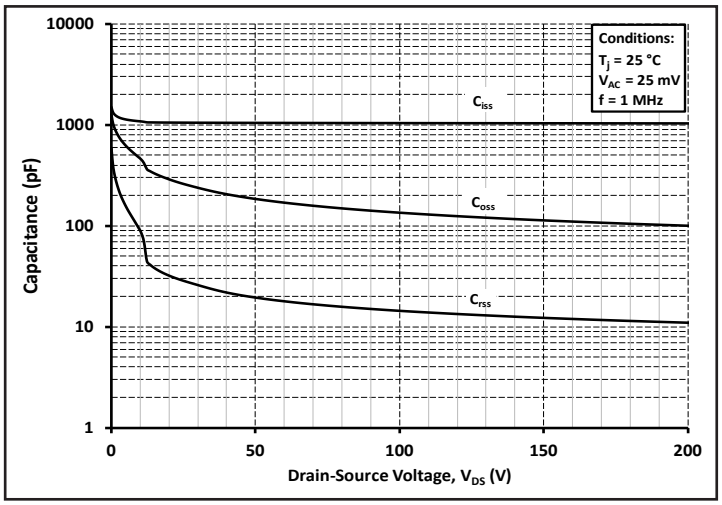


Figure 17. Capacitances vs. Drain-Source Voltage (0 - 200V)

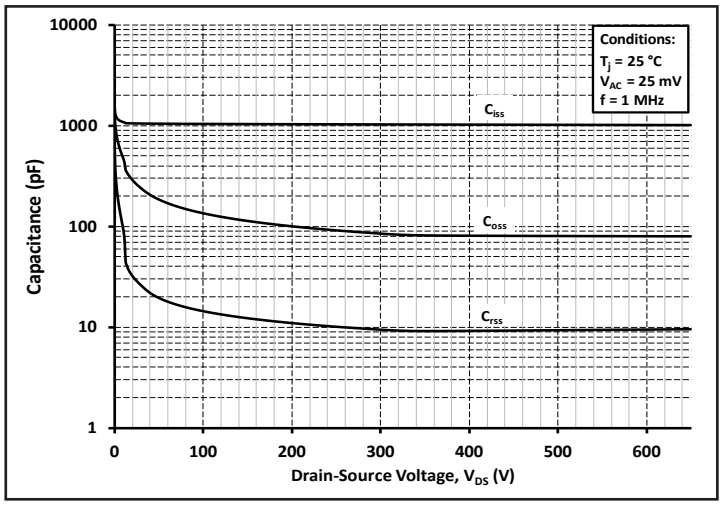


Figure 18. Capacitances vs. Drain-Source Voltage (0 - 650V)

Typical Performance

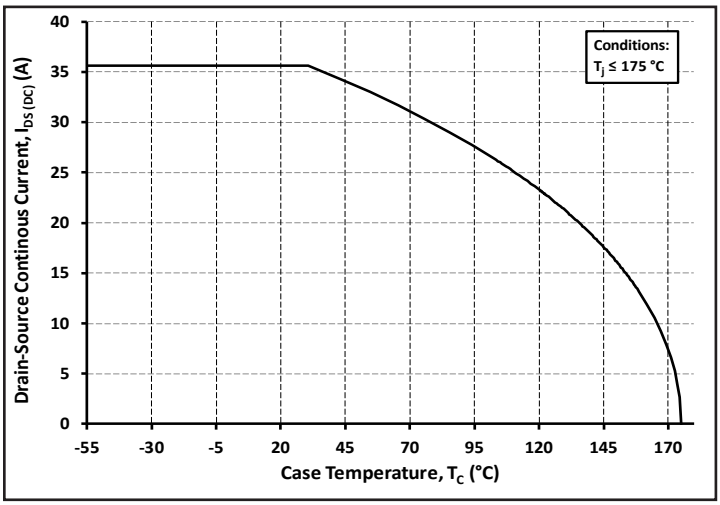


Figure 19. Continuous Drain Current Derating vs. Case Temperature

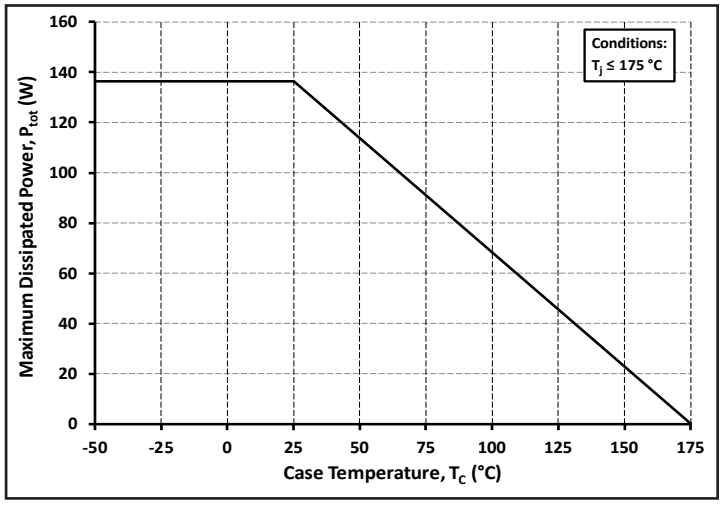


Figure 20. Maximum Power Dissipation Derating Vs Case Temperature

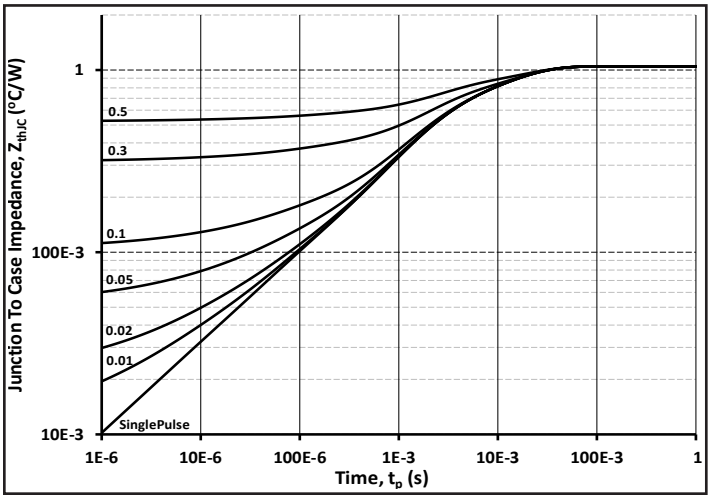


Figure 21. Transient Thermal Impedance (Junction - Case)

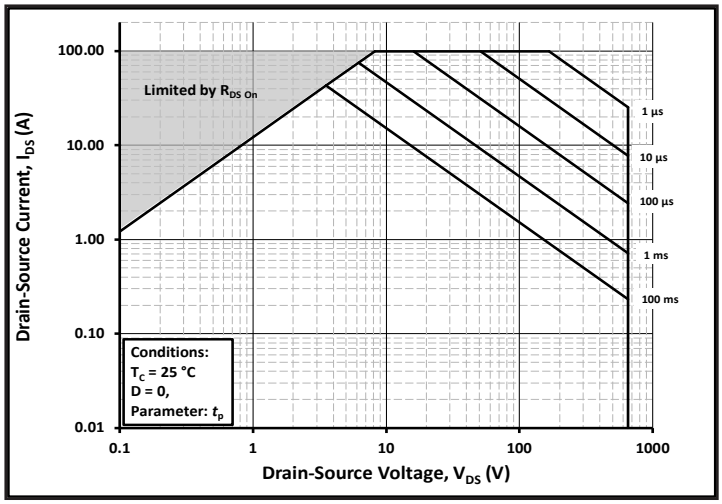


Figure 22. Safe Operating Area

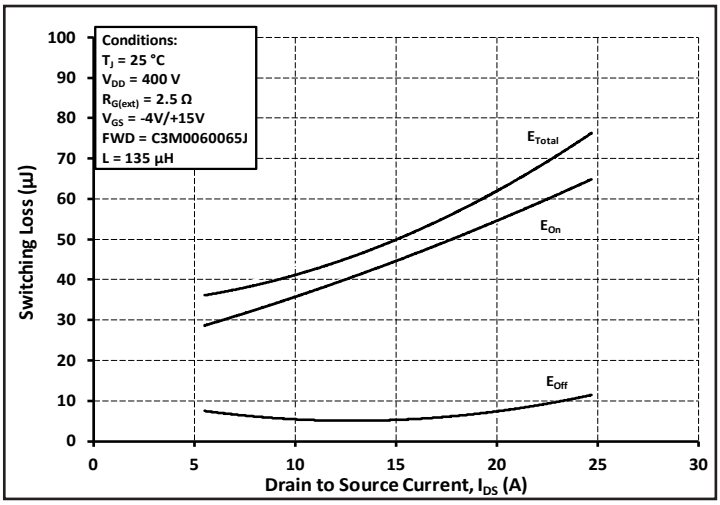


Figure 23. Clamped Inductive Switching Energy vs. Drain Current (V_{DD} = 400V)

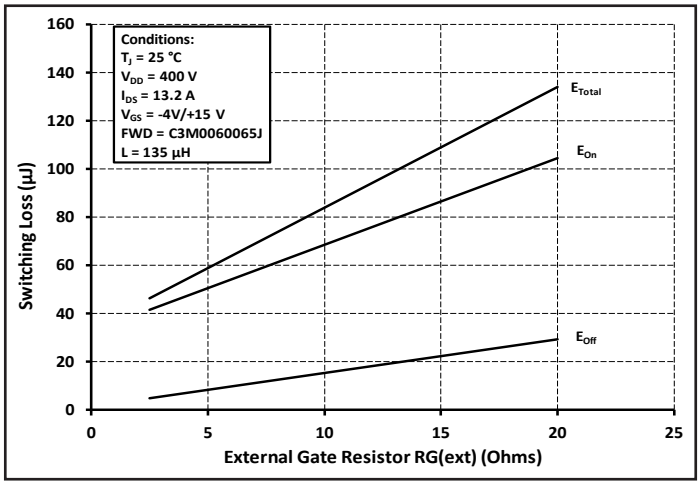


Figure 24. Clamped Inductive Switching Energy vs. $R_{G(ext)}$

Typical Performance

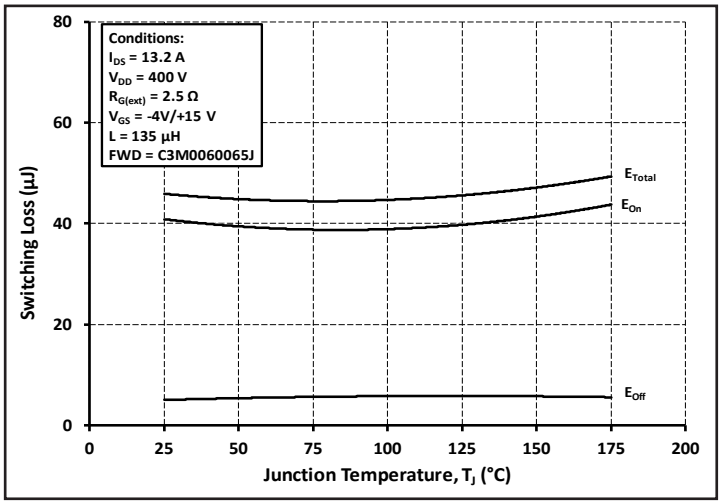


Figure 25. Clamped Inductive Switching Energy vs. Temperature

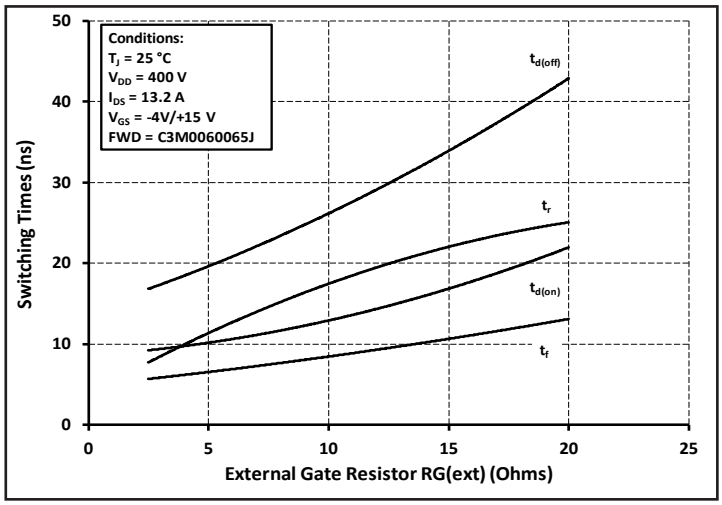


Figure 26. Switching Times vs. $R_{G(ext)}$

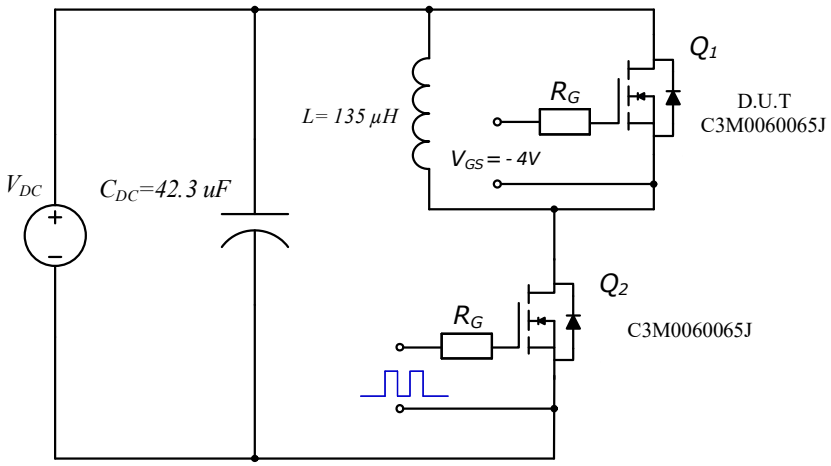


Figure 27. Clamped Inductive Switching Waveform Test Circuit

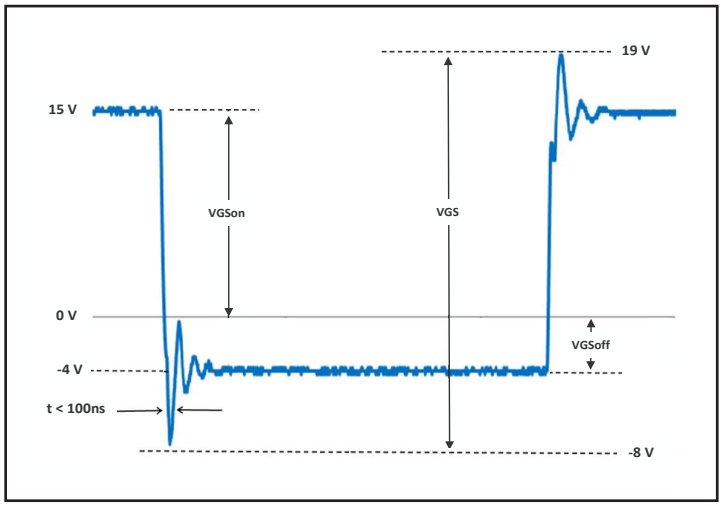
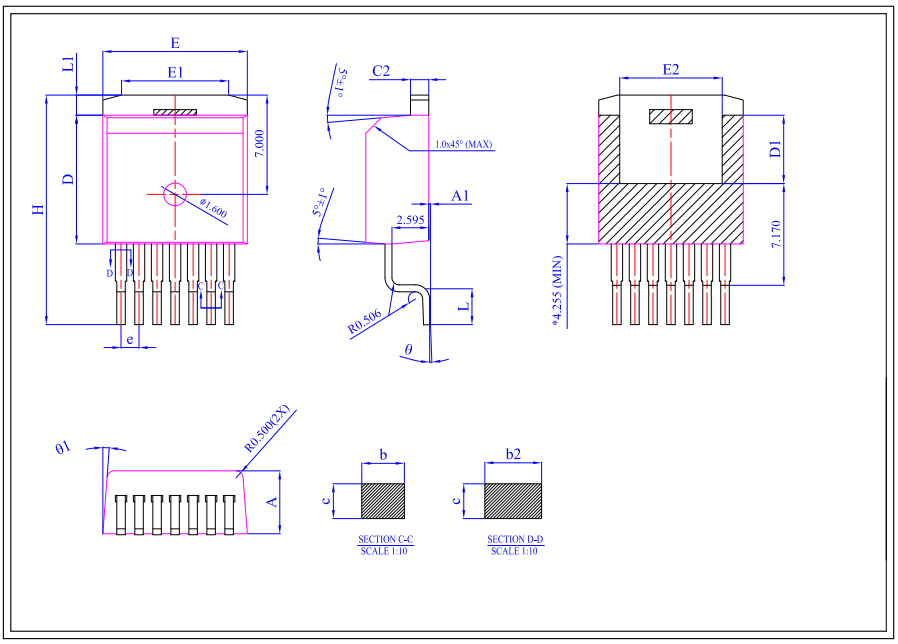


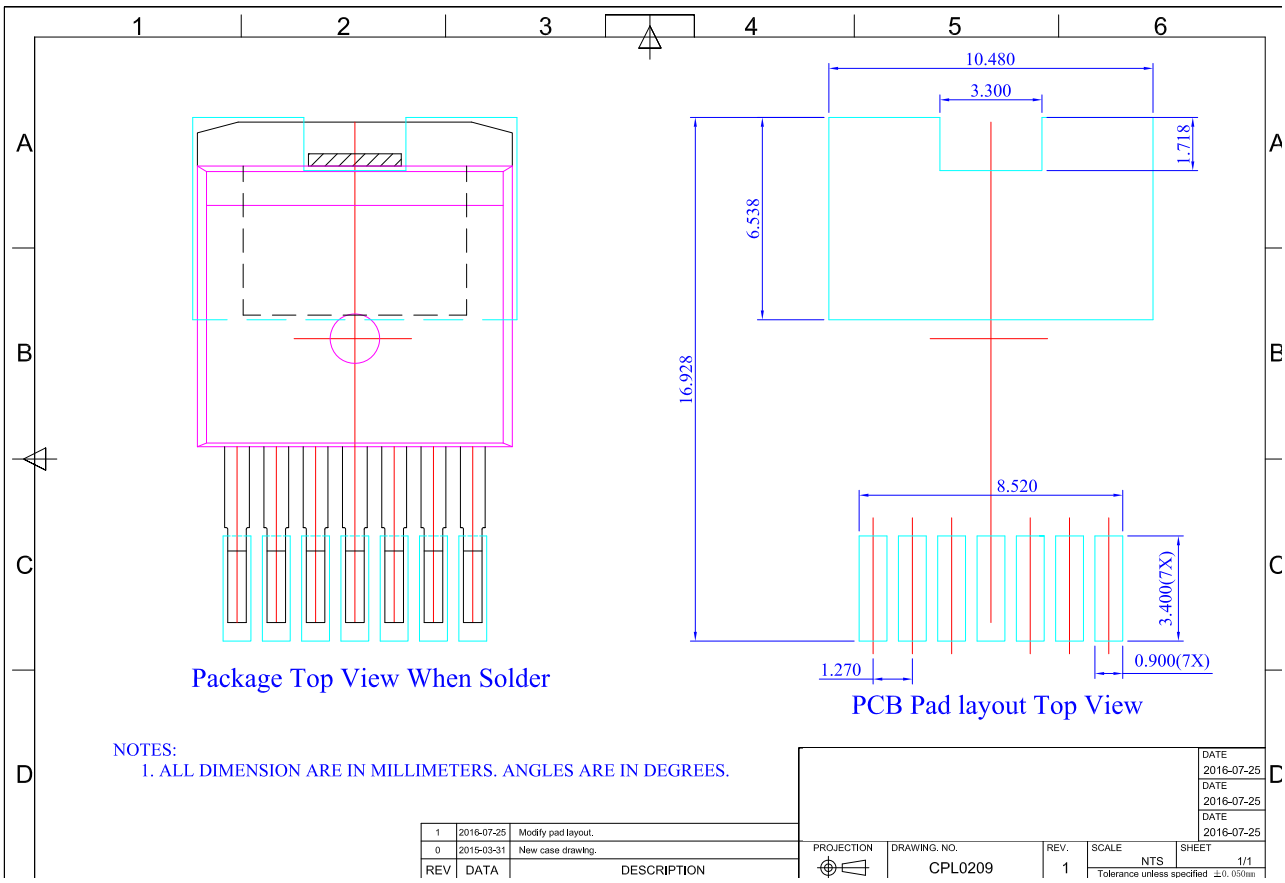
Figure 28. V_{GS} Waveform Example

Package Dimensions

Package 7L D2PAK



Dim	All Dimensions in Millimeters		
	Min	typ	Max
A	4.300	4.435	4.570
A1	0.00	0.125	0.25
b	0.500	0.600	0.700
b2	0.600	0.800	1.000
c	0.330	0.490	0.650
C2	1.170	1.285	1.400
D	9.025	9.075	9.125
D1	4.700	4.800	4.900
E	10.130	10.180	10.230
E1	6.500	7.550	8.600
E2	6.778	7.223	7.665
e	1.27		
H	15.043	16.178	17.313
L	2.324	2.512	2.700
L1	0.968	1.418	1.868
Ø	0°	4°	8°
Ø1	4.5°	5°	5.5°



Notes

- **RoHS Compliance**
  The levels of RoHS restricted materials in this product are below the maximum concentration values (also referred to as the threshold limits) permitted for such substances, or are used in an exempted application, in accordance with EU Directive 2011/65/EC (RoHS2), as implemented January 2, 2013. RoHS Declarations for this product can be obtained from your Cree representative or from the Product Documentation sections of www.cree.com.

- **REACh Compliance**
  REACh substances of high concern (SVHCs) information is available for this product. Since the European Chemical Agency (ECHA) has published notice of their intent to frequently revise the SVHC listing for the foreseeable future,please contact a Cree representative to insure you get the most up-to-date REACh SVHC Declaration. REACh banned substance information (REACh Article 67) is also available upon request.

- This product has not been designed or tested for use in, and is not intended for use in, applications implanted into the human body nor in applications in which failure of the product could lead to death, personal injury or property damage, including but not limited to equipment used in the operation of nuclear facilities, life-support machines, cardiac defibrillators or similar emergency medical equipment, aircraft navigation or communication or control systems, air traffic control systems.

Related Links

- **SPICE Models: http://wolfspeed.com/power/tools-and-support**
- **SiC MOSFET Isolated Gate Driver reference design: http://wolfspeed.com/power/tools-and-support**
- **SiC MOSFET Evaluation Board: http://wolfspeed.com/power/tools-and-support**

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