# 8-BIT, 4-CHANNEL, 50 KSPS to 200 KSPS, LOW POWER ANALOG-TO-DIGITAL CONVERTER

## FEATURES

- Four Input Channels
- Specified for $V_A$ of 2.70 V to 5.25 V
- Specified Over a Range of Sample Rates
- Throughput Rate: 50 - 200 KSPS
- Zero Latency
- ±0.4LSB INL, ±0.4LSB DNL
- SPI/DSP/MICROWIRE/QSPI-Compatible Serial Interface
- Low Power (typical):
  2.15mW (2.7V, 200KSPS)
  3.60mW (3.3V, 200KSPS)
- Packaged in 10-Lead MSOP

## APPLICATIONS

- Portable Systems
- Remote Data Acquisition
- Instrumentation and Control Systems
- Medical Instruments
- Mobile Communications



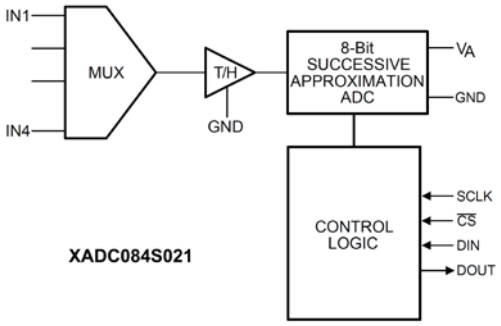



*Figure 1. Functional Block Diagram*

## DESCRIPTION

The XADC084S021 is a low power, 4-channel 8-bit analog-to-digital converter with a high speed serial interface. Unlike the conventional practice of specifying performance at a single sample rate only, the XADC084S021 is fully specified over a sample rate range of 50 KSPS to 200 KSPS. The converter is based upon a successive-approximation register architecture with an internal track-and-hold circuit. The XADC084S021 contains four single-ended analog inputs, IN1 through IN4. The analog input on each of these channels is from 0 to $V_A$.

The XADC084S021 is available in a 10-lead MSOP package and has an operating temperature range of -40°C to 85°C.

**The XADC084S021 is a drop-in replacement for the ADC084S021.**

# SPECIFICATIONS

At-40℃ to 85℃, $f_{SAMPLE}$ = 200 KSPS and $f_{SCLK}$ = 3.2 MHz, 2.70 V ≤ $V_A$ ≤ 5.25 V, unless otherwise noted.

## XADC084S021

| PARAMETER | TEST CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **SYSTEM PERFORMANCE** | | | | | | |
| Resolution | | | | **8** | | Bits |
| No missing codes | | | | **8** | | Bits |
| Integral linearity | | | **-0.4** | **±0.2** | **0.4** | LSB |
| Differential linearity | | | **-0.4** | **±0.2** | **0.4** | LSB |
| $f_{SAMPLE}$ Throughput rate | $f_{SCLK}$ = 1.6 MHz, $f_{SCLK}$ = 3.2 MHz<br>2.70 V ≤ $V_A$ ≤ 5.25 V | | **50** | | **200** | KSPS |
| SNR | $f_{IN}$ = 40 kHz | | | **49.5** | | dB |
| THD | $f_{IN}$ = 40 kHz | | | **-70** | | dB |
| $I_A$ Supply current, normal operation | $\overline{CS}$ low | $f_{SAMPLE}$ = 100 KSPS, $f_{SCLK}$ = 3.2 MHz, $V_A$ = 2.7 V | | **0.65** | **1.30** | mA |
| | | $f_{SAMPLE}$ =200 KSPS, $f_{SCLK}$ = 3.2 MHz, $V_A$ = 2.7 V | | **0.80** | **1.50** | |
| | | $f_{SAMPLE}$ = 100 KSPS, $f_{SCLK}$ = 3.2 MHz, $V_A$ = 3.3 V | | **1.00** | **2.30** | |
| | | $f_{SAMPLE}$ =200 KSPS, $f_{SCLK}$ = 3.2 MHz, $V_A$ = 3.3 V | | **1.10** | **2.50** | |
| **POWER DISSIPATION** | | | | | | |
| Normal operation | | $f_{SAMPLE}$ = 200 KSPS, $f_{SCLK}$ = 3.2 MHz, $V_A$ = 2.7 V | | **2.15** | **4.10** | mW |
| | | $f_{SAMPLE}$ = 200 KSPS, $f_{SCLK}$ = 3.2 MHz, $V_A$ = 3.3 V | | **3.60** | **8.20** | mW |
| | | | | | | |

# PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

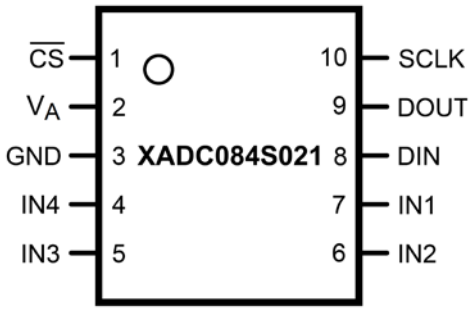



*Figure 2. Pin Configuration*

| TERMINAL | | DESCRIPTION |
|---|---|---|
| NAME | NO. | |
| $\overline{CS}$ | 1 | Chip select. On the falling edge of $\overline{CS}$, a conversion process begins. |
| $V_A$ | 2 | Power supply pin. This voltage is also used as the reference voltage. The $V_A$ range is from 2.70 V to 5.25 V. |
| GND | 3 | Ground reference point for all circuitry on the XADC084S021. Both of these pins should connect to the GND plane of a system. |
| IN4 – IN1 | 4-7 | Analog Input 1 through Analog Input 4. Four single-ended analog input channels that are multiplexed into the on-chip track/hold. The analog input channel to be converted is selected by using the ADD0 through ADD2 bits of the Control Register. The input range for all input channels is 0 to $V_A$. Any unused input channels should be connected to GND to avoid noise pickup. |
| DIN | 8 | Digital data input. The XADC084S021's Control Register is loaded through this pin on rising edges of the SCLK pin. |
| DOUT | 9 | Digital data output. The output samples are clocked out of this pin on the falling edges of the SCLK pin. |
| SCLK | 10 | Digital clock input. SCLK provides the serial clock for accessing data from the part and writing serial data to the Control Register. This clock input is also used as the clock source for the XADC084S021's conversion process. |

# TYPICAL CONNECTION

*Figure 3* shows a typical connection diagram for the XADC084S021. The 3.3 V supply should come from a stable power supply such as an LDO. The supply to XADC084S021 should be decoupled to the ground. A 1-µF and a 0.1-µF decoupling capacitor are required between the $V_A$ and GND pins of the converter. This capacitor should be placed as close as possible to the pins of the device.

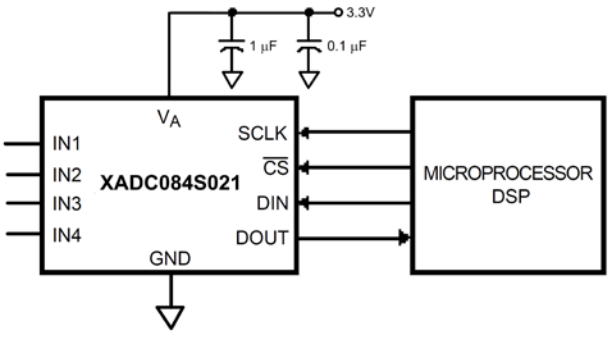



*Figure 3. Typical Circuit Configuration*

# CONTROL REGISTER

The Control Register on the XADC084S021 is an 8-bit, write-only register. Data is loaded from the DIN pin of the XADC084S021 on the rising edge of SCLK. The data is transferred on the DIN line at the same time as the conversion result is read from the part. This requires 16 serial clocks for every data transfer. Only the information provided on the first 8 rising clock edges (after $\overline{CS}$ falling edge) is loaded to the Control Register. MSB denotes the first bit in the data stream. The bit functions are outlined in Table 1 and Table 2. Note that, the default contents of the Control Register on power-up is all zeros.

***Table 1. Control Register Bits***

| Bit7(MSB) | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---|---|---|---|---|---|---|---|
| DONTC | ZERO | ADD2 | ADD1 | ADD0 | ONE | ZERO | ZERO |

***Table 2. Control Register Bit Descriptions***

| Bit | Mnemonic | Comment |
|---|---|---|
| 7 | DONTC | Don't care. The values of these bits do not affect the device. |
| 6 | ZERO | A zero must be written to this bit to ensure correct operation of the XADC084S021. |
| 5 | ADD2 | These three bits determine which input channel is sampled and converted at the next conversion cycle. |
| 4 | ADD1 | |
| 3 | ADD0 | |
| 2 | ONE | A one must be written to this bit to ensure correct operation of the XADC084S021. |
| 1，0 | ZERO | A zero must be written to this bit to ensure correct operation of the XADC084S021. |

# INPUT CHANNEL SELECTION

On power-up, the default selection is IN4. When returning to normal operation from tri-state, the IN selected will be the same one that was selected prior to tri-state being initiated. Table 3 below shows the multiplexer address corresponding to each analog input from IN4 to IN1 for the XADC084S021.

***Table 3. Input Channel Selection***

| ADD2 | ADD1 | ADD0 | Input Channel |
|---|---|---|---|
| 0 | 0 | 0 | IN4(Default) |
| 0 | 0 | 1 | IN3 |
| 0 | 1 | 0 | IN2 |
| 0 | 1 | 1 | IN1 |

Please note that the difference between XADC084S021 and ADC084S021 is that when XADC084S021 is restarted, the default channel is IN4 instead of IN1.

# TIMING DIAGRAM

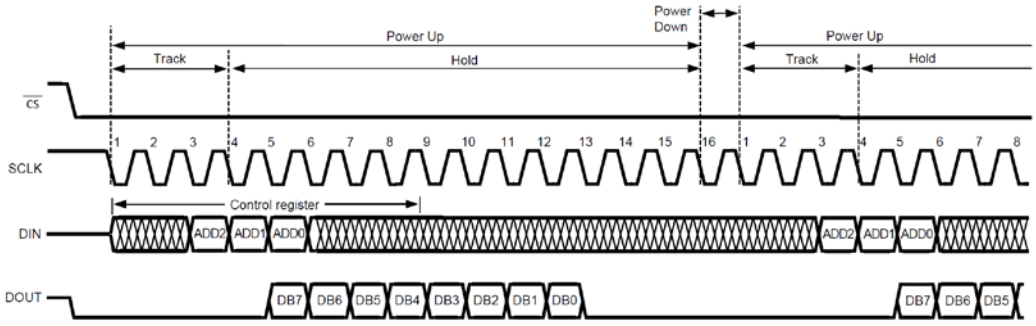
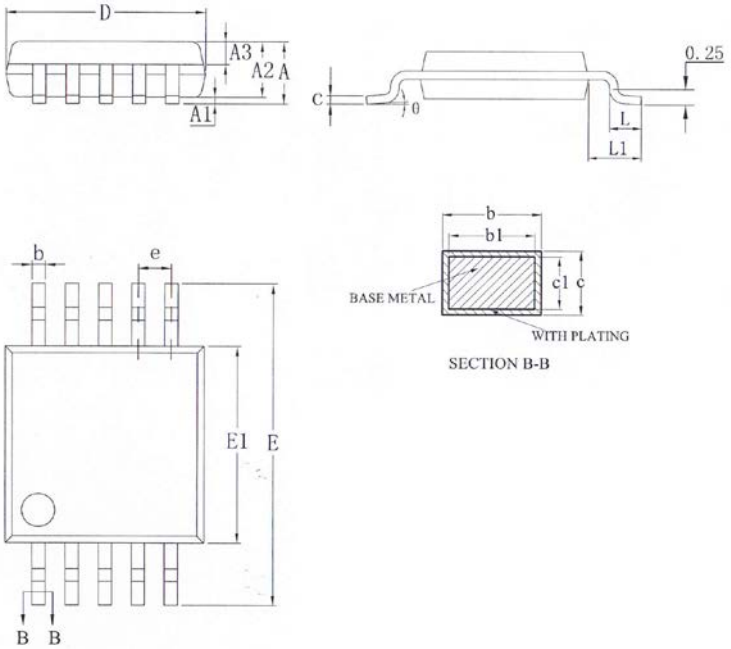



*Figure 4. Timing Diagram*

The conversion is initiated on the falling edge of $\overline{CS}$. The device outputs data while the conversion is in progress, and it requires 16 serial clock cycles to complete the conversion and access the full results. The XADC084S021 data word contains 4 leading zeros, followed by 8-bit data and 4 trailing zeros in MSB first format.

Once a data transfer is complete, DOUT will return to the tri-state mode, and another conversion can be initiated after the quiet time has elapsed by again bringing $\overline{CS}$ low.

# OUTLINE DIMENTIONS




| SYMBOL | MILLIMETER | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | — | — | 1.10 |
| A1 | 0.05 | — | 0.15 |
| A2 | 0.75 | 0.85 | 0.95 |
| A3 | 0.30 | 0.35 | 0.40 |
| b | 0.18 | — | 0.26 |
| b1 | 0.17 | 0.20 | 0.23 |
| c | 0.15 | — | 0.19 |
| c1 | 0.14 | 0.15 | 0.16 |
| D | 2.90 | 3.00 | 3.10 |
| E | 4.70 | 4.90 | 5.10 |
| E1 | 2.90 | 3.00 | 3.10 |
| e | 0.50BSC | | |
| L | 0.40 | — | 0.70 |
| L1 | 0.95REF | | |
| θ | 0 | — | 8° |

# NOTES

1. Unpacked ICs, tube-mounted ICs, etc. must be stored in a drying cabinet, and the humidity in the drying cabinet < 20% R.H.
2. After access, the components are stored in an electrostatic packaging protective bag.
3. Anti-static damage: the device is an electrostatic sensitive device, and sufficient anti-static measures should be taken during transmission, assembly and testing.
4. The user should conduct a visual inspection before use, and the bottom, side and surrounding of the circuit can be welded only if it is bright. If oxidation occurs, the circuit can be processed by means of oxidation, and the circuit must be soldered within 12 hours after processing.