AK09919

3-axis Electronic Compass

1. General Description

AK09919 is 3-axis electronic compass IC with high sensitive Hall sensor technology.
Small package of AK09919 incorporates magnetic sensors for detecting terrestrial magnetism in the X-axis, Y-axis, and Z-axis, a sensor driving circuit, signal amplifier chain, and an arithmetic circuit for processing the signal from each sensor. Self-test function is also incorporated. From its compact foot print and thin package feature, it is suitable for map heading up purpose in Smart phone to realize pedestrian navigation function.

2. Features

- Functions:
  - 3-axis magnetometer device suitable for compass application
  - Built-in A to D Converter for magnetometer data out
  - 16-bit data out for each 3-axis magnetic component
    - Sensitivity: 0.15 μT/LSB (typ.)
  - Serial interface
    - I3C bus interface
      Compliant with MIPI I3C v1.0 specification
  - Operation mode
    - Power-down, Single measurement, Continuous measurement and Self-test
  - Magnetic sensor overflow monitor function
  - Built-in oscillator for internal clock source
  - Power On Reset circuit
  - Self-test function with internal magnetic source
  - Built-in magnetic sensitivity adjustment circuit
  - 16 FIFO data buffer

- Operating temperatures:
  - -30˚C to +85˚C
- Operating supply voltage:
  - +1.65 V to +1.95 V
- Current consumption:
  - Power-down: 1 μA (typ.)
  - Measurement:
    - Average current consumption at 100 Hz repetition rate: 1.1 mA (typ.)

- Package:
  - AK09919C 4-pin WL-CSP (BGA): 0.8 mm × 0.8 mm × 0.5 mm

3. Table of Contents

4. Block Diagram and Functions

4.1. Block Diagram

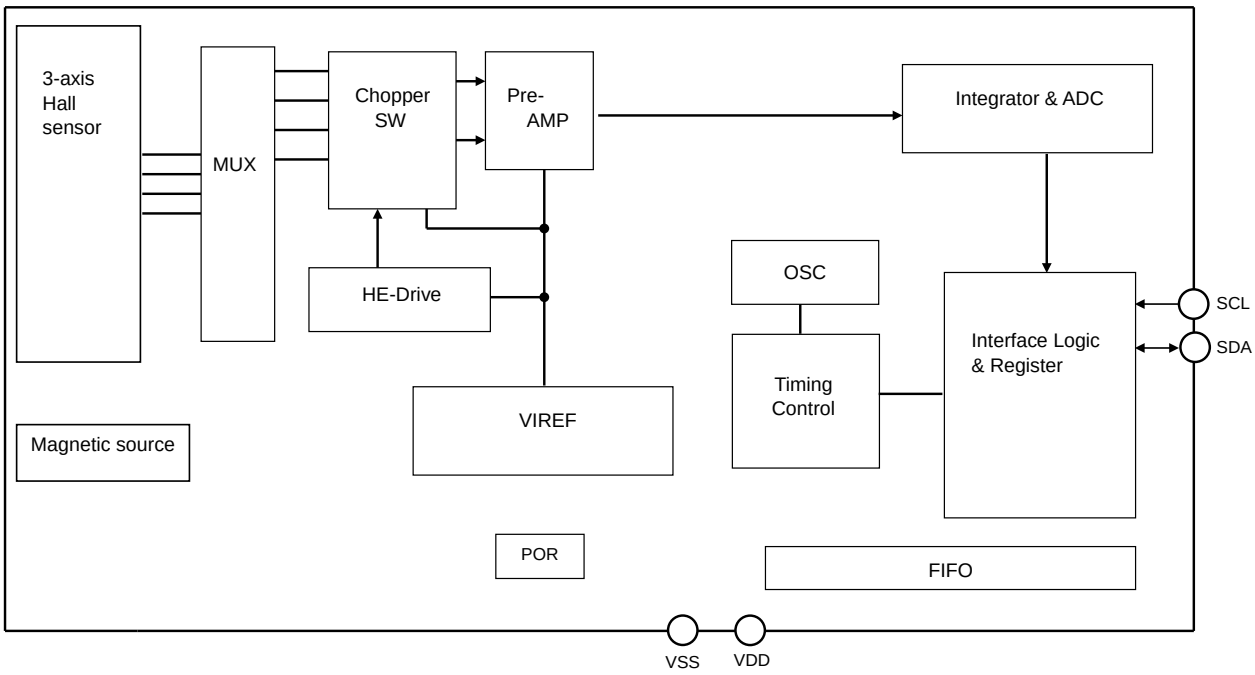


Figure 4.1. Block diagram

4.2. Functions

Block	Function
3-axis Hall sensor	Monolithic Hall elements.
MUX	Multiplexer for selecting Hall elements.
Chopper SW	Performs chopping.
HE-Drive	Magnetic sensor drive circuit.
Pre-AMP	Fixed-gain differential amplifier used to amplify the magnetic sensor signal.
Integrator & ADC	Integrates and amplifies Pre-AMP output and performs analog-to-digital conversion.
OSC	Generates an operating clock for sensor measurement.
POR	Power On Reset circuit. Generates reset signal on rising edge of VDD.
VIREF	Generates reference voltage and current.
Interface Logic & Register	Exchanges data with an external CPU. I3C bus interface using two pins, namely, SCL and SDA.
Timing Control	Generates a timing signal required for internal operation from a clock generated by the OSC.
Magnetic Source	Generates magnetic field for self-test of magnetic sensor.
FIFO	The buffer is capable up to 16 sets of data.

5. Pin Configurations and Functions

Pin No.	Pin name	I/O	Type	Function
A1	VSS	-	-	Ground pin.
A2	SCL	I	CMOS	Control data clock input pin. Input: Schmitt trigger.
B1	VDD	-	Power	Positive power supply pin.
B2	SDA	I/O	CMOS	Control data input/output pin. Input: Schmitt trigger, Output: Open-Drain and Push-Pull.

6. Absolute Maximum Ratings

Vss = 0 V

Parameter	Symbol	Min.	Max.	Unit
Power supply voltage	Vdd	-0.3	+2.5	V
Input voltage (except for power supply pin)	VIN	-0.3	Vdd + 0.3	V
Input current (except for power supply pin)	IIN	-10	+10	mA
Storage temperature	Tst	-40	+125	˚C

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

7. Recommended Operating Conditions

Vss = 0 V

Parameter	Symbol	Min.	Typ.	Max.	Unit
Operating temperature	Ta	-30		+85	˚C
Power supply voltage	Vdd	1.65	1.8	1.95	V
Input voltage	VIN	1.1	1.8	Vdd	V

WARNING: AKM assumes no responsibility for the usage beyond the conditions in this data sheet.

8. Electrical Characteristics

The following conditions apply unless otherwise noted:
Vdd = 1.65 V to 1.95 V, VIN = 1.1 V to Vdd, Temperature range = -30˚C to +85˚C.
Typical condition: Vdd = VIN = 1.8 V, Temperature = +25˚C.

8.1. DC Characteristics

Parameter	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
High level input voltage	VIH	SCL SDA		0.95		Vdd	V
Low level input voltage	VIL			-0.3		0.42	V
Input current	IIN		VIN = Vss or Vdd	-10		+10	µA
Hysteresis input voltage (* 1)	VHS			0.15			V
High level output voltage (* 2)	VOH1	SDA	IOH1 ≥ -0.1 mA VIN ≥ 1.4 V	VIN - 0.27		VIN + 0.3	V
	VOH2		IOH2 ≥ -0.1 mA VIN < 1.4 V	VIN - 0.18		VIN + 0.3	V
Low level output voltage (* 3)	VOL	SDA	IOL ≤ +3 mA			0.18	V
Current consumption (* 4)	IDD1	VDD	Power-down mode Vdd = VIN = 1.95 V		1	5	µA
	IDD2		When magnetic sensor is driven		1.5	3	mA
	IDD3		Self-test mode		2.6	4	mA

Notes:
* 1. Schmitt trigger input (reference value for design).
* 2. Output is Push-Pull.
* 3. Output is Open-Drain and Push-Pull. Connect a pull-up resistor externally in Open-Drain mode.
* 4. Without any resistance load. It does not include the current consumed by external loads (pull-down resistor, etc.). SDA = SCL = VIN or 0 V.

8.2. AC Characteristics

Parameter	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
Power supply rise time (* 5)	PSUP	VDD	Period of time that VDD changes from 0.2 V to Vdd.			50	ms
POR completion time (* 5)	PORT		Period of time after PSUP to Power-down mode (* 6)			100	µs
Power supply turn off voltage (* 5)	SDV	VDD	Turn off voltage to enable POR to restart (* 6)			0.2	V
Power supply turn on interval (* 5)	PSINT	VDD	Period of time that voltage lower than SDV needed to be kept to enable POR to restart (* 6)	100			µs
Wait time before mode setting	Twait			100			µs

Notes:
* 5. Reference value for design.
* 6. When POR circuit detects the rise of VDD voltage, it resets internal circuits and initializes the registers. After reset, AK09919 transits to Power-down mode.

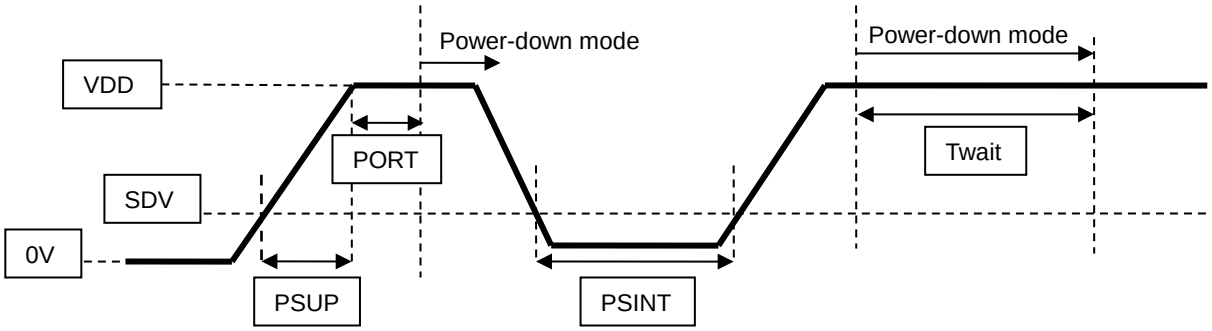


Figure 8.1. Voltage waveform of VDD

8.3. Analog Circuit Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Measurement data output bit	DBIT		-	16	-	bit
Time for measurement	TSM	Single measurement mode		7.2	8.2	ms
Magnetic sensor sensitivity	BSE	Ta = 25˚C	0.1425	0.15	0.1575	µT/LSB
Magnetic sensor measurement range (* 7)	BRG	Ta = 25˚C	±4670	±4912	±5160	µT
Magnetic sensor initial offset (* 8)	BOF	Ta = 25˚C	-2000		+2000	LSB

Notes:
* 7. Reference value for design.
* 8. Value of measurement data register on shipment test without applying magnetic field on purpose.

8.4. I3C Bus Interface

8.4.1. I²C Mode

Parameter	Symbol	Min.	Typ.	Max.	Unit
SCL clock frequency	fSCL			400	kHz
START Condition setup time	tSU_STA	600			ns
START Condition hold time	tHD_STA	600			ns
SCL clock “Low” time	tLOW	1300			ns
SCL clock “High” time	tHIGH	600			ns
SDA setup time	tSU_DAT	100			ns
SDA hold time	tHD_DAT	-		-	ns
SCL rise time	trCL	20		300	ns
SCL fall time	tfCL			300	ns
SDA rise time	trDA	20		300	ns
SDA fall time	tfDA			300	ns
STOP Condition setup time	tSU_STO	600			ns
Bus free time	tBUF	1.3			µs

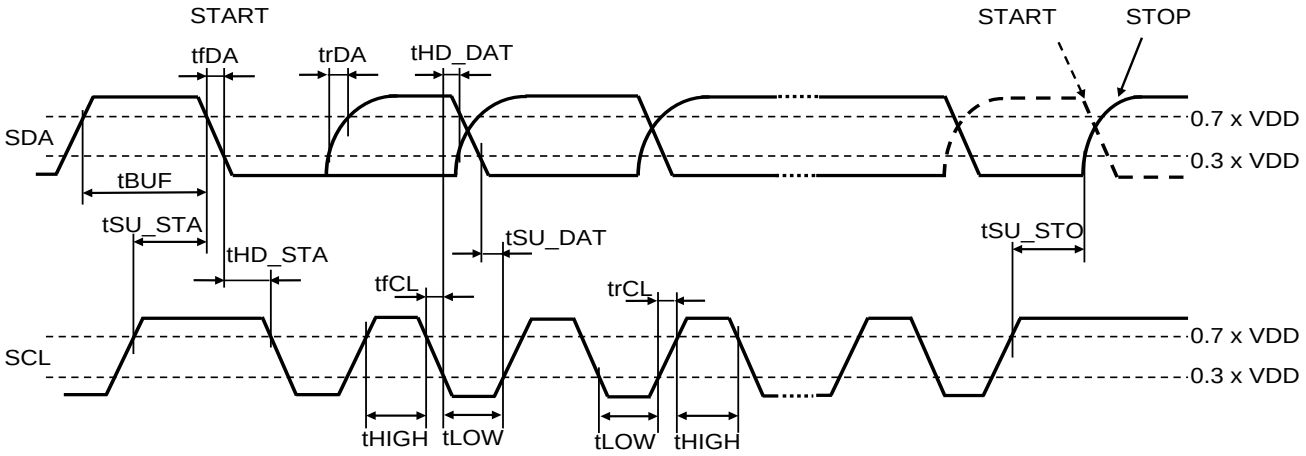


Figure 8.2. I²C Mode timing

8.4.2. I3C Mode

I3C bus interface is compliant with Open-Drain mode and Push-Pull mode. Open-Drain/Push-Pull mode is selected automatically by I3C function.

☐ Open-Drain mode

Parameter	Symbol	Min.	Typ.	Max.	Unit
SCL clock “High” time	tHIGH			41	ns
SCL clock “Low” time	tLOW_OD	200			ns
SDA fall time	tfDA_OD			12	ns
SDA setup time	tSU_OD	3			ns
START Condition hold time	tCAS	38.4			ns
STOP Condition setup time	tCBP	19.2			ns
Bua available condition	tAVAL	1			µs
Bus idle condition	tIDLE	1			µs

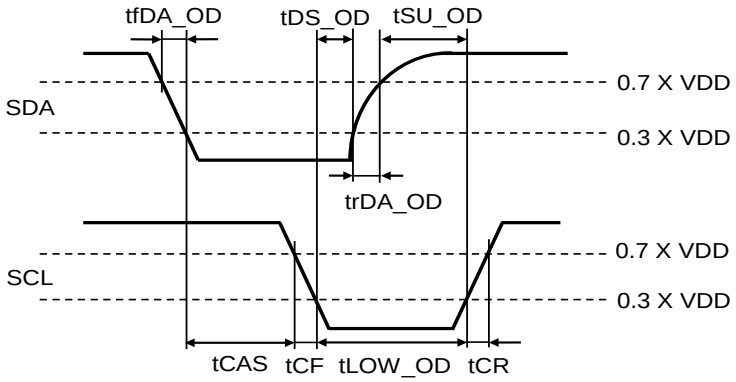


Figure 8.3. START condition timing (Open-Drain mode)

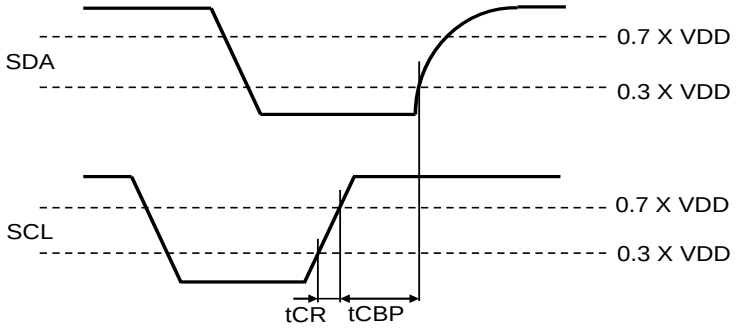


Figure 8.4. STOP condition timing (Open-Drain mode)

☐ Push-Pull mode

Parameter	Symbol	Min.	Typ.	Max.	Unit
SCL clock frequency	fSCL	0.01	12.5	12.9	MHz
SCL clock “High” time	tHIGH	24.0			ns
SCL clock “Low” time	tLOW	24.0			ns
Clock in to Data Out	tSCO			12.0	ns
SCL rise time	tCR			150*1/fSCL	ns
SCL fall time	tCF			150*1/fSCL	ns
SDA setup time	tSU_PP	3			ns
Capacitive Load per Bus Line (SDA/SCL)	Cb			50	pF

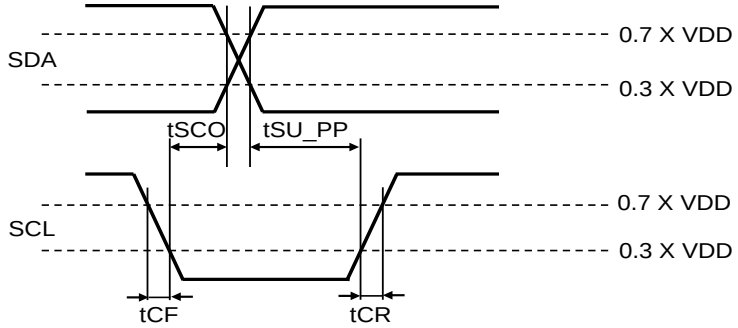


Figure 8.5. Data Output timing (Push-Pull mode)

9. Functional Descriptions

9.1. Power States

When VDD is turned ON from Vdd = OFF (0 V), all registers in AK09919 are initialized by POR circuit and AK09919 transits to Power-down mode.

Table 9.1. Power States

State	VDD	Power state
1	OFF (0 V)	OFF (0 V). It does not affect external interface.
2	1.65 V to 1.95 V	ON.

9.2. Reset Functions

Power On Reset (POR) works until Vdd reaches to the operation effective voltage (about 1.2 V: reference value for design) on power-on sequence. After POR is completed, all registers are initialized and AK09919 transits to Power-down mode.

When Vdd = 1.65 to 1.95 V, POR circuit is active.

AK09919 has two types of reset;

(1) Power On Reset (POR)
When Vdd rise is detected, POR circuit operates, and AK09919 is reset.

(2) Soft reset
AK09919 is reset by setting SRST bit.

After reset is completed, all registers and FIFO buffer are initialized and AK09919 transit to Power-down mode automatically.

9.3. Operation Modes

AK09919 has following eight operation modes:
(1) Power-down mode
(2) Single measurement mode
(3) Continuous measurement mode 1
(4) Continuous measurement mode 2
(5) Continuous measurement mode 3
(6) Continuous measurement mode 4
(7) Continuous measurement mode 5
(8) Self-test mode

By setting CNTL2 register MODE[4:0] bits, the operation set for each mode is started. A transition from one mode to another is shown below.

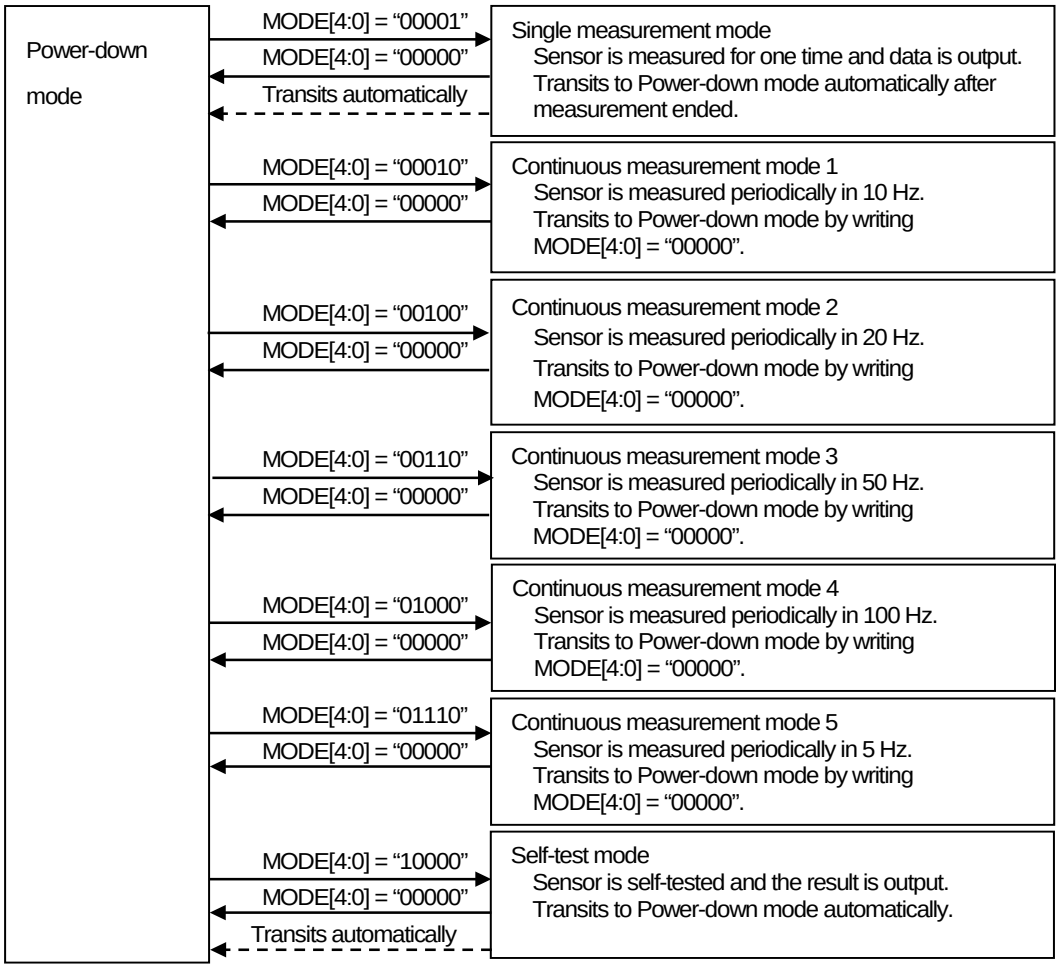


Figure 9.1. Operation mode

When power is turned ON, AK09919 is in Power-down mode. When a specified value is set to MODE[4:0] bits, AK09919 transits to the specified mode and starts operation. When user wants to change operation mode, transit to Power-down mode first and then transit to other modes. After Power-down mode is set, at least 100 μs (Twait) is needed before setting another mode.

9.4. Description of Each Operation Mode

9.4.1. Power-down Mode

Power to almost all internal circuits is turned off. All registers are accessible in Power-down mode. Data stored in read/write registers are remained. They can be reset by soft reset.

9.4.2. Single Measurement Mode

When Single measurement mode (MODE[4:0] bits = “00001”) is set, magnetic sensor measurement is started. After magnetic sensor measurement and signal processing is finished, Measurement Magnetic Data is stored to measurement data registers (HXH to HZL), then AK09919 transits to Power-down mode automatically. On transition to Power-down mode, MODE[4:0] bits turn to “00000”. At the same time, DRDY bit in ST1 register turns to “1”. This is called “Data Ready”. When any of measurement data register (HXH to TMPS) or ST2 register is read, DRDY bit turns to “0”. It remains “1” on transition from Power-down mode to another mode. (Figure 9.2.)

When sensor is measuring (Measurement period), measurement data registers (HXH to TMPS) keep the previous data. Therefore, it is possible to read out data even in Measurement period. Data read out in Measurement period are previous data. (Figure 9.3.)

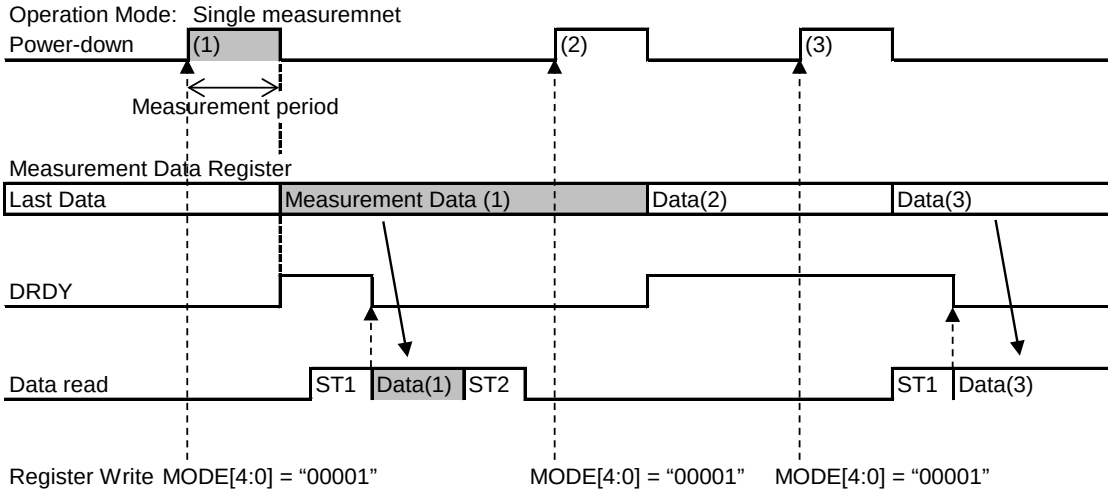


Figure 9.2. Single measurement mode when data is read out of measurement period

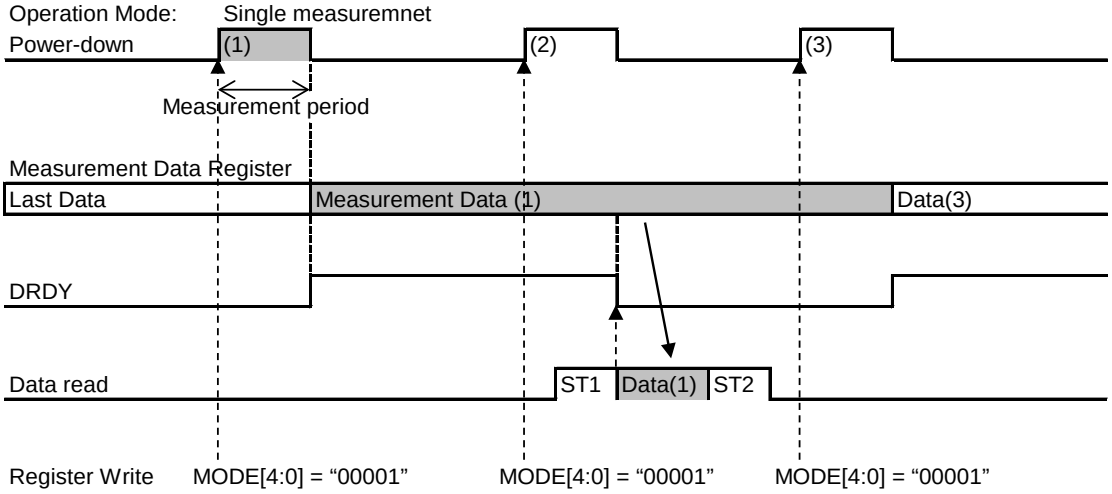


Figure 9.3. Single measurement mode when data read started during measurement period

9.4.3. Continuous Measurement Modes

When Continuous measurement modes (1 to 5) are set, magnetic sensor measurement is started periodically at 10 Hz, 20 Hz, 50 Hz, 100 Hz or 5 Hz respectively. After magnetic sensor measurement and signal processing is finished, Measurement Magnetic Data is stored to measurement data registers (HXH to HZL) and all circuits except for the minimum circuit required for counting cycle length are turned off (PD). When the next measurement timing comes, AK09919 wakes up automatically from PD and starts measurement again. Continuous measurement mode ends when Power-down mode (MODE[4:0] bits = “00000”) is set. It repeats measurement until Power-down mode is set.

When Continuous measurement modes (1 to 5) are set again while AK09919 is already in Continuous measurement mode, a new measurement starts. ST1, ST2 and measurement data registers (HXH to TMPS) will not be initialized by this.

Table 9.2. Continuous measurement modes

Operation mode	Register setting (MODE[4:0] bits)	Measurement frequency [Hz]
Continuous measurement mode 1	00010	10
Continuous measurement mode 2	00100	20
Continuous measurement mode 3	00110	50
Continuous measurement mode 4	01000	100
Continuous measurement mode 5	01110	5

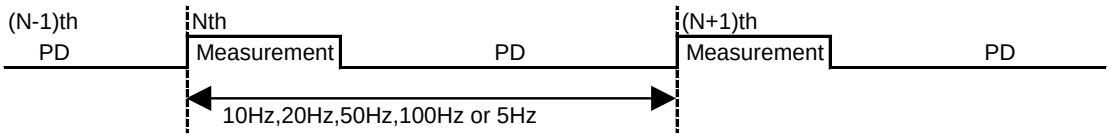


Figure 9.4. Continuous measurement mode

9.4.3.1. Data Ready

When measurement data is stored and ready to be read, DRDY bit in ST1 register turns to “1”. This is called “Data Ready”. When measurement is performed correctly, AK09919 becomes Data Ready on transition to PD after measurement.

9.4.3.2. Normal Read Sequence

(1) Check Data Ready or not by polling DRDY bit of ST1 register
DRDY: Shows Data Ready or not. Not when “0”, Data Ready when “1”.
DOR: Shows if any data has been skipped before the current data or not. There are no skipped data when “0”, there are skipped data when “1”.

(2) Read measurement data
When any of measurement data register (HXH to TMPS) or ST2 register is read, AK09919 judges that data reading is started. When data reading is started, DRDY bit and DOR bit turns to “0”.

(3) Read ST2 register (required)
HOFL: Shows if magnetic sensor is overflowed or not. “0” means not overflowed, “1” means overflowed.

When ST2 register is read, AK09919 judges that data reading is finished. Stored measurement data is protected during data reading and data is not updated. By reading ST2 register, this protection is released. It is required to read ST2 register after data reading.

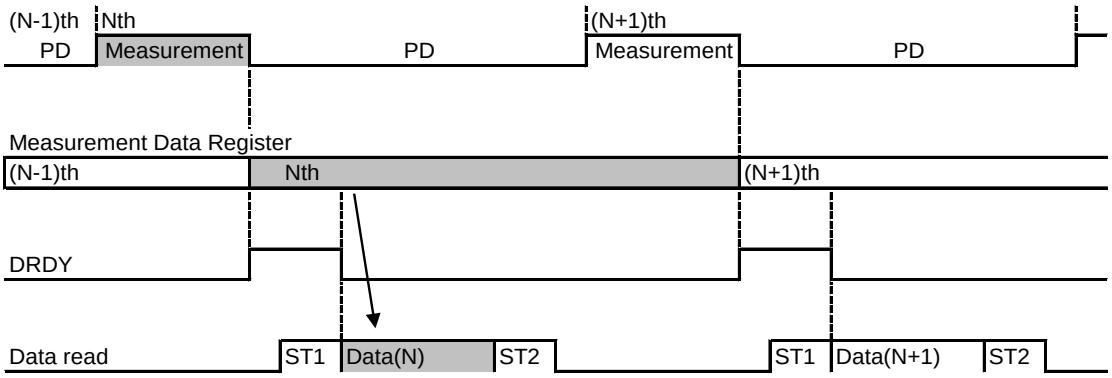


Figure 9.5. Normal read sequence

9.4.3.3. Data Read Start during Measurement

When sensor is measuring (Measurement period), measurement data registers (HXH to TMPS) keep the previous data. Therefore, it is possible to read out data even in Measurement period. If data is started to be read during Measurement period, previous data is read.

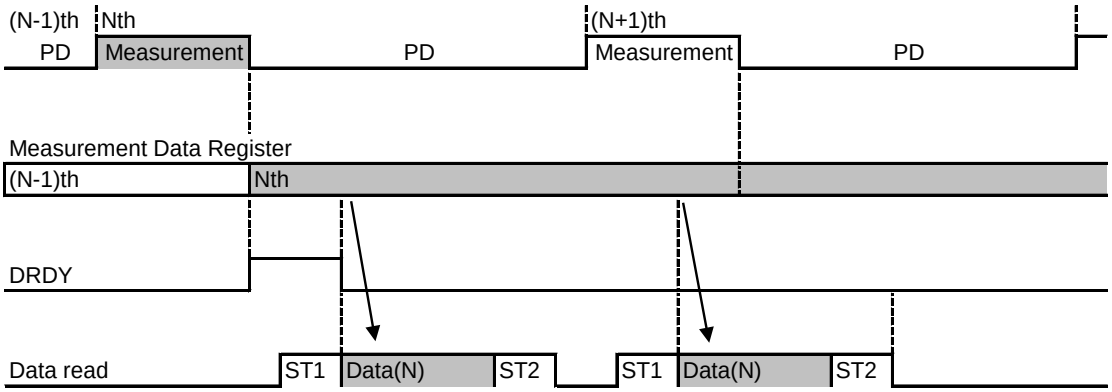


Figure 9.6. Data read start during measuring

9.4.3.4. Data Skip

When Nth data was not read before (N+1)th measurement ends, Data Ready remains until data is read. In this case, a set of measurement data is skipped so that DOR bit turns to “1”.
When data reading started after Nth measurement ended and did not finish reading before (N+1)th measurement ended, Nth measurement data is protected to keep correct data. In this case, a set of measurement data is skipped and not stored so that DOR bit turns to “1”.
In both cases, DOR bit turns to “0” at the next start of data reading.

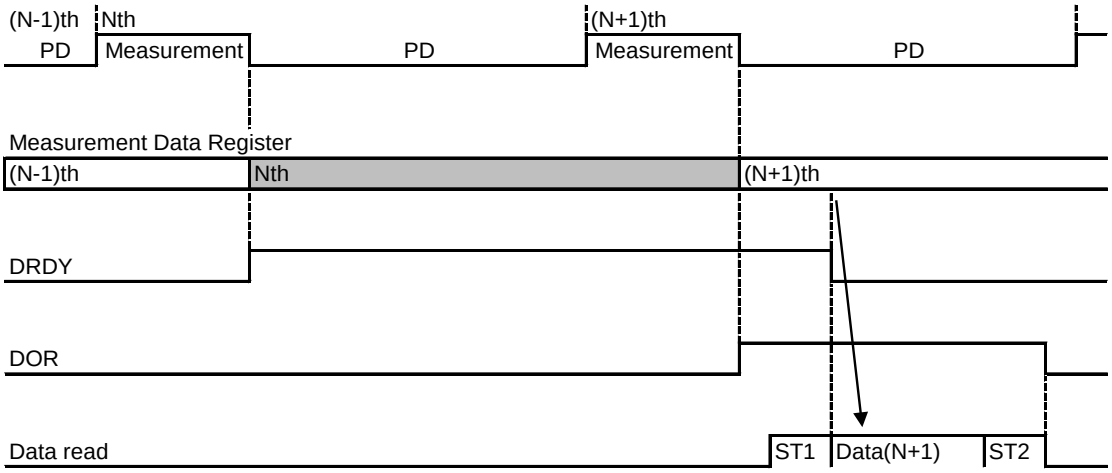


Figure 9.7. Data Skip: When data is not read

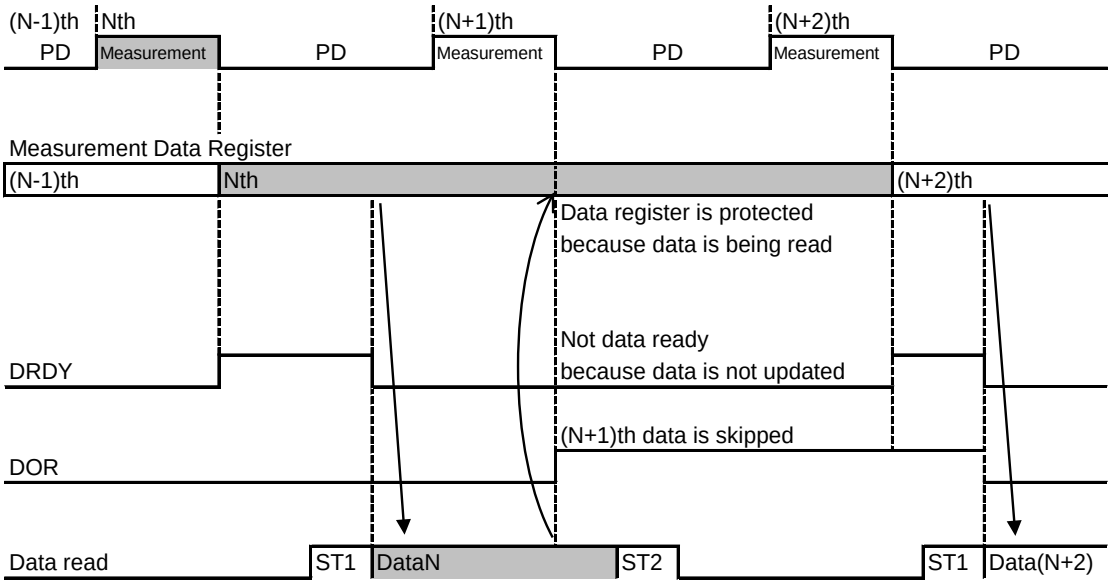


Figure 9.8. Data Skip: When data read has not been finished before the next measurement end

9.4.3.5. End Operation

Set Power-down mode (MODE[4:0] = “00000”) to end Continuous measurement mode.

9.4.3.6. Magnetic Sensor Overflow

AK09919 has the limitation for measurement range that the sum of absolute values of each axis should be smaller than 4912 μT. (* 9)

$$|X| + |Y| + |Z| < 4912\ \mu T$$

When the magnetic field exceeded this limitation, data stored at measurement data are not correct. This is called Magnetic Sensor Overflow.
When Magnetic Sensor Overflow occurs, HOFL bit turns to “1”.
When measurement data register (HXH to HZL) is updated, HOFL bit is updated.
Notes:
* 9. BSE: 0.15 μT/LSB

9.4.4. Self-test Mode

Self-test mode is used to check if the magnetic sensor is working normally.
When Self-test mode (MODE[4:0] bits = “10000”) is set, magnetic field is generated by the internal magnetic source and magnetic sensor is measured. Measurement data is stored to measurement data registers (HXH to HZL), then AK09919 transits to Power-down mode automatically.
Data read sequence and functions of read-only registers in Self-test mode is the same as Single measurement mode.

9.4.4.1. Self-test Sequence

(1) Set Power-down mode. (MODE[4:0] bits = “00000”)
(2) Set Self-test mode. (MODE[4:0] bits = “10000”)
(3) Check Data Ready or not by polling DRDY bit of ST1 register.
When Data Ready, proceed to the next step.
(4) Read measurement data (HXH to HZL)

9.4.4.2. Self-test Judgment

When measurement data read by the above sequence is in the range of following table, AK09919 is working normally.

	HX[15:0] bits	HY[15:0] bits	HZ[15:0] bits
Criteria	-200 ≤ HX ≤ 200	-200 ≤ HY ≤ 200	-1000 ≤ HZ ≤ -150

9.5. Low Noise Drive

AK09919 has Low noise drive. Low noise drive is available only in Continuous measurement modes.
Low noise drive is enabled by setting SDR bit = “1”, and the noise suppression level can be changed by setting ITS[1:0] bits (Table 9.3.).
SDR bit and ITS[1:0] bits can be changed in Power-down mode only. Default SDR bit is Low noise drive disable (SDR bit = “0”).

Table 9.3. Low noise drive settings

Register setting (ITS[1:0] bits)	Noise suppression level
00	Off
01	Low
10, 11	High

9.6. FIFO

FIFO function is available in Continuous measurement modes. FIFO function is enabled by setting FIFO bit = “1”. It is prohibited to enable FIFO function in any modes other than Continuous measurement modes.

When FIFO function is enabled, Measurement Magnetic Data (HXH to HZL) and HOFL bit are stored to the buffer as a set of data. The buffer is capable up to 16 sets of data. If a new data is measured when 16 sets of data are already stored, the oldest data set is deleted and the new data set is stored. If measurement data registers are read when FIFO function is enabled, the oldest data set is read as first-in first-out method.

When reading out data from the buffer, always start with HXH register and finish with ST2 register. By accessing HXH register, the oldest data set is loaded to the measurement data registers from the buffer. Reading ST2 register is regarded as the finish of reading out one set of data. Then the read data set is deleted, and the next oldest data set will be ready to be read. If ST2 register or HXH register is not read, the same set of data is kept in the measurement data registers.

When FIFO function is enabled, DRDY bit and DOR bit functions differently. DRDY bit informs that data set is stored up to Watermark. Refer to 9.6.1. for details. DOR bit informs that data set is overflowed from the buffer. If a set of new data is measured when the buffer is full, DOR bit turns to “1”. If at least one data set is read from the buffer, DOR bit turns to “0”.

If data is read out when the buffer is empty, INV bit is turned to “1”, and measurement data registers (HXH to HZL) are forced to fixed value 7FFFh. If a set of new data is measured, INV bit turns to “0”.

When AK09919 is reset (refer to 9.2.), FIFO buffer is initialized.

9.6.1. Watermark

When FIFO function is enabled, Watermark function is available. By setting WM[3:0] bits, AK09919 informs that data set is stored up to or more than Watermark. If the number of stored data set is equal to or more than the number set to WM[3:0] bits, DRDY bit turns to “1”. If the number of stored data set is less than the number set to WM[3:0] bits, DRDY bit turns to “0”.
WM[3:0] bits should be changed in the Power-down mode only. It is prohibited to write WM[3:0] bits in other modes.

9.6.2. FIFO status

When FIFO function is enabled, AK09919 can be use FNUM register for monitor of FIFO.

9.7. In-Band Interrupt (IBI)

AK09919 supports In-Band Interrupt (IBI) using the SDA line.
The IBI can be used only in I3C SDR mode. After setting AK09919 to I3C SDR mode, set IBI_EN bit = "1" with the CCC (ENEC).

When IBI is enabled and each measurement mode is set, AK09919 starts magnetic measurement and monitoring of the I3C Bus. When the measurement is completed and it is determined that the bus is free, AK09919 drives the SDA line low and generates a START condition.
After AK09919 generates a START condition, AK09919 sends its own Dynamic Address and R/W bit = "1" in Open-Drain. AK09919 receives an acknowledgment from the Master and completes the IBI. If AK09919 fails to transmit its own address (another device drives SDA) and no acknowledgment is returned from the Master, wait for bus free status and perform IBI again. AK09919 repeats until IBI is completed.

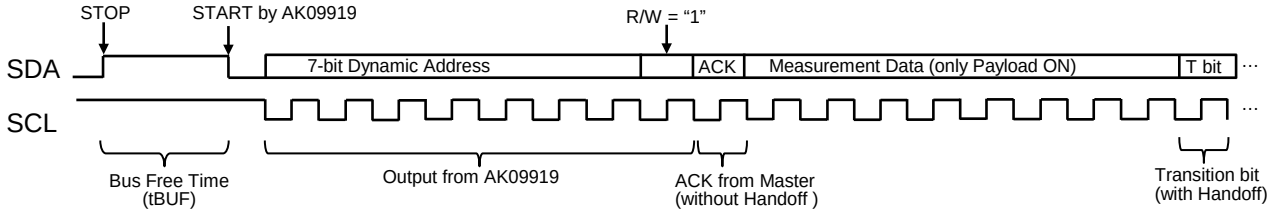


Figure 9.9. In-Band Interrupt Data format

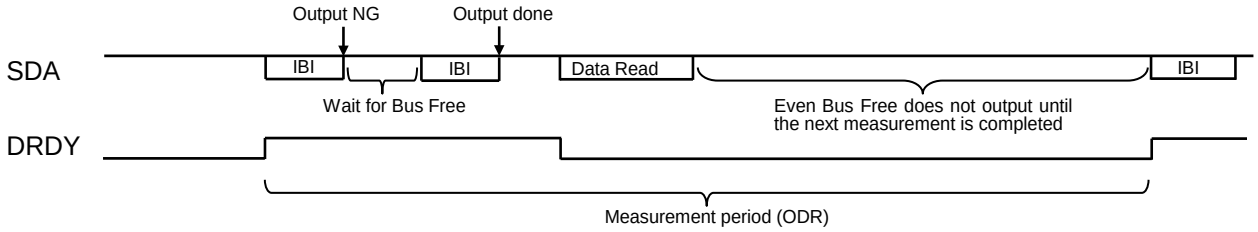


Figure 9.10. In-Band Interrupt output flow

9.7.1. IBI Payload

When IBI is enabled and IBIP in the CTRL2 register is set to "1", AK09919 transfers 8 bytes of data (HXH to ST2) after IBI completes. When using IBI Payload, ACK from the Master is without Handoff. This is different from the MIPI I3C v1.0 specification. Therefore, BCR[2] bit is "0" (Table 10.8.). Stored measurement data is protected during data reading and data is not updated. By reading ST2 register, this protection is released. It is required to read HXH to ST2 registers. IBI Payload can not be used in FIFO mode. When FIFO function is enabled, read data by normal read access.

10. Serial Interface

10.1. I3C Bus Interface

The I3C Bus interface of AK09919 supports the I²C mode (400 kHz max.) and the I3C Single Data Rate (SDR) mode (12.9 MHz max.).

10.1.1. Bus Protocol Configuration

Protocol	Bit length	Description	Abbreviation
START condition	-	Input at the start of communication	S
Slave Address	7	Select Slave Device	-
Read/Write control bit	1	0: write 1: read	R/W
Register Address	8	Set access address	-
Control data	8	Write/Read data	-
Repeated START	-	Two or more instance of a START in a row without an intervening STOP	Sr
STOP condition	-	Input at the end of communication	P
Acknowledge	-	Generated when receiving data	ACK
Transition Bit	-	Generated when sending data	T
Parity Bit	-	Received when writing data	PAR
HDR Exit Pattern	-	Entered when returning from error condition	-

10.1.1.1. START/STOP Condition

If the SDA line is driven to “Low” from “High” when the SCL line is “High”, a START condition is generated. Every instruction starts with a START condition.
If the SDA line is driven to “High” from “Low” when the SCL line is “High”, a STOP condition is generated. Every instruction stops with a STOP condition.
The I3C START and STOP are identical to the I²C START and STOP in their signaling, but they may vary from I²C in their timing. Refer to 8.4.1. and 8.4.2. .

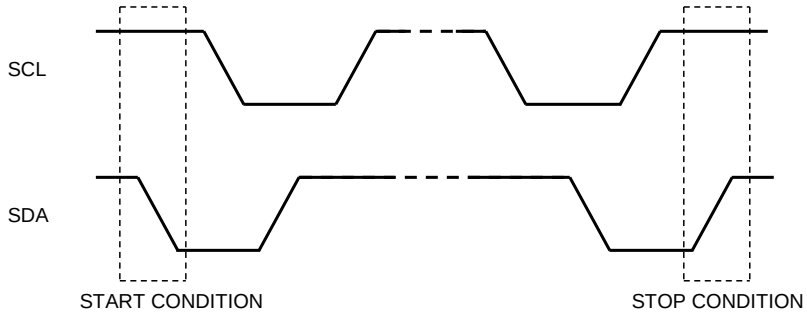


Figure 10.1. START and STOP Condition

10.1.1.2. Acknowledge

The IC that is transmitting data releases the SDA line (in the “High” state) after sending 1-byte data. The IC that receives the data drives the SDA line to “Low” on the next clock pulse. This operation is referred as acknowledge. With this operation, whether data has been transferred successfully can be checked.

In I^2C mode, AK09919 generates an acknowledge after reception of a START condition and Slave Address. When a WRITE instruction is executed, AK09919 generates an acknowledge (without Handoff) after every byte is received. When a READ instruction is executed, AK09919 generates an acknowledge (without Handoff) then transfers the data stored at the specified address. Next, AK09919 releases the SDA line then monitors the SDA line. If a Master generates an acknowledge instead of a STOP condition, AK09919 transmits the 8 bits data stored at the next address. If no acknowledge is generated, AK09919 stops data transmission.
AK09919 generates an acknowledge after reception of a START condition and Broadcast Address (7’h7E). When a WRITE instruction is executed, AK09919 generates an acknowledge (with Handoff). When a READ instruction is executed, AK09919 generates an acknowledge (without Handoff).
.
In I3C SDR mode, AK09919 generates an acknowledge after reception of a START condition and under following conditions.

(1) When receiving its own Dynamic Address.
(2) When a Broadcast Address is received.
(3) When a Slave Address is received by Dynamic Address Assignment.

In case of (1), when the R/W bit is set to “1”, it returns one clock (without Handoff), and when R/W bit is set to “0”, it returns an acknowledge of half clock (with Handoff). In case of (2), when the R/W bit is set to “0”, it returns an acknowledge of half clock (with Handoff). In case of (3), it returns an acknowledge of one clock (without Handoff).

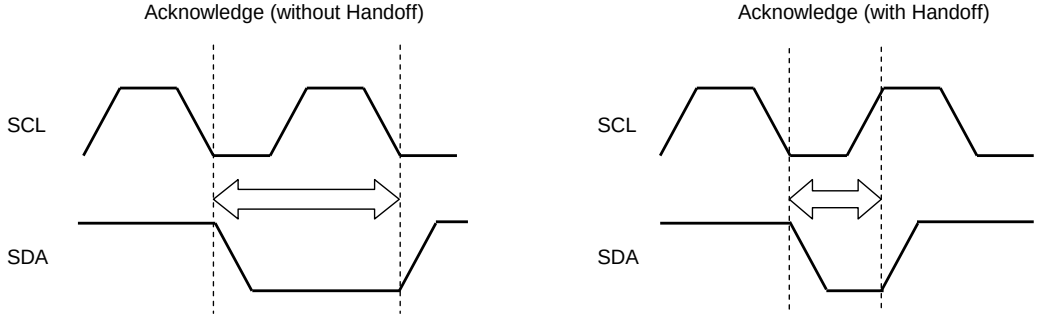


Figure 10.2. Generation of Acknowledge

10.1.1.3. Transition-Bit (T-Bit)

In I3C, the data words match I^2C only in the sense that they are both 9 bits long.
In I^2C, the ninth data bit written by the Master is an acknowledge by the Slave. By contrast, in I3C the ninth data bit written by the Master is the parity of the preceding eight data bits. In SDR terms, the ninth bit of write data is referred to as the T-Bit (for 'Transition'). The ninth data bit of each SDR data word written by the I3C Master (also referred to as the T-Bit) is a Parity bit, calculated using odd parity. Parity can help in detecting noise-caused errors on the line. The value of this parity bit shall be the XOR of the 8 data bits with 1, i.e.: XOR(Data [7:0], 1).
T (Parity) bit writes shall always be kept valid through the SCL high period. In the case of a T-Bit representing the last data byte, the write is therefore kept valid through the SCL high period, and the next SCL low can then be used to either change the SDA, or not change the SDA, in preparation for the Repeated START condition or STOP condition that follows.
If parity is different, AK09919 will not receive data.

In I^2C, the ninth data bit from Slave to Master is an acknowledge by the Master. By contrast, in I3C this bit allows the Slave to end a read and allows the Master to abort a read. In SDR terms, the ninth bit of read data is referred to as the T-Bit (for 'Transition').
If transmission of the number of bytes set by SETMRL has not been completed, AK09919 generates T-Bit = "1" and transmits data at the next address from the falling edge of SCL after that. When transmission of the number of bytes set by SETMRL is completed, AK09919 generates T-Bit = "0" and then releases the SDA line.

10.1.1.4. Slave Address

The Slave Address of AK09919 is 7'h0E.

MSB							LSB
0	**0**	**0**	**1**	**1**	**1**	**0**	**R/W**

Figure 10.3. Slave Address

The first byte including a Slave Address is transmitted after a START condition, and an IC to be accessed is selected from the ICs on the bus according to the Slave Address.
When a Slave Address is transferred, the IC whose device address matches the transferred Slave Address generates an acknowledge then executes an instruction. The 8th bit (least significant bit) of the first byte is a R/W bit.
When the R/W bit is set to "1", READ instruction is executed. When the R/W bit is set to "0", WRITE instruction is executed.

10.1.1.5. Broadcast Address

The Broadcast Address of Slave devices is 7'h7E.
All I3C Slaves match address value 7'h7E. No I^2C Slave will match address 7'h7E.

MSB							LSB
1	**1**	**1**	**1**	**1**	**1**	**0**	**R/W**

Figure 10.4. Broadcast Address

The first byte including a Broadcast Address is transmitted after a START condition, and all I3C Slaves are selected on the bus.
When a Broadcast Address is transferred, all I3C Slaves generate an acknowledge then executes an instruction. The 8th bit (least significant bit) of the first byte is a R/W bit.
When the R/W bit is set to "1", READ instruction is executed. When the R/W bit is set to "0", WRITE instruction is executed.

10.1.1.6. Dynamic Address

In I²C mode, AK09919 is assigned a Dynamic Address by performing SETDASA or ENTDAA flow. After the flow is completed, AK09919 communicates in I3C SDR mode.

10.1.1.6.1. SETDASA (Set Dynamic Address from Static Address)

The SETDASA CCC is a flow for assigning Dynamic Address based on the Slave Address in the I²C state. AK09919 can assign a Dynamic Address by Direct CCC. The Slave Address of AK09919 is 7'h0E. The newly assigned address is transmitted in the Dynamic Address byte shown in Figure 10.5., where the 7 most significant bits (Bits [7:1]) contain the 7-bit Dynamic Address, and the least significant bit (Bit [0]) is filled with the value 1'b0. If this least significant bit (Bit [0]) has the value 1'b1, AK09919 will not accept the Dynamic Address.

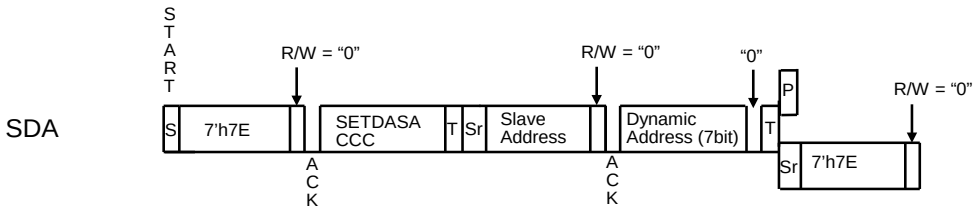


Figure 10.5. SETDASA Format 1: Primary

The SETDASA CCC may also be specially used for simple point-to-point communication in I3C Minimal Bus use cases. An I3C Minimal Bus is an I3C Bus with one I3C Master (potentially with reduced functionality), and one I3C Slave. In this special usage of the SETDASA CCC, the Master both uses the fixed value 7'h01 as the static address, and uses the fixed (and reserved) value of 7'h01 as the Dynamic Address (Figure 10.6.).

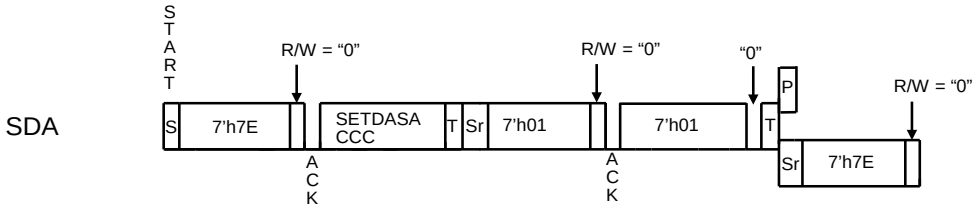


Figure 10.6. SETDASA Format 2: Point-to-Point

10.1.1.6.2. ENTDAA (Enter Dynamic Address Assignment)

The ENTDAA CCC is a flow for assigning Dynamic Address based on the 48-bit Provisional ID (PID), Bus Characteristic Register (BCR) and Device Characteristic Register (DCR). Data input will follow in the flow of Figure 10.7. . The values of AK09919 are PID = 48'h03BA99190000, BCR = 8'h02, DCR = 8'h00 (Table 10.8.).

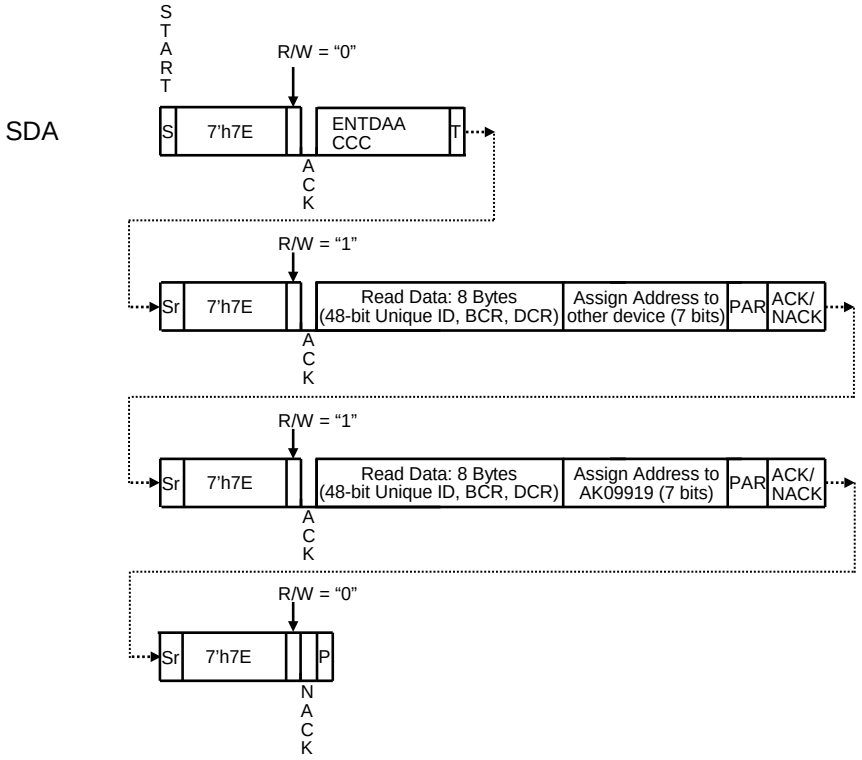


Figure 10.7. Dynamic Address Assignment Transaction

10.1.2. I²C Mode

After power-on or after the soft reset, AK09919 communicates as I²C mode until the Dynamic Address is assigned.

10.1.2.1. WRITE Instruction

When the R/W bit is set to "0", AK09919 performs write operation.
In write operation, AK09919 generates an acknowledge after receiving a START condition and the first byte (Slave Address) then receives the second byte. The second byte is used to specify the address of an internal control register and is based on the MSB-first configuration.

MSB							LSB
A7	**A6**	**A5**	**A4**	**A3**	**A2**	**A1**	**A0**

Figure 10.8. Register Address

After receiving the second byte (register address), AK09919 generates an acknowledge then receives the third byte.
The third and the following bytes represent control data. Control data consists of 8 bits and is based on the MSB-first configuration. AK09919 generates an acknowledge after every byte is received. Data transfer always stops with a STOP condition generated by the Master.

MSB							LSB
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**

Figure 10.9. Control Data

AK09919 can write multiple bytes of data at a time.
After reception of the third byte (control data), AK09919 generates an acknowledge then receives the next data. If additional data is received instead of a STOP condition after receiving one byte of data, the address counter inside the LSI chip is automatically incremented and the data is written at the next address.
The address is incremented from 00h to 10h, from 11h to 18h and from 30h to 32h. When the address is 00h to 10h, the address is incremented 00h → 01h → 02h → 03h → 10h. When the address is 11h to 18h, the address is incremented 11h → 12h → 13h → … → 18h, and the address goes back to 00h after 18h. In the case that FIFO function is enabled, the address is incremented 11h → 12h → 13h → … → 18h, and the address goes back to 11h after 18h. When the address is 30h to 32h, the address goes back to 30h after 32h.
Actual data is written only to Read/Write registers (Table 11.2.).

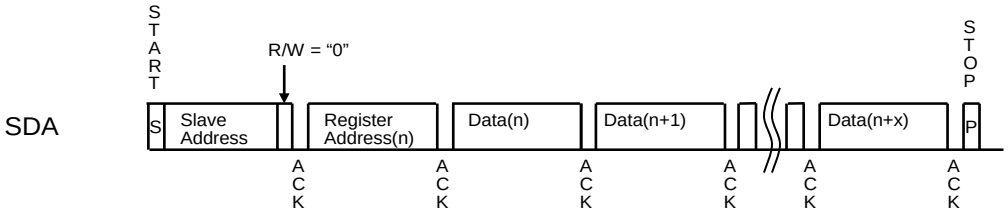


Figure 10.10. WRITE Instruction

10.1.2.2. READ Instruction

When the R/W bit is set to “1”, AK09919 performs read operation.
If a Master generates an acknowledge instead of a STOP condition after AK09919 transfers the data at a specified address, the data at the next address can be read.
The address is incremented from 00h to 10h, from 11h to 18h and from 30h to 32h. When the address is 00h to 10h, the address is incremented 00h → 01h → 02h → 03h → 10h. When the address is 11h to 18h, the address is incremented 11h → 12h → 13h → … → 18h, and the address goes back to 00h after 18h. In the case that FIFO function is enabled, the address is incremented 11h → 12h → 13h → … → 18h, and the address goes back to 11h after 18h. When the address is 30h to 32h, the address goes back to 30h after 32h.

10.1.2.3. Current Address READ

AK09919 has an address counter inside the LSI chip. In current address read operation, the data at an address specified by this counter is read.
The internal address counter holds the next address of the most recently accessed address.
For example, if the address most recently accessed (for READ instruction) is address “n”, and a current address read operation is attempted, the data at address “n+1” is read.
In current address read operation, AK09919 generates an acknowledge after receiving a Slave Address for the READ instruction (R/W bit = “1”). Next, AK09919 transfers the data specified by the internal address counter starting with the next clock pulse, then increments the internal counter by one. If the Master generates a STOP condition instead of an acknowledge after AK09919 transmits one byte of data, the read operation stops.

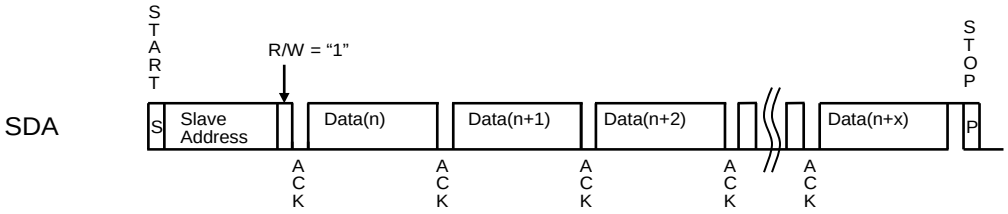


Figure 10.11. Current Address READ

10.1.2.4. Random Address Read

By random address read operation, data at an arbitrary address can be read.
The random address read operation requires to execute WRITE instruction as dummy before a Slave Address for the READ instruction (R/W bit = “1”) is transmitted. In random read operation, a START condition is first generated then a Slave Address for the WRITE instruction (R/W bit = “0”) and a read address are transmitted sequentially.
After AK09919 generates an acknowledge in response to this address transmission, a Repeated START condition and a Slave Address for the READ instruction (R/W bit = “1”) are generated again. AK09919 generates an acknowledge in response to this Slave Address transmission. Next, AK09919 transfers the data at the specified address then increments the internal address counter by one. If the Master generates a STOP condition instead of an acknowledge after data is transferred, the read operation stops.

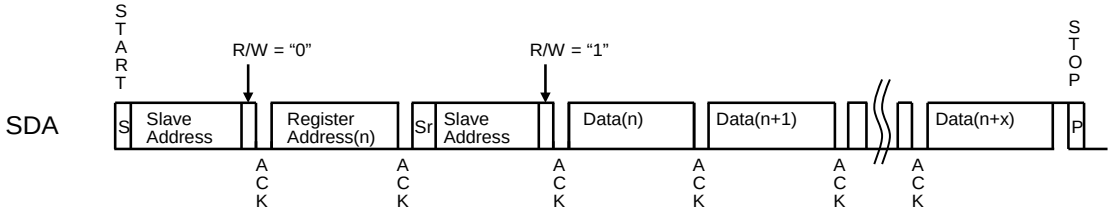


Figure 10.12. Random Address READ

10.1.3. I3C SDR Mode

When Dynamic Address is assigned properly, AK09919 shifts to I3C SDR mode.
I3C SDR mode is significantly similar to the I^2C protocol in terms of procedures and conditions.
In I3C SDR mode, AK09919 can communicate with Private Messages or Common Command Code (CCC).

10.1.3.1. Private Messages

10.1.3.1.1. WRITE Instruction

When the R/W bit is set to "0", AK09919 performs write operation.
In write operation, AK09919 generates an acknowledge (with Handoff) after receiving a START condition and the first byte (Dynamic Address). The second byte is used to specify the address of an internal control register and is based on the MSB-first configuration.
After receiving the second byte (register address), AK09919 receives a T-Bit then receives the third byte.
The third and the following bytes represent control data. Control data consists of 8 bits and is based on the MSB-first configuration. AK09919 generates a T-Bit after every byte is received. Data transfer always stops with a STOP condition generated by the Master.
AK09919 can write multiple bytes of data at a time. The maximum value is determined Max Write Length.
After reception of the third byte (control data), AK09919 receives a T-Bit then receives the next data. If additional data is received instead of a STOP condition after receiving one byte of data, the address counter inside the LSI chip is automatically incremented and the data is written at the next address. The address is incremented from 00h to 10h, from 11h to 18h and from 30h to 32h. When the address is 00h to 10h, the address is incremented 00h → 01h → 02h → 03h → 10h. When the address is 11h to 18h, the address is incremented 11h → 12h → 13h → … → 18h, and the address goes back to 00h after 18h. In the case that FIFO function is enabled, the address is incremented 11h → 12h → 13h → … → 18h, and the address goes back to 11h after 18h. When the address is 30h to 32h, the address goes back to 30h after 32h.
Actual data is written only to Read/Write registers (Table 11.2.).

Table 10.1. I3C Private WRITE sequence

Master	Slave (AK09919)	Bus Condition
START condition		Open-Drain
7-bit Dynamic Address		Open-Drain
R/W = "0"	ACK (with Handoff)	Open-Drain
Access Address (1 byte)	Parity Check, using T-Bit	Push-Pull
Control Data (1 byte)	Parity Check, using T-Bit	Push-Pull
Control Data (1 byte)	Parity Check, using T-Bit	Push-Pull
|	|	|
STOP condition		Push-Pull

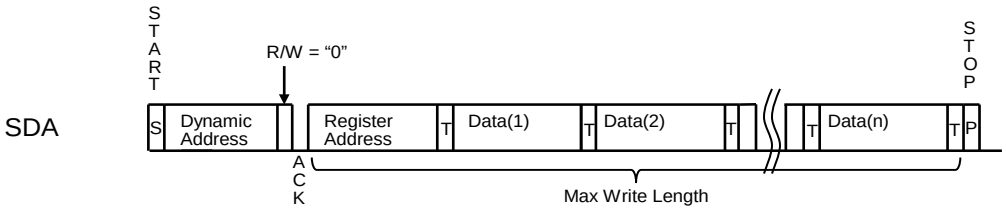


Figure 10.13. I3C Private WRITE

Max Write Length can be set by SETMWL CCC and read by GETMWL CCC.
The minimum value that Max Write Length can be set to is 8.
When a value smaller than 8 is set, AK09919 operations as Max Write Length = 8.
The maximum value that Max Write Length can be set to is 255.
When it over byte by setting SETMWL, AK09919 stops receiving data and ignore the next data.

10.1.3.1.2. READ Instruction

When the R/W bit is set to “1”, AK09919 performs read operation.
The read operation requires to execute WRITE instruction as dummy before a Slave Address for the READ instruction (R/W bit = “1”) is transmitted. In read operation, a START condition is first generated then a Dynamic Address for the WRITE instruction (R/W bit = “0”) and a read address are transmitted sequentially.
After AK09919 receives a T-Bit in response to this address transmission, a Repeated START condition and a Dynamic Address for the READ instruction (R/W bit = “1”) are generated again. AK09919 generates a T-Bit in response to this Dynamic Address transmission. Next, AK09919 transfers the data at the specified address then increments the internal address counter by one. If the Master generates a STOP condition instead of an acknowledge after data is transferred, the read operation stops.
The address is incremented from 00h to 10h, from 11h to 18h and from 30h to 32h. When the address is 00h to 10h, the address is incremented 00h → 01h → 02h → 03h → 10h. When the address is 11h to 18h, the address is incremented 11h → 12h → 13h → … → 18h, and the address goes back to 00h after 18h. In the case that FIFO function is enabled, the address is incremented 11h → 12h → 13h → … → 18h, and the address goes back to 11h after 18h. When the address is 30h to 32h, the address goes back to 30h after 32h.

Table 10.2. I3C Private READ sequence

Master	Slave (AK09919)	Bus Condition
START condition		Open-Drain
7-bit Dynamic Address		Open-Drain
R/W = “0”	ACK (with Handoff)	Open-Drain
Access Address (1 byte)	Parity Check, using T-Bit	Push-Pull
Repeated START condition		Push-Pull
7-bit Dynamic Address		Push-Pull
R/W = “1”	ACK (without Handoff)	Push-Pull
Data Read (1 byte)	T-Bit (with Handoff)	Push-Pull
Data Read (1 byte)	T-Bit (with Handoff)	Push-Pull
|	|	|
STOP condition		Push-Pull

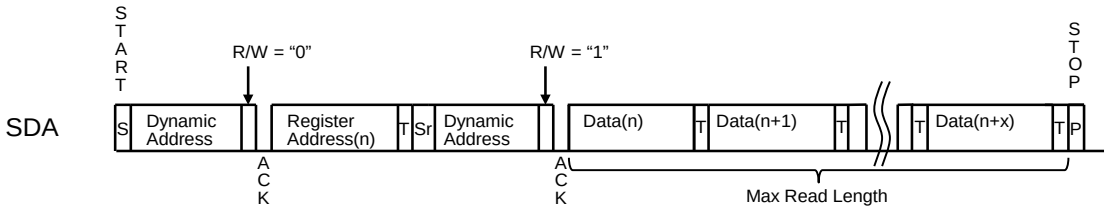


Figure 10.14. I3C Private READ

Max Read Length can be set by SETMRL CCC and read by GETMRL CCC.
The minimum value that Max Read Length can be set is 16.
When a value smaller than 16 is set, AK09919 operations as Max Read Length = 16.
The maximum value that Max Read Length can be set to is 255.

10.1.3.2. Common Command Code (CCC)

AK09919 has the Common Command Codes (CCCs) specified in the specification of I3C.
Common Command Codes (CCCs) are globally supported commands that can be transmitted either directly to a specific I3C Slave Device, or to all I3C Slave Devices simultaneously.

10.1.3.2.1. Broadcast CCC

A Broadcast Write CCC is seen by all I3C Slaves. All Slaves inspect every received Broadcast command, even if the Slave then ignores the Broadcast command.
Every Broadcast Write CCC Command ends with a Repeated START or a STOP, except ENTDAA which always ends with a STOP.

Table 10.3. I3C Broadcast CCC sequence

Master	Slave (AK09919)	Bus Condition
START condition		Open-Drain
Broadcast Address (7 bits)		Open-Drain
R/W = “0”	ACK (with Handoff)	Open-Drain
Broadcast CCC (1 byte)	Parity Check, using T-Bit	Push-Pull
Optional Data (1 byte)	Parity Check, using T-Bit	Push-Pull
Optional Data (1 byte)	Parity Check, using T-Bit	Push-Pull
|	|	|
STOP condition		Push-Pull

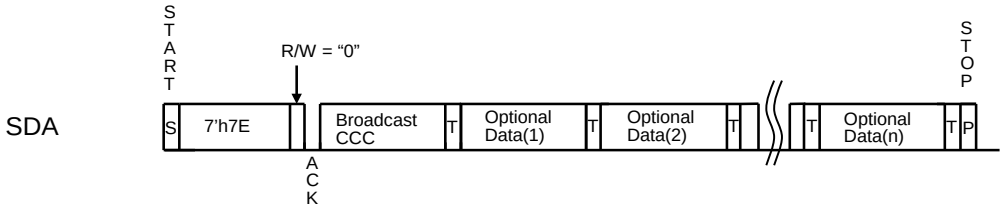


Figure 10.15. I3C Broadcast CCC

Table 10.4. CCC (Broadcast) Table

Command Code	Command Name	Broadcast/ Direct	Set/Get	Brief Description
00h	ENEC	Broadcast	Set	Enable Events Command, “1”: enable
01h	DISEC	Broadcast	Set	Disable Events Command, “1”: disable
02h	ENTAS0	Broadcast	Set	Enter Activity State 0
03h	ENTAS1	Broadcast	Set	Enter Activity State 1
04h	ENTAS2	Broadcast	Set	Enter Activity State 2
05h	ENTAS3	Broadcast	Set	Enter Activity State 3
06h	RSTDAA	Broadcast	Set	Reset Dynamic Address Assignment
07h	ENTDAA1	Broadcast	Get	PID[47:40]
	ENTDAA2	Broadcast	Get	PID[39:32]
	ENTDAA3	Broadcast	Get	PID[31:24]
	ENTDAA4	Broadcast	Get	PID[23:16]
	ENTDAA5	Broadcast	Get	PID[15:8]
	ENTDAA6	Broadcast	Get	PID[7:0]
	ENTDAA7	Broadcast	Get	BCR
	ENTDAA8	Broadcast	Get	DCR
	ENTDAA9	Broadcast	Set	Enter Dynamic Address
08h	DEFSLVS	Broadcast	-	Not supported
09h	SETMWL1	Broadcast	Set	Max_Write_Length[15:8]
	SETMWL2	Broadcast	Set	Max_Write_Length[7:0]
0Ah	SETMRL1	Broadcast	Set	Max_Read_Length[15:8]
	SETMRL2	Broadcast	Set	Max_Read_Length[7:0]
0Bh	ENTTM	Broadcast	-	Not supported
0Ch-1Fh	Reserved			
20h	ENTHDR0	Broadcast	-	Not supported
21h	ENTHDR1	Broadcast	-	
22h	ENTHDR2	Broadcast	-	
23h	ENTHDR3	Broadcast	-	
24h	ENTHDR4	Broadcast	-	
25h	ENTHDR5	Broadcast	-	
26h	ENTHDR6	Broadcast	-	
27h	ENTHDR7	Broadcast	-	
28h	SETXTIME1	Broadcast	-	
	SETXTIME2	Broadcast	-	
	SETXTIME3	Broadcast	-	
	SETXTIME4	Broadcast	-	
	SETXTIME5	Broadcast	-	
	SETXTIME6	Broadcast	-	
29h-7Fh	Reserved			

Table 10.5. CCC (Broadcast) Map

Command Code	Command Name	D7	D6	D5	D4	D3	D2	D1	D0	Initial value
00h	ENEC	-	-	-	-	-	-	-	IBI_EN	00h
01h	DISEC	-	-	-	-	-	-	-	IBI_DIS	00h
02h	ENTAS0	-	-	-	-	-	-	-	-	-
03h	ENTAS1	-	-	-	-	-	-	-	-	-
04h	ENTAS2	-	-	-	-	-	-	-	-	-
05h	ENTAS3	-	-	-	-	-	-	-	-	-
06h	RSTDAA	-	-	-	-	-	-	-	-	-
07h	ENTDAA1	0	0	0	0	0	0	1	1	03h
	ENTDAA2	1	0	1	1	1	0	1	0	BAh
	ENTDAA3	1	0	0	1	1	0	0	1	99h
	ENTDAA4	0	0	0	1	1	0	0	1	19h
	ENTDAA5	0	0	0	0	0	0	0	0	00h
	ENTDAA6	0	0	0	0	0	0	0	0	00h
	ENTDAA7	0	0	0	0	0	0	1	0	02h
	ENTDAA8	0	0	0	0	0	0	0	0	00h
	ENTDAA9	-	DA6	DA5	DA4	DA3	DA2	DA1	DA0	00h
08h	DEFSLVS	Not supported								-
09h	SETMWL1	0	0	0	0	0	0	0	0	00h
	SETMWL2	WL7	WL6	WL5	WL4	WL3	WL2	WL1	WL0	00h
0Ah	SETMRL1	0	0	0	0	0	0	0	0	00h
	SETMRL2	RL7	RL6	RL5	RL4	RL3	RL2	RL1	RL0	00h
0Bh	ENTTM	Not supported								-
0Ch-1Fh	Reserved									
20h	ENTHDR0	Not supported								-
21h	ENTHDR1									-
22h	ENTHDR2									-
23h	ENTHDR3									-
24h	ENTHDR4									-
25h	ENTHDR5									-
26h	ENTHDR6									-
27h	ENTHDR7									-
28h	SETXTIME1									-
	SETXTIME2									-
	SETXTIME3									-
	SETXTIME4									-
	SETXTIME5									-
	SETXTIME6									-
29h-7Fh	Reserved									

10.1.3.2.2. Directed CCC

A Direct CCC is directed to one or more specific I3C Slaves, selected by the Slave Dynamic Address. Every Direct CCC Command ends with a STOP or a Repeated START, followed by the I3C Broadcast Address (7'h7E).

Table 10.6. I3C Directed CCC sequence

Master	Slave (AK09919)	Bus Condition
START condition		Open-Drain
Broadcast Address (7 bits)		Open-Drain
R/W = "0"	ACK (with Handoff)	Open-Drain
Directed CCC (1 byte)	Parity Check, using T-Bit	Push-Pull
Repeated START condition		Push-Pull
7-bit Dynamic Address		Push-Pull
R/W	ACK (W: with Handoff) (R: without Handoff)	Push-Pull
Optional Data (1 byte)	Parity Check, using T-Bit	Push-Pull
|	|	
Repeated START condition		Push-Pull
7-bit Dynamic Address		Push-Pull
R/W	ACK (W: with Handoff) (R: without Handoff)	Push-Pull
Optional Data (1 byte)	Parity Check, using T-Bit	Push-Pull
|	|	
STOP condition or Repeated START + Broadcast Address + W		Push-Pull

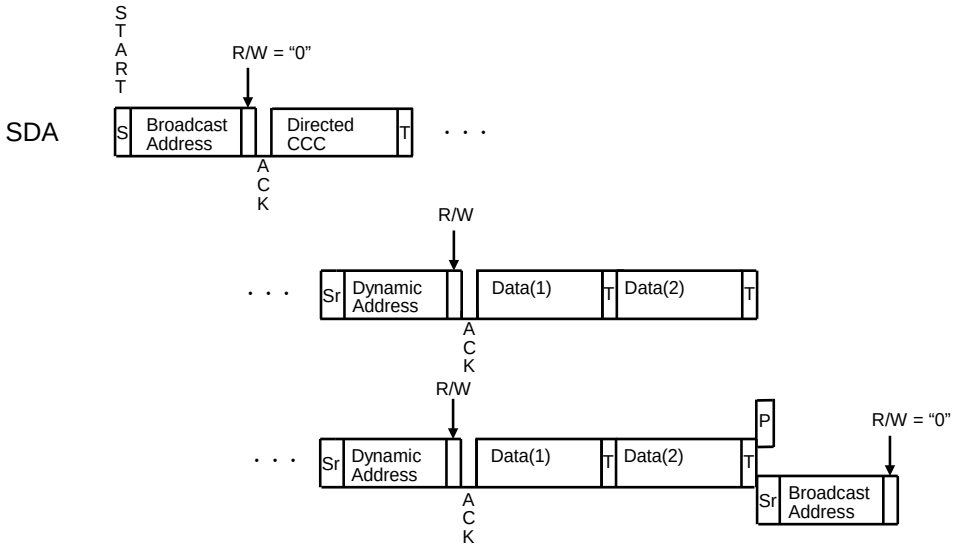


Figure 10.16. I3C Directed CCC

Table 10.7. CCC (Direct) Table

Command Code	Command Name	Broadcast/ Direct	Set/Get	Brief Description
80h	ENEC	Direct	Set	Enable Events Command, “1”: enable
81h	DISEC	Direct	Set	Disable Events Command, “1”: disable
82h	ENTAS0	Direct	Set	Enter Activity State 0
83h	ENTAS1	Direct	Set	Enter Activity State 1
84h	ENTAS2	Direct	Set	Enter Activity State 2
85h	ENTAS3	Direct	Set	Enter Activity State 3
86h	RSTDAA	Direct	Set	Reset Dynamic Address Assignment
87h	SETDASA	Direct	Set	Set Dynamic Address
88h	SETNEWDA	Direct	Set	Set New Dynamic Address
89h	SETMWL1	Direct	Set	Max_Write_Length[15:8]
	SETMWL2	Direct	Set	Max_Write_Length[7:0]
8Ah	SETMRL1	Direct	Set	Max_Read_Length[15:8]
	SETMRL2	Direct	Set	Max_Read_Length[7:0]
8Bh	GETMWL1	Direct	Get	Max_Write_Length[15:8]
	GETMWL2	Direct	Get	Max_Write_Length[7:0]
8Ch	GETMRL1	Direct	Get	Max_Read_Length[15:8]
	GETMRL2	Direct	Get	Max_Read_Length[7:0]
8Dh	GETPID1	Direct	Get	PID[47:40]
	GETPID2	Direct	Get	PID[39:32]
	GETPID3	Direct	Get	PID[31:24]
	GETPID4	Direct	Get	PID[23:16]
	GETPID5	Direct	Get	PID[15:8]
	GETPID6	Direct	Get	PID[7:0]
8Eh	GETBCR	Direct	Get	BCR
8Fh	GETDCR	Direct	Get	DCR
90h	GETSTATUS1	Direct	Get	STATUS[15:8]
	GETSTATUS2	Direct	Get	STATUS[7:0]
91h	GETACCMST	Direct	-	Not supported
92h	Reserved			
93h	SETBRGTGT	Direct	-	Not supported
94h	GETMXDS	Direct	-	Not supported
95h	GETHDRCAP	Direct	Get	HDR Capability
96h-97h	Reserved			
98h	SETXTIME	Direct	-	Not supported
99h	GETXTIME	Direct	-	Not supported
9Ah-FFh	Reserved			

Table 10.8. CCC (Direct) Map

Command Code	Command Name	D7	D6	D5	D4	D3	D2	D1	D0	Initial value
80h	ENEC	-	-	-	-	-	-	-	IBI_EN	00h
81h	DISEC	-	-	-	-	-	-	-	IBI_DIS	00h
82h	ENTAS0	-	-	-	-	-	-	-	-	-
83h	ENTAS1	-	-	-	-	-	-	-	-	-
84h	ENTAS2	-	-	-	-	-	-	-	-	-
85h	ENTAS3	-	-	-	-	-	-	-	-	-
86h	RSTDAA	-	-	-	-	-	-	-	-	-
87h	SETDASA	DA6	DA5	DA4	DA3	DA2	DA1	DA0	0	00h
88h	SETNEWDA	DA6	DA5	DA4	DA3	DA2	DA1	DA0	0	00h
89h	SETMWL1	0	0	0	0	0	0	0	0	00h
	SETMWL2	WL7	WL6	WL5	WL4	WL3	WL2	WL1	WL0	00h
8Ah	SETMRL1	0	0	0	0	0	0	0	0	00h
	SETMRL2	RL7	RL6	RL5	RL4	RL3	RL2	RL1	RL0	00h
8Bh	GETMWL1	0	0	0	0	0	0	0	0	00h
	GETMWL2	WL7	WL6	WL5	WL4	WL3	WL2	WL1	WL0	08h
8Ch	GETMRL1	0	0	0	0	0	0	0	0	00h
	GETMRL2	RL7	RL6	RL5	RL4	RL3	RL2	RL1	RL0	10h
8Dh	GETPID1	0	0	0	0	0	0	1	1	03h
	GETPID2	1	0	1	1	1	0	1	0	BAh
	GETPID3	1	0	0	1	1	0	0	1	99h
	GETPID4	0	0	0	1	1	0	0	1	19h
	GETPID5	0	0	0	0	0	0	0	0	00h
	GETPID6	0	0	0	0	0	0	0	0	00h
8Eh	GETBCR	0	0	0	0	0	0	1	0	02h
8Fh	GETDCR	0	0	0	0	0	0	0	0	00h
90h	GETSTATUS1	0	0	0	0	0	0	0	0	00h
	GETSTATUS2	AM1	AM0	WE	0	PI3	PI2	PI1	PI0	00h
91h	GETACCMST	Not supported								
92h	Reserved									
93h	SETBRGTGT	Not supported								
94h	GETMXDS	Not supported								
95h	GETHDRCAP	0	0	0	0	0	0	0	0	00h
96h-97h	Reserved									
98h	SETXTIME	Not supported								
99h	GETXTIME	Not supported								
9Ah-FFh	Reserved									

10.1.4. HDR Exit Pattern

The HDR Exit Pattern is defined thus:

- SDA starts High, SCL starts Low
- SDA falls (from High to Low) 4 times, while SCL remains Low (for the whole time)
- Each SDA transition is separated by a time interval of at least tHIGH
- At the end of the HDR Exit Pattern, first SCL rises and then SDA rises. This is a normal I3C STOP.

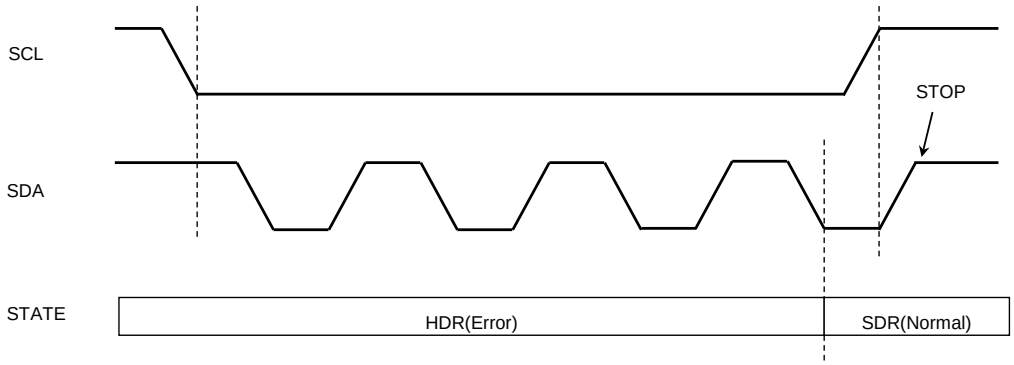


Figure 10.17. HDR-EXIT pattern

10.1.5. Error Detection and Recovery Method

There are multiple error modes in the interface of AK09919. Table 10.9. shows the error detections and recovery methods.

Table 10.9. Error Detection and Recovery Methods

Error Type	Description	Error Detection Method	Error Recovery Method
S0	Broadcast Address/W (= 7'h7E/W) or Dynamic Address/RW (*)Other than in ENTDAA	Detect any of the following: 7'h3E / W 7'h5E / W 7'h6E / W 7'h76 / W 7'h7A / W 7'h7C / W 7'h7F / W 7'h7E / R(*)	Enable HDR EXIT Detector and ignore all other patterns
S1	CCC Code	Parity Check, using T-Bit	Enable HDR EXIT detector and neglect other patterns
S2	Write Data	Parity Check, using T-Bit	Enable STOP or Repeated START detector and neglect other patterns
S3	Assigned Address during Dynamic Address Arbitration	Parity Check, using PAR Bit	Generate NACK (after PAR), then wait for another Repeated START and 7'h7E/R to re-transmit the Provisional ID
S4	7'h7E/R after Sr during Dynamic Address Arbitration	Detect any value other than 7'h7E/R after Sr during Dynamic Address Arbitration	Generate NACK (after 7'h7E/R), then enable STOP or Repeated START Detector and ignore all other patterns
S5	Transaction after detecting CCC	Detect illegally formatted CCC	Generate NACK (after Slave Address), then enable STOP or Repeated START Detector and ignore all other patterns
S6	Monitoring Error	AK09919 detects (through monitoring) that transmitted Data differs from what it intended to transmit (Does not apply during Dynamic Address Arbitration)	Stop the transmission, then enable STOP or Repeated START Detector and ignore all other patterns

11. Registers

11.1. Description of Registers

AK09919 has registers of 18 addresses as indicated in Table 11.1.. Every address consists of 8 bits data. Data is transferred to or received from the external CPU via the serial interface described previously.

Table 11.1. Register Table

Name	Address	READ/ WRITE	Description	Bit width	Remarks
WIA1	00h	READ	Company ID	8	
WIA2	01h	READ	Device ID	8	
RSV1	02h	READ	Reserved 1	8	
RSV2	03h	READ	Reserved 2	8	
ST1	10h	READ	Status 1	8	Data status
HXH	11h	READ	Measurement Magnetic Data	8	X-axis data
HXL	12h	READ		8	
HYH	13h	READ		8	Y-axis data
HYL	14h	READ		8	
HZH	15h	READ		8	Z-axis data
HZL	16h	READ		8	
TMPS	17h	READ	Dummy	8	Dummy
ST2	18h	READ	Status 2	8	Data status
CNTL1	30h	READ/WRITE	Control 1	8	Control settings
CNTL2	31h	READ/WRITE	Control 2	8	Control settings
CNTL3	32h	READ/WRITE	Control 3	8	Control settings
TS1	33h	READ/WRITE	Test	8	DO NOT ACCESS
TS2	34h	READ/WRITE	Test	8	DO NOT ACCESS

The address is incremented from 00h to 10h, from 11h to 18h and from 30h to 32h. When the address is 00h to 10h, the address is incremented 00h → 01h → 02h → 03h → 10h. When the address is 11h to 18h, the address is incremented 11h → 12h → 13h → … → 18h, and the address goes back to 00h after 18h. In the case that FIFO function is enabled, the address is incremented 11h → 12h → 13h → … → 18h, and the address goes back to 11h after 18h. When the address is 30h to 32h, the address goes back to 30h after 32h.

11.2. Register Map

Table 11.2. Register Map

Addr.	Register name	D7	D6	D5	D4	D3	D2	D1	D0
Read-only register									
00h	WIA1	0	1	0	0	1	0	0	0
01h	WIA2	0	0	0	0	1	1	1	0
02h	RSV1	RSV17	RSV16	RSV15	RSV14	RSV13	RSV12	RSV11	RSV10
03h	RSV2	RSV27	RSV26	RSV25	RSV24	RSV23	RSV22	RSV21	RSV20
10h	ST1	0	FNUM4	FNUM3	FNUM2	FNUM1	FNUM0	DOR	DRDY
11h	HXH	HX15	HX14	HX13	HX12	HX11	HX10	HX9	HX8
12h	HXL	HX7	HX6	HX5	HX4	HX3	HX2	HX1	HX0
13h	HYH	HY15	HY14	HY13	HY12	HY11	HY10	HY9	HY8
14h	HYL	HY7	HY6	HY5	HY4	HY3	HY2	HY1	HY0
15h	HZH	HZ15	HZ14	HZ13	HZ12	HZ11	HZ10	HZ9	HZ8
16h	HZL	HZ7	HZ6	HZ5	HZ4	HZ3	HZ2	HZ1	HZ0
17h	TMPS	0	0	0	0	0	0	0	0
18h	ST2	0	RSV30	RSV29	RSV28	HOFL	INV	0	0
Read/Write register									
30h	CNTL1	RSV31	ITS1	ITS0	0	WM3	WM2	WM1	WM0
31h	CNTL2	FIFO	SDR	IBIP	MODE4	MODE3	MODE2	MODE1	MODE0
32h	CNTL3	0	0	0	0	0	0	0	SRST
33h	TS1	-	-	-	-	-	-	-	-
34h	TS2	-	-	-	-	-	-	-	-

When VDD is turned ON, POR function works and all registers of AK09919 are initialized.
TS1 and TS2 are test registers for shipment test. Do not access these registers.

11.3. Detailed Description of Registers

11.3.1. WIA: Who I Am

Addr.	Register name	D7	D6	D5	D4	D3	D2	D1	D0
Read-only register									
00h	WIA1	0	1	0	0	1	0	0	0
01h	WIA2	0	0	0	0	1	1	1	0

WIA1[7:0] bits: Company ID of AKM. It is described in one byte and fixed value.
48h: fixed
WIA2[7:0] bits: Device ID of AK09919. It is described in one byte and fixed value.
0Eh: fixed

11.3.2. RSV: Reserved

Addr.	Register name	D7	D6	D5	D4	D3	D2	D1	D0
Read-only register									
02h	RSV1	RSV17	RSV16	RSV15	RSV14	RSV13	RSV12	RSV11	RSV10
03h	RSV2	RSV27	RSV26	RSV25	RSV24	RSV23	RSV22	RSV21	RSV20

RSV1[7:0] bits / RSV2[7:0] bits: Reserved register used internal of AKM.

11.3.3. ST1: Status 1

Addr.	Register name	D7	D6	D5	D4	D3	D2	D1	D0
Read-only register									
10h	ST1	0	FNUM4	FNUM3	FNUM2	FNUM1	FNUM0	DOR	DRDY
Reset		0	0	0	0	0	0	0	0

DRDY bit: Data Ready
"0": Normal
"1": Data is ready

When FIFO is disabled (FIFO bit = "0");
DRDY bit turns to "1" when data is ready in Single measurement mode, Continuous measurement mode 1, 2, 3, 4, 5 or Self-test mode. It returns to "0" when any one of ST2 register or measurement data register (HXH to TMPS) is read.

When FIFO is enabled (FIFO bit = "1");
If the number of stored data set is equal to or more than the number set to WM[3:0] bits, DRDY bit turns to "1". If the number of stored data set is less than the number set to WM[3:0] bits, DRDY bit turns to "0".

DOR bit: Data Overrun
"0": Normal
"1": Data overrun

When FIFO is disabled (FIFO bit = "0");
DOR bit turns to "1" when data has been skipped in Continuous measurement mode 1, 2, 3, 4 or 5. It returns to "0" when any one of ST2 register or measurement data register (HXH to TMPS) is read.

When FIFO is enabled (FIFO bit = "1");
If a set of new data is measured when the buffer is full, DOR bit turns to "1". If at least one data set is read from the buffer, DOR bit turns to "0".

FNUM[4:0] bits: FIFO status
FNUM[4:0] bits correspond to how many data sets are currently in the FIFO buffer.

11.3.4. HXH to HZL: Measurement Magnetic Data

Addr.	Register name	D7	D6	D5	D4	D3	D2	D1	D0
Read-only register									
11h	HXH	HX15	HX14	HX13	HX12	HX11	HX10	HX9	HX8
12h	HXL	HX7	HX6	HX5	HX4	HX3	HX2	HX1	HX0
13h	HYH	HY15	HY14	HY13	HY12	HY11	HY10	HY9	HY8
14h	HYL	HY7	HY6	HY5	HY4	HY3	HY2	HY1	HY0
15h	HZH	HZ15	HZ14	HZ13	HZ12	HZ11	HZ10	HZ9	HZ8
16h	HZL	HZ7	HZ6	HZ5	HZ4	HZ3	HZ2	HZ1	HZ0
Reset		0	0	0	0	0	0	0	0

Measurement data of magnetic sensor X-axis/Y-axis/Z-axis
HXH[15:8]: X-axis measurement data higher 8-bit
HXL[7:0]: X-axis measurement data lower 8-bit
HYH[15:8]: Y-axis measurement data higher 8-bit
HYL[7:0]: Y-axis measurement data lower 8-bit
HZH[15:8]: Z-axis measurement data higher 8-bit
HZL[7:0]: Z-axis measurement data lower 8-bit

Measurement data is stored in two's complement. Measurement range of each axis is -32752 to 32752 in 16-bit output.

Table 11.3. Measurement magnetic data format

Measurement data (each axis) [15:0]			Magnetic flux density [μT]
Two's complement	Hex	Decimal	
0111 1111 1111 0000	7FF0	32752	4912(max.)
|	|	|	|
0000 0000 0000 0001	0001	1	0.15
0000 0000 0000 0000	0000	0	0
1111 1111 1111 1111	FFFF	-1	-0.15
|	|	|	|
1000 0000 0001 0000	8010	-32752	-4912(min.)

When FIFO is enabled (FIFO bit = "1");
By accessing HXH register, the oldest data set is passed to the read register from the buffer. Reading ST2 register is regarded as the finish of reading out one set of data. Then the read data set is deleted, and the next oldest data set will be ready to be read. If ST2 register or HXH register is not read, the same set of data is kept in the read register. When reading out data, always start with HXH register and finish with ST2 register.

11.3.5. TMPS: Temperature Data

Addr.	Register name	D7	D6	D5	D4	D3	D2	D1	D0
Read-only register									
17h	TMPS	TMPS7	TMPS6	TMPS5	TMPS4	TMPS3	TMPS2	TMPS1	TMPS0
Reset		0	0	0	0	0	0	0	0

TMPS[7:0] bits: Dummy register

11.3.6. ST2: Status 2

Addr.	Register name	D7	D6	D5	D4	D3	D2	D1	D0
Read-only register									
18h	ST2	0	RSV30	RSV29	RSV28	HOFL	INV	0	0
Reset		0	0	0	0	0	1	0	0

ST2[6:4] bits: Reserved register for AKM.

HOFL bit: Magnetic sensor overflow
"0": Normal
"1": Magnetic sensor overflow occurred

In Single measurement mode, Continuous measurement modes (1 to 5) and Self-test mode, magnetic sensor may overflow even though measurement data register is not saturated. In this case, measurement data is not correct and HOFL bit turns to "1". When measurement data register (HXH to HZL) is updated, HOFL bit is updated. Refer to 9.4.3.6. for detailed information.

INV bit: Invalid data
"0": Normal
"1": Data is invalid
INV bit functions only when FIFO is enabled (FIFO bit = "1"). If data is read out when there is no data set in the buffer, INV bit is turned to "1" and measurement data registers (HXH to HZL) are forced to fixed value 7FFFh. If a set of new data is measured, INV bit turns to "0".

When FIFO is disabled (FIFO bit = "0");
ST2 register has a role as data reading end register, also. When any of measurement data register (HXH to TMPS) is read in Continuous measurement modes (1 to 5), it means data reading start and taken as data reading until ST2 register is read. Therefore, when any of measurement data is read, be sure to read ST2 register at the end. There is no data set in the buffer, INV bit is always "1".

When FIFO is enabled (FIFO bit = "1");
ST2 register is a part of one set of data stored in the buffer. If any of data register (HXH to TMPS) is read, be sure to read ST2 register at the end. If read data set includes magnetic sensor over flow, HOFL bit is "1". If there is no data set in the buffer, INV bit is "1".

11.3.7. CNTL1: Control 1

Addr.	Register name	D7	D6	D5	D4	D3	D2	D1	D0
Read/Write register									
30h	CNTL1	RSV31	ITS1	ITS0	0	WM3	WM2	WM1	WM0
Reset		0	0	0	0	0	0	0	0

CNTL1[7] bit: Reserved register for AKM.

ITS[1:0] bits: Noise suppression level setting
"00": Off
"01": Low
"10": High
"11": High

ITS[1:0] bits setting is valid when SDR bit = "1". Refer to 9.5. for detailed information.

WM[3:0] bits: Watermark level setting
"0000": 1 step
"0001": 2 steps
"0010": 3 steps
|
"1111": 16 steps (upper limit)

Watermark level can be set every 1 step. The upper limit of watermark level is 16 steps (WM[3:0] bits = "1111"). It is prohibited to change WM[3:0] bits in any other modes than Power-down mode.

11.3.8. CNTL2: Control 2

Addr.	Register name	D7	D6	D5	D4	D3	D2	D1	D0
Read/Write register									
31h	CNTL2	FIFO	SDR	IBIP	MODE4	MODE3	MODE2	MODE1	MODE0
Reset		0	0	0	0	0	0	0	0

MODE[4:0] bits: Operation mode setting
"00000": Power-down mode
"00001": Single measurement mode
"00010": Continuous measurement mode 1
"00100": Continuous measurement mode 2
"00110": Continuous measurement mode 3
"01000": Continuous measurement mode 4
"01110": Continuous measurement mode 5
"10000": Self-test mode

When each mode is set, AK09919 transits to the set mode. Refer to 9.3. for detailed information. If other value is set, AK09919 transits to Power-down mode automatically.

SDR bit: Low noise drive setting
"0": disable
"1": enable

Low noise drive is available only in Continuous measurement modes. It is prohibited to enable it other than Continuous measurement modes. Refer to 9.5. for detailed information.

FIFO bit: FIFO setting
"0": disable
"1": enable

By writing "1" to FIFO bit, FIFO function is enabled. By writing "0", FIFO function is disabled, and the buffer is cleared at the same time. FIFO function is available only in Continuous measurement modes. It is prohibited to enable it other than Continuous measurement modes.

IBIP bit: IBI Payload setting
"0": disable
"1": enable

IBIP bit functions only when FIFO is disabled (FIFO bit = "0"). When FIFO is enabled (FIFO bit = "1"), read data by normal read access. Refer to 9.7.1. for detailed information.

11.3.9. CNTL3: Control 3

Addr.	Register name	D7	D6	D5	D4	D3	D2	D1	D0
Read/Write register									
32h	CNTL3	0	0	0	0	0	0	0	SRST
Reset		0	0	0	0	0	0	0	0

SRST bit: Soft reset
"0": Normal
"1": Reset
When "1" is set, all registers are initialized. After reset, SRST bit turns to "0" automatically.

11.3.10. TS1, TS2: Test

Addr.	Register name	D7	D6	D5	D4	D3	D2	D1	D0
Read/Write register									
33h	TS1	-	-	-	-	-	-	-	-
34h	TS2	-	-	-	-	-	-	-	-
Reset		0	0	0	0	0	0	0	0

TS1 and TS2 registers are AKM internal test register. Do not access these registers.

12. Recommended External Circuits

12.1. I²C Bus Interface

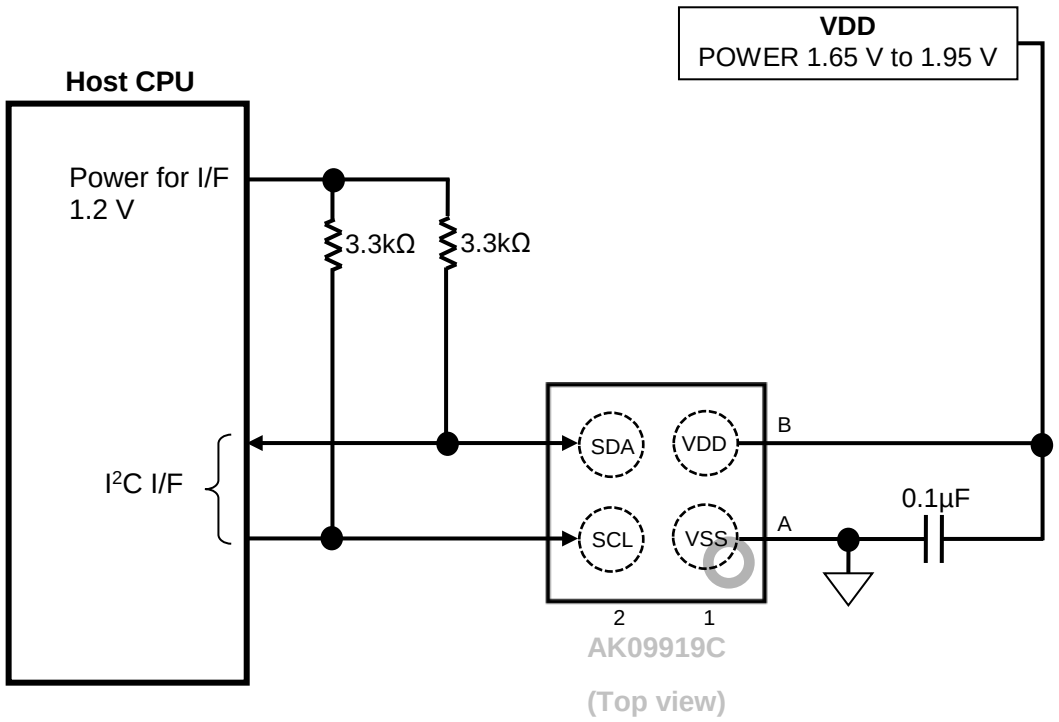


Figure 12.1. When power for I/F is 1.2V

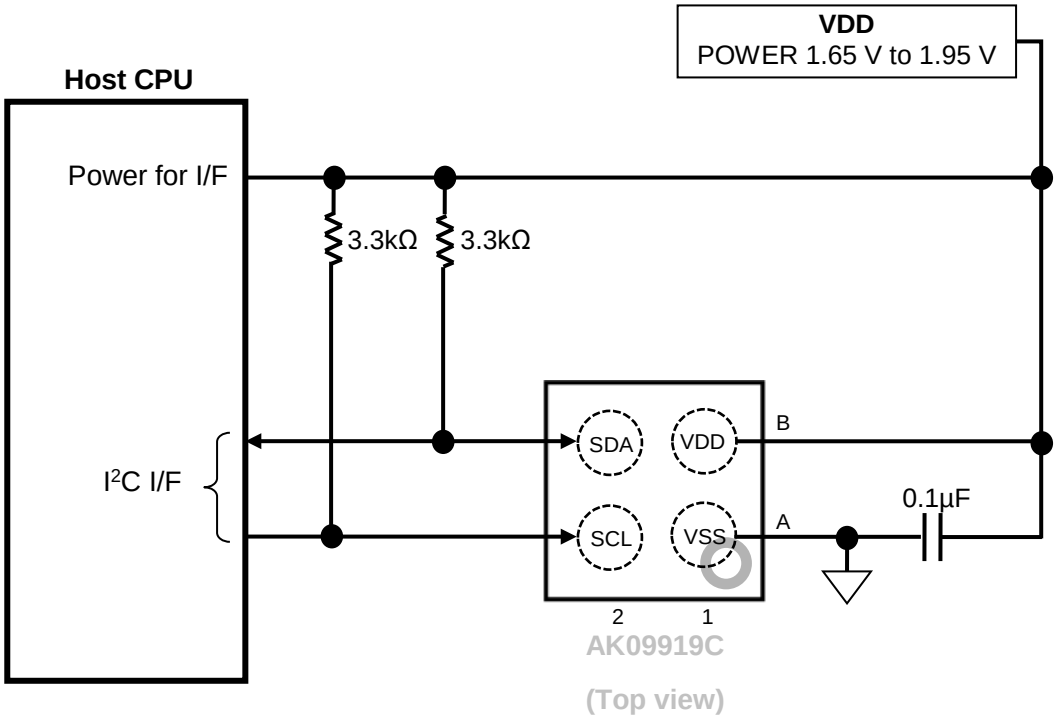


Figure 12.2. When power for I/F is the same as VDD

12.2. I3C Bus Interface

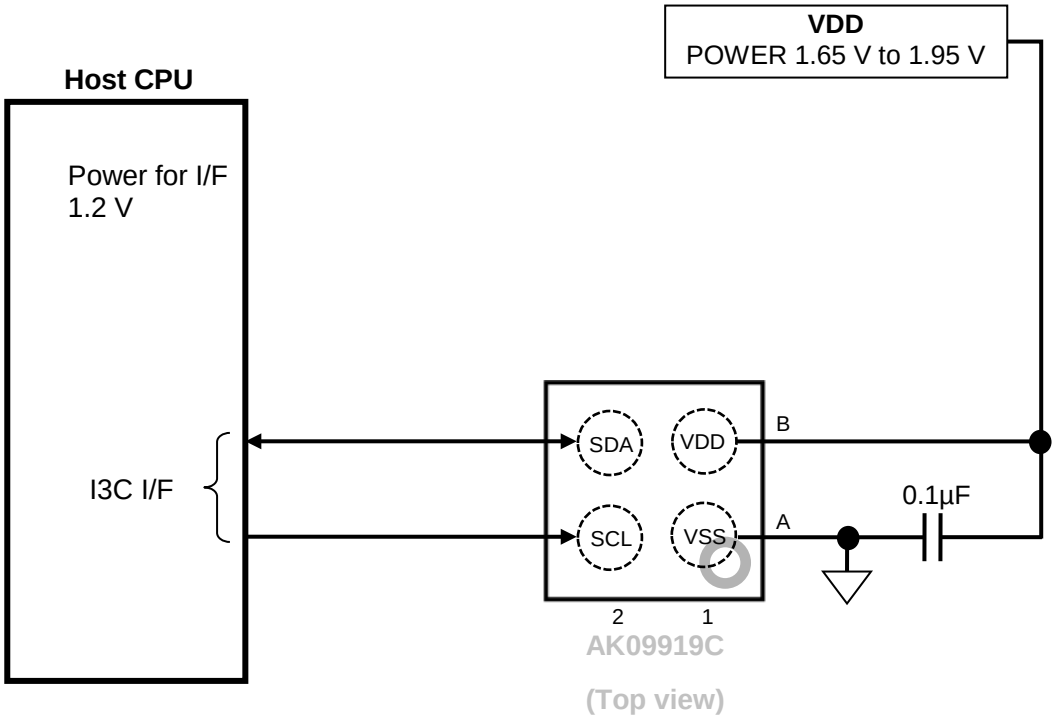


Figure 12.3. When power for I/F is 1.2V

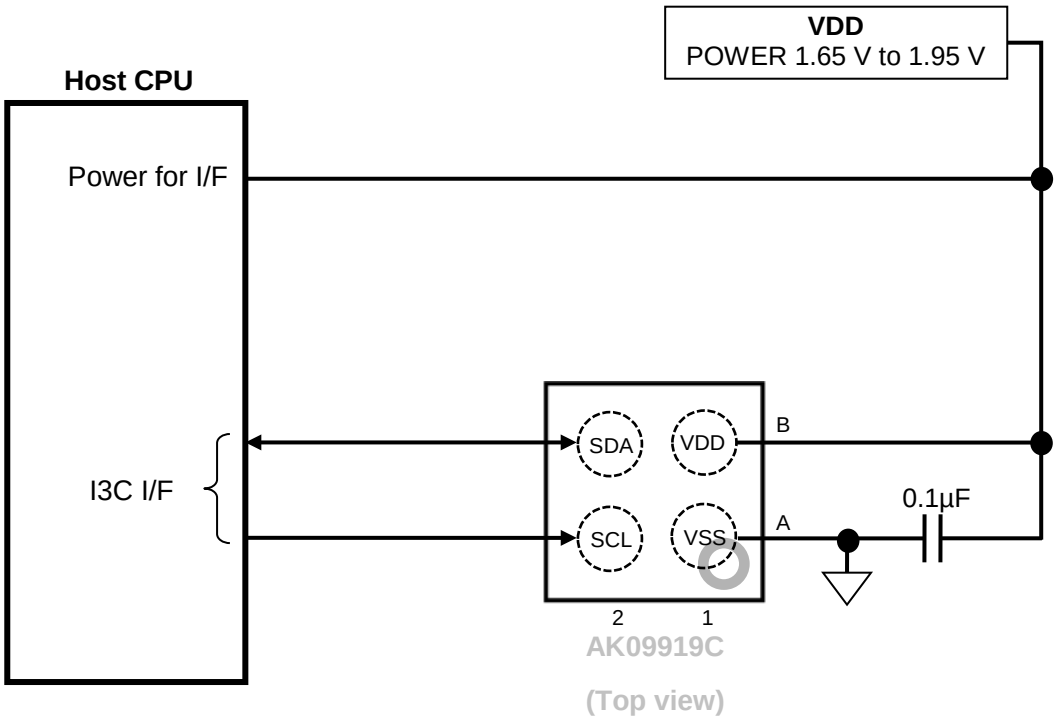


Figure 12.4. When power for I/F is the same as VDD

13. Package

13.1. Marking

Date code: $X_1X_2X_3X_4X_5$

- X1 = ID
- X2 = Year code
- X3 = Month code
- X4X5 = Lot

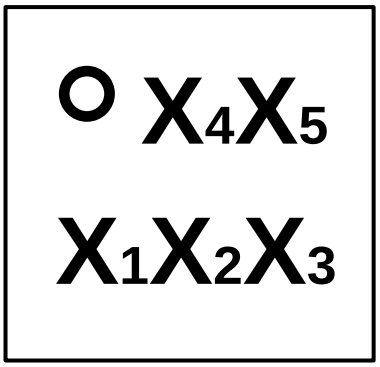
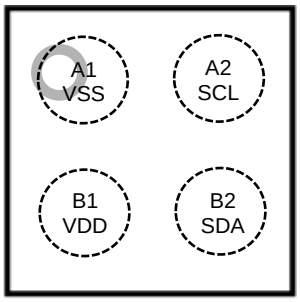


Figure 13.1. Marking format

13.2. Pin Assignment



	1	2
A	VSS	SCL
B	VDD	SDA

<Top view>

Figure 13.2. Pin assignment

13.3. Outline Dimensions

[mm]

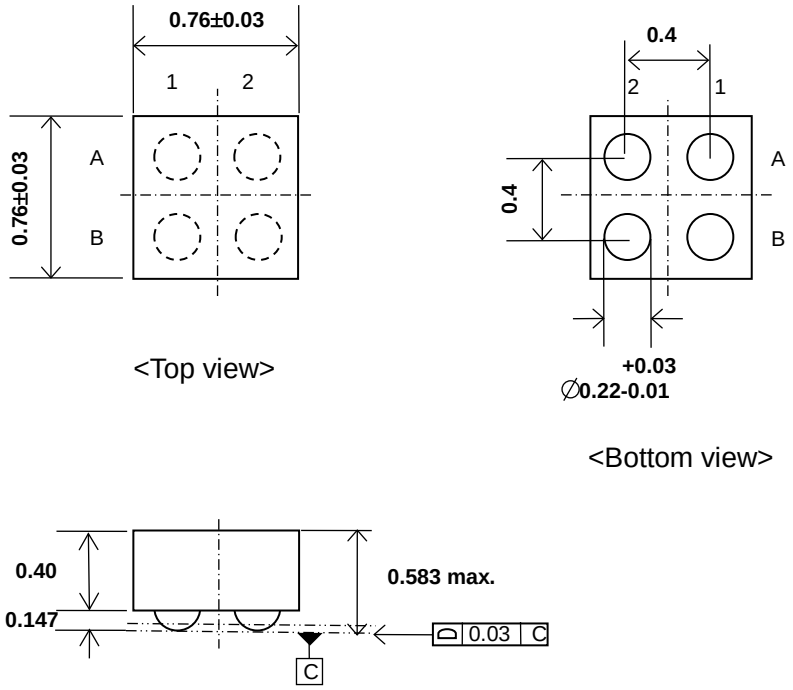


Figure 13.3. Package outline dimensions

13.4. Recommended Foot Print Pattern

[mm]

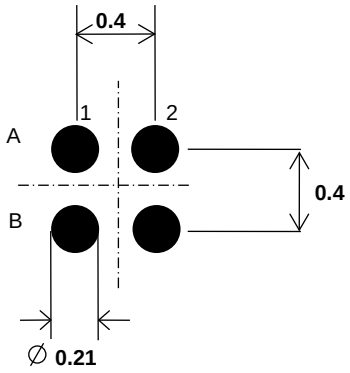


Figure 13.4. Foot print pattern dimensions

14. Relationship between the Magnetic Field and Output Code

The measurement data increases as the magnetic flux density increases in the arrow directions.

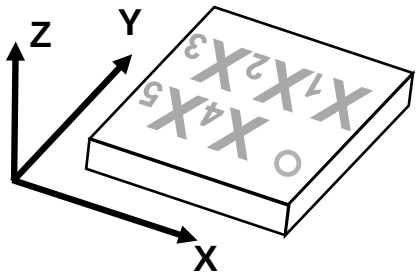


Figure 14.1. Direction of magnetic field detection

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