1. DESCRIPTION

The XD/XL1881 Video sync separator extracts timing information including composite and vertical sync, burst or back porch timing, and odd and even field information from standard negative going sync NTSC,PAL (1) and SECAM video signals with amplitude from 0.5-V to 2-V p-p. The integrated circuit is also capable of providing sync separation for non-standard, faster horizontal rate video signals. The vertical output is produced on the rising edge of the first serration in the vertical sync period. A default vertical output is produced after a time delay if the rising edge mentioned above does not occur within the externally set delay period, such as might be the case for a non-standard video signal.

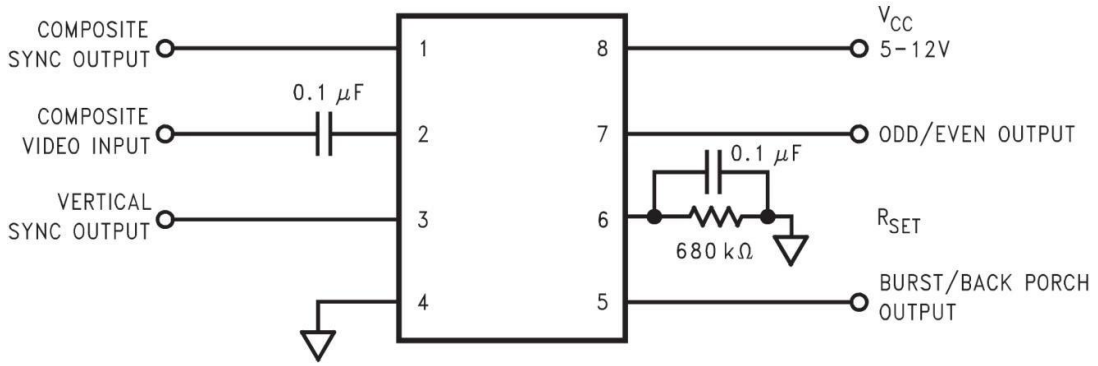
2. FEATURES

- AC Coupled Composite Input Signal
- >10-kΩ Input Resistance
- <10-mA Power Supply Drain Current
- Composite Sync and Vertical Outputs
- Odd and Even Field Output
- Burst Gate or Back Porch Output
- Horizontal Scan Rates to 150 kHz
- Edge Triggered Vertical Output
- Default Triggered Vertical Output for Non-
- Standard Video Signal (Video Games-Home Computers)

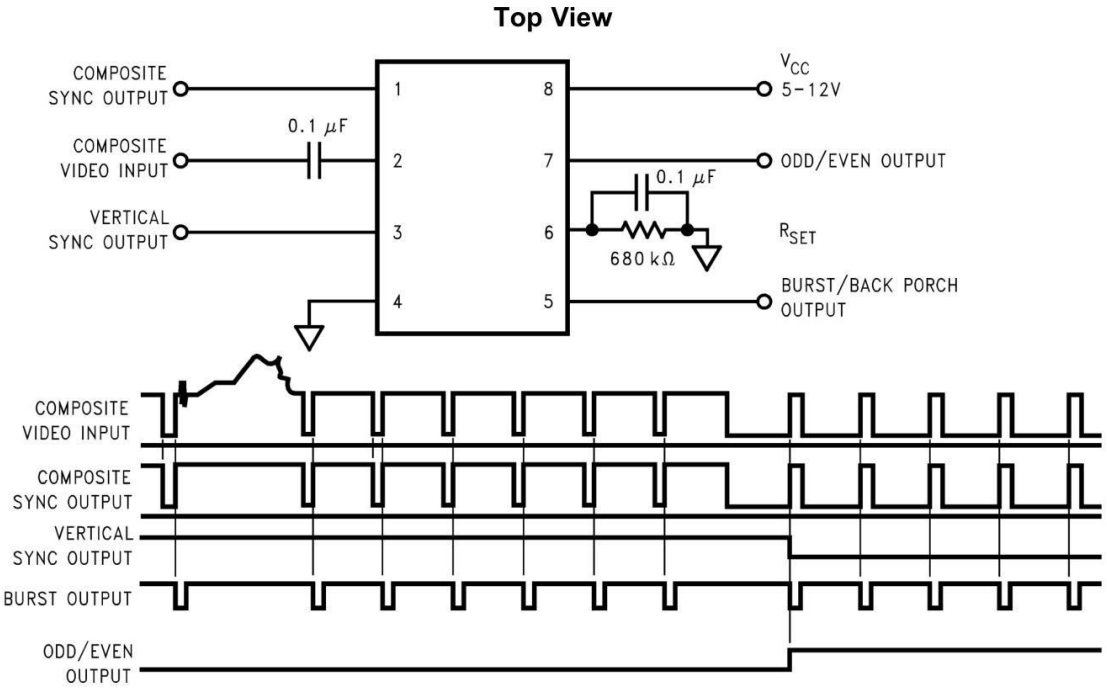
3. APPLICATIONS

- Video Cameras and Recorders
- Broadcasting Systems
- Set-Top Boxes
- Home Entertainment
- Computing and Gaming Applications

4. TYPICAL CONNECTION DIAGRAM



5. PIN CONFIGURATION AND FUNCTIONS



PIN		TYPE	DESCRIPTION
NO.	NAME		
1	CSOUT	Output	Composite Sync Output
2	CVIN	Input	Composite Video Input
3	VSOUT	Output	Vertical Sync Output
4	GND	—	Ground
5	BPOUT	Output	Burst or Back Porch Timing Output
6	RSET	Input	Charge Current External Resistor
7	OEOUT	Output	Odd and Even Field Output
8	VCC	Input	Supply Voltage

6. SPECIFICATIONS

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

			MIN	MAX	UNIT
Supply Voltage				13.2	V
Input Voltage			3 V_{P-P} (V_{CC} = 5)	6 V_{P-P} (V_{CC} ≥ 8)	V
Output Sink Currents; Pins, 1, 3, 5				5	mA
Output Sink Current; Pin 7				2	mA
Soldering Information	PDIP Package (10 sec.)			260	°C
	SOIC Package	Vapor Phase (60 sec.)		215	
		Infrared (15 sec.)		220	
Storage temperature, T_{stg}			−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Machine Model	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommend Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
T_A	Operating free-air temperature	0	70	°C

6.4 Electrical Characteristics XD/XL1881

V_{CC} = 5 V; R_{SET} = 680 kΩ; T_A = 0°C to +70°C by correlation with 100% electrical testing at T_A=25°C

PARAMETER	TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
Supply Current	Outputs at Logic 1	V_{CC} = 5 V		5.2	10	mA
		V_{CC} = 12 V		5.5	12	
DC Input Voltage	Pin 2		1.3	1.5	1.8	V
Input Threshold Voltage	See (2)		55	70	85	mV
Input Discharge Current	Pin 2; V_{IN} = 2 V		6	11	16	µA
Input Clamp Charge Current	Pin 2; V_{IN} = 1 V		0.2	0.8		mA
R_{SET} Pin Reference Voltage	Pin 6;(3)		1.1	1.22	1.35	V
Composite Sync. & Vertical Outputs	I_{OUT} = 40 µA; Logic 1	V_{CC} = 5 V	4.0	4.5		V
		V_{CC} = 12 V	11			
	I_{OUT} = 1.6 mA Logic 1	V_{CC} = 5 V	2.4	3.6		V
		V_{CC} = 12 V	10			
Burst Gate and Odd and Even Outputs	I_{OUT} = 40 µA; Logic 1	V_{CC} = 5 V	4	4.5		V
		V_{CC} = 12 V	11			
Composite Sync. Output	I_{OUT} = −1.6 mA; Logic 0; Pin 1			0.2	0.8	V
Vertical Sync. Output	I_{OUT} = −1.6 mA; Logic 0; Pin 3			0.2	0.8	V
Burst Gate Output	I_{OUT} = −1.6 mA; Logic 0; Pin 5			0.2	0.8	V
Odd and Even Output	I_{OUT} = −1.6 mA; Logic 0; Pin 7			0.2	0.8	V
Vertical Sync Width			190	230	300	µs
Burst Gate Width	2.7 kΩ from Pin 5 to V_{CC}		2.5	4	4.7	µs

Vertical Default Time	See (4)	32	65	90	μs

(1) Typicals are at T_J = 25°C and represent the most likely parametric norm.
(2) Relative difference between the input clamp voltage and the minimum input voltage which produces a horizontal output pulse.
(3) Careful attention should be made to prevent parasitic capacitance coupling from any output pin (Pins 1, 3, 5 and 7) to the R_{SET} pin (Pin 6).
(4) Delay time between the start of vertical sync (at input) and the vertical output pulse.

6.5 Dissipation Ratings

	MIN	MAX	UNIT
Package Dissipation(1)		1100	mW

(1) For operation in ambient temperatures above 25°C, the device must be derated based on a 150°C maximum junction temperature and a package thermal resistance of 110°C/W, junction to ambient.

6.6 Typical Characteristics

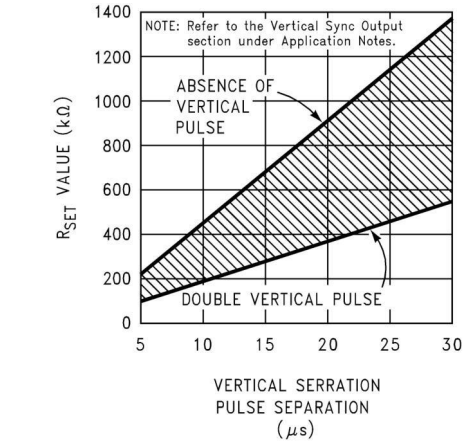


Figure 1. R_{SET} Value Selection vs Vertical Serration Pulse Separation

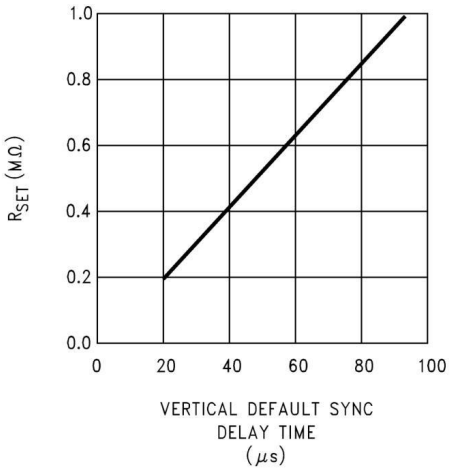


Figure 2. Vertical Default Sync Delay Time vs R_{SET}

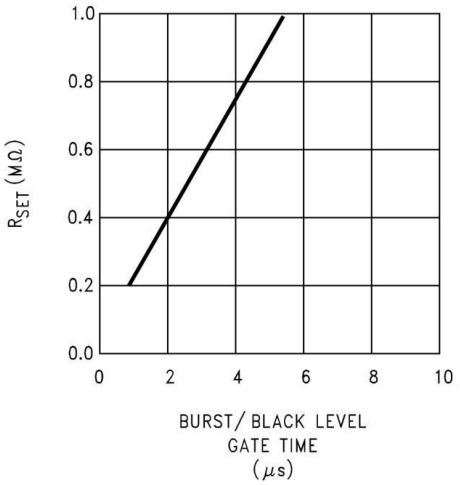


Figure 3. Burst or Black Level Gate Time vs R_{SET}

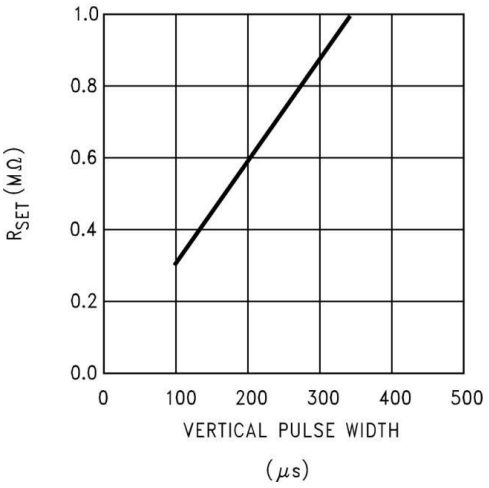


Figure 4. Vertical Pulse Width vs R_{SET}

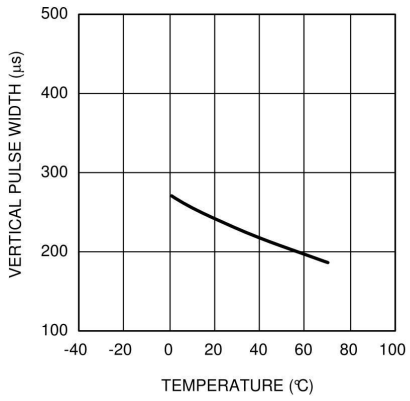


Figure 5. Vertical Pulse Width vs Temperature

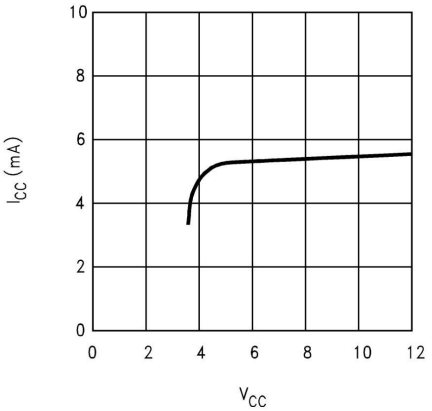


Figure 6. Supply Current vs Supply Voltage

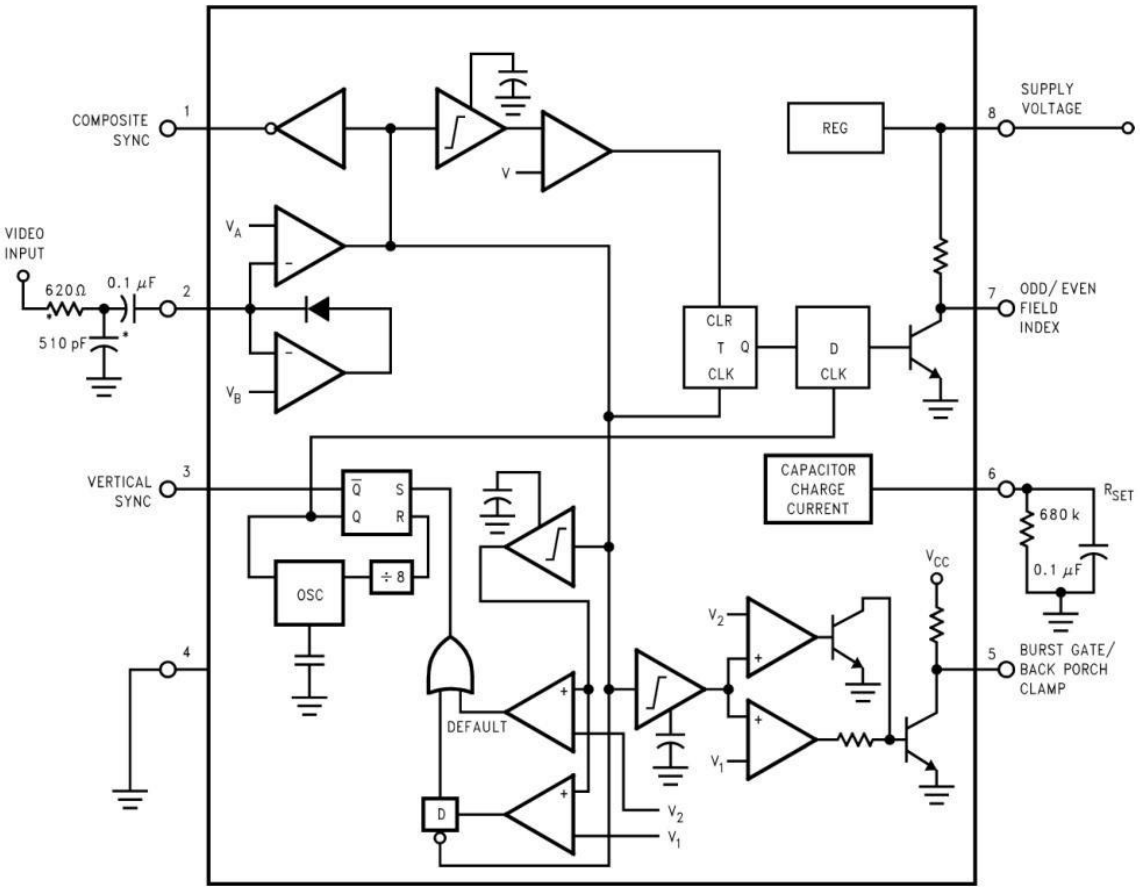
7. DETAILED DESCRIPTION

7.1 Overview

The XD/XL1881 is designed to strip the synchronization signals from composite video sources that are in, or similar to, the N.T.S.C. format. Input signals with positive polarity video (increasing signal voltage signifies increasing scene brightness) from 0.5 V (p-p) to 2 V (p-p) can be accommodated. The XD/XL1881 operates from a single supply voltage between 5-V DC and 12-V DC. The only required external components besides a power supply decoupling capacitor at pin 8 and a set current decoupling capacitor at pin 6, are the composite input coupling capacitor at pin 2 and one resistor at pin 6 that sets internal current levels. The resistor on pin 6 (that is, Rset) allows the XD/XL1881 to be adjusted for source signals with line scan frequencies differing from 15.734 kHz. Four major sync signals are available from the I/C; composite sync including both horizontal and vertical scan timing information; a vertical sync pulse; a burst gate or back porch clamp pulse; and an odd and even output. The odd and even output level identifies which video field of an interlaced video source is present at the input. The outputs from the XD/XL1881 can be used to gen-lock video camera/VTR signals with graphics sources, provide identification of video fields for memory storage, recover suppressed or contaminated sync signals, and provide timing references for the extraction of coded or uncoded data on specific video scan lines.

To better understand the XD/XL1881 timing information and the type of signals that are used, refer to Figure 7(a-e) which shows a portion of the composite video signal from the end of one field through the beginning of the next field.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Composite sync Output

The composite sync output, Figure 7(b), is simply a reproduction of the signal waveform below the composite video black level, with the video completely removed. This is obtained by clamping the video signal sync tips to 1.5-V DC at Pin 2 and using a comparator threshold set just above this voltage to strip the sync signal, which is then buffered out to Pin 1. The threshold separation from the clamped sync tip is nominally 70 mV which means that for the minimum input level of 0.5 V (p-p), the clipping level is close to the halfway point on the sync pulse amplitude (shown by the dashed line on Figure 7(a). This threshold separation is independent of the signal amplitude, therefore, for a 2-V (p-p) input the clipping level occurs at 11% of the sync pulse amplitude. The charging current for the input coupling capacitor is 0.8 mA,

Normally the signal source for the XD/XL1881 is assumed to be clean and relatively noise-free, but some sources may have excessive video peaking, causing high-frequency video and chroma components to extend below the black level reference. Some video discs keep the chroma burst pulse present throughout the vertical blanking period so that the burst actually appears on the sync tips for three line periods instead of at black level. A clean composite sync signal can be generated from these sources by filtering the input signal. When the source impedance is low, typically 75 Ω, a

620-Ω resistor in series with the source and a 510-pF capacitor to ground will form a lowpass filter with a corner frequency of 500 kHz. This bandwidth is more than sufficient to pass the sync pulse portion of the waveform; however, any subcarrier content in the signal will be attenuated by almost 18 dB, effectively taking it below the comparator threshold. Filtering will also help if the source is contaminated with thermal noise. The output waveforms will become delayed from between 40 ns to as much as 200 ns due to this filter. This much delay will not usually be significant but it does contribute to the sync delay produced by any additional signal processing. Because the original video may also undergo processing, the need for time delay correction will depend on the total system, not just the sync stripper.

7.3.2 Vertical sync Output

A vertical sync output is derived by internally integrating the composite sync waveform (Functional Block Diagram). To understand the generation of the vertical sync pulse, refer to the lower left hand section Functional Block Diagram. Note there are two comparators in the section. One comparator has an internally generated voltage reference called V1 going to one of its inputs. The other comparator has an internally generated voltage reference called V2 going to one of its inputs. Both comparators have a common input at their noninverting input coming from the internal integrator. The internal integrator is used for integrating the composite sync signal. This signal comes from the input side of the composite sync buffer and are positive going sync pulses. The capacitor to the integrator is internal to the XD/XL1881. The capacitor charge current is set by the value of the external resistor RSET. The output of the integrator is going to be at a low voltage during the normal horizontal lines because the integrator has a very short time to charge the capacitor, which is during the horizontal sync period. The equalization pulses will keep the output voltage of the integrator at about the same level, below the V1. During the vertical sync period the narrow going positive pulses shown in Figure 7 is called the serration pulse. The wide negative portion of the vertical sync period is called the vertical sync pulse. At the start of the vertical sync period, before the first Serration pulse occurs, the integrator now charges the capacitor to a much higher voltage. At the first serration pulse the integrator output should be between V1 and V2. This would give a high level at the output of the comparator with V1 as one of its inputs. This high is clocked into the “D” flip-flop by the falling edge of the serration pulse (remember the sync signal is inverted in this section of the XD/XL1881). The “Q” output of the “D” flip-flop goes through the OR gate, and sets the R/S flip-flop. The output of the R/S flip-flop enables the internal oscillator and also clocks the ODD/EVEN “D” flip-flop. The ODD/EVEN field pulse operation is covered in Odd and Even Field Pulse. The output of the oscillator goes to a divide by 8 circuit, thus resetting the R/S flip-flop after 8 cycles of the oscillator. The frequency of the oscillator is established by the internal capacitor going to the oscillator and the external RSET. The “Q” output of the R/S flip-flop goes to pin 3 and is the actual vertical sync output of the XD/XL1881. By clocking the “D” flip-flop at the start of the first serration pulse means that the vertical sync output pulse starts at this point in time and lasts for eight cycles of the

internal oscillator as shown in Figure 7.

Feature Description (continued)

How RSET affects the integrator and the internal oscillator is shown under the Typical Performance Characteristics. The first graph is “RSET Value Selection vs Vertical Serration Pulse Separation”. For this graph to be valid, the vertical sync pulse should last for at least 85% of the horizontal half line (47% of a full horizontal line). A vertical sync pulse from any standard should meet this requirement; both NTSC and PAL do meet this requirement (the serration pulse is the remainder of the period, 10% to 15% of the horizontal half line). Remember this pulse is a positive pulse at the integrator but negative in Figure 7. This graph shows how long it takes the integrator to charge its internal capacitor above V1.

With RSET too large the charging current of the integrator will be too small to charge the capacitor above V1, thus there will be no vertical synch output pulse. As mentioned above, RSET also sets the frequency of the internal oscillator. If the oscillator runs too fast its eight cycles will be shorter than the vertical sync portion of the composite sync. Under this condition another vertical sync pulse can be generated on one of the later serration pulse after the divide by 8 circuit resets the R/S flip-flop. The first graph also shows the minimum RSET necessary to prevent a double vertical pulse, assuming that the serration pulses last for only three full horizontal line periods (six serration pulses for NTSC). The actual pulse width of the vertical sync pulse is shown in the “Vertical Pulse Width vs RSET” graph. Using NTSC as an example, lets see how these two graphs relate to each other. The Horizontal line is 64 μs long, or 32 μs for a horizontal half line. Now round this off to 30 μs. In the “RSET Value Selection vs Vertical Serration Pulse Separation” graph the minimum resistor value for 30 μs serration pulse separation is about 550 kΩ. Going to the “Vertical Pulse Width vs RSET” graph one can see that 550 kΩ gives a vertical pulse width of about 180 μs, the total time for the vertical sync period of NTSC (3 horizontal lines). A 550 kΩ will set the internal oscillator to a frequency such that eight cycles gives a time of 180 μs, just long enough to prevent a double vertical sync pulse at the vertical sync output of the XD/XL1881.

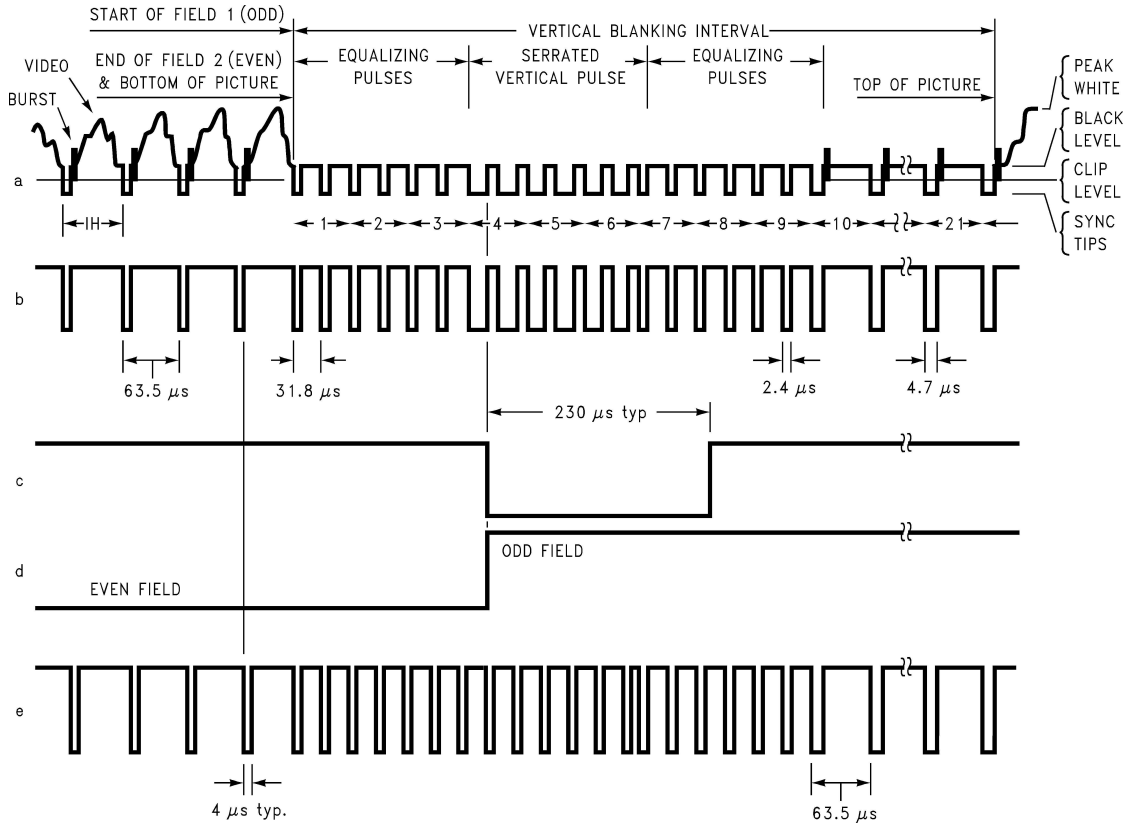
The XD/XL1881 also generates a default vertical sync pulse when the vertical sync period is unusually long and has no serration pulses. With a very long vertical sync time the integrator has time to charge its internal capacitor above the voltage level V2. Since there is no falling edge at the end of a serration pulse to clock the “D” flip-flop, the only high signal going to the OR gate is from the default comparator when output of the integrator reaches V2. At this time the R/S flip-flop is toggled by the default comparator, starting the vertical sync pulse at pin 3 of the XD/XL1881. If the default vertical sync period ends before the end of the input vertical sync period, then the falling edge of the vertical sync (positive pulse at the “D” flip-flop) will clock the high output from the comparator with V1 as a reference input. This will retrigger the oscillator, generating a second vertical sync output pulse. The “Vertical Default Sync Delay Time vs RSET” graph shows the

relationship between the RSET value and the delay time from the start of the vertical sync period before the default vertical sync pulse is generated. Using the NTSC example again the smallest resistor for RSET is 500 kΩ. The vertical default time delay is about 50 µs, much longer than the 30 µs serration pulse spacing.

A common question is how can one calculate the required RSET with a video timing standard that has no serration pulses during the vertical blanking. If the default vertical sync is to be used this is a very easy task. Use the "Vertical Default Sync Delay Time vs RSET" graph to select the necessary RSET to give the desired delay time for the vertical sync output signal. If a second pulse is undesirable, then check the "Vertical Pulse Width vs RSET" graph to make sure the vertical output pulse will extend beyond the end of the input vertical sync period. In most systems the end of the vertical sync period may be very accurate. In this case the preferred design may be to start the vertical sync pulse at the end of the vertical sync period, similar to starting the vertical sync pulse after the first serration pulse. A VGA standard is to be used as an example to show how this is done. In this standard a horizontal line is 32 µs long. The vertical sync period is two horizontal lines long, or 64 µs. The vertical default sync delay time must be longer than the vertical sync period of 64 µs. In this case RSET must be larger than 680 kΩ. RSET must still be small enough for the output of the integrator to reach V1 before the end of the vertical period of the input pulse. The first graph can be used to confirm that RSET is small enough for the integrator. Instead of using the vertical serration pulse separation, use the actual pulse width of the vertical sync period, or 64 µs in this example. This graph is linear, meaning that a value as large as 2.7 MΩ can be used for RSET (twice the value as the maximum at 30 µs). Due to leakage currents it is advisable to keep the value of RSET under 2.0 MΩ. In this example a value of 1.0 MΩ is selected, well above the minimum of 680 kΩ. With this value for RSET the pulse width of the vertical sync output pulse of the XD/XL1881 is about 340 µs.

Feature Description (continued)

Figure 7. (a) Composite Video; (b) Composite Sync; (c) Vertical Output Pulse; (d) Odd and Even Field Index; (e) Burst Gate or Back Porch Clamp



7.3.3 Odd and Even Field Pulse

An unusual feature of XD/XL1881 is an output level from Pin 7 that identifies the video field present at the input to the XD/XL1881. This can be useful in frame memory storage applications or in extracting test signals that occur in alternate fields. For a composite video signal that is interlaced, one of the two fields that make up each video frame or picture must have a half horizontal scan line period at the end of the vertical scan—that is, at the bottom of the picture. This is called the “odd field” or “even field”. The “even field” or “field 2” has a complete horizontal scan line at the end of the field. An odd field starts on the leading edge of the first equalizing pulse, whereas the even field starts on the leading edge of the second equalizing pulse of the vertical retrace interval. Figure 7(a) shows the end of the even field and the start of the odd field.

To detect the odd and even fields the XD/XL1881 again integrates the composite sync waveform (Functional Block Diagram). A capacitor is charged during the period between sync pulses and discharged when the sync pulse is present. The period between normal horizontal sync pulses is enough to allow the capacitor voltage to reach a threshold level of a comparator that clears a flip-flop which is also being clocked by the sync waveform. When the vertical interval is reached, the shorter integration time between equalizing pulses prevents this threshold from being reached and

the Q output of the flip-flop is toggled with each equalizing pulse. Because the half-line period at the end of the odd field will have the same effect as an equalizing pulse period, the Q output will have a different polarity on successive fields. Thus by comparing the Q polarity with the vertical output pulse, an odd and even field index is generated. Pin 7 remains low during the even field and high during the odd field.

7.3.4 Burst or Back Porch Output Pulse

In a composite video signal, the chroma burst is located on the back porch of the horizontal blanking period. This period, approximately 4.8 μs long, is also the black level reference for the subsequent video scan line. The XD/XL1881 generates a pulse at Pin 5 that can be used either to retrieve the chroma burst from the composite video signal (thus providing a subcarrier synchronizing signal) or as a clamp for the DC restoration of the video waveform. This output is obtained simply by charging an internal capacitor starting on the trailing edge of the horizontal sync pulses. Simultaneously the output of Pin 5 is pulled low and held until the capacitor charge circuit times out—4 μs later. A shorter output burst gate pulse can be derived by differentiating the burst output using a series C-R network. This may be necessary in applications which require high horizontal scan rates in combination with normal (60 Hz–120 Hz) vertical scan rates.

7.4 Device Functional Modes

7.4.1 Operation Mode

In the normal operation mode, the XD/XL1881 will extract video timing information and split the data up into the respective signals.

The XD/XL1881 will output four sync signals including the composite sync, a vertical sync pulse, a burst gate or back porch clamp pulse, and an odd and even output.

The outputs from the XD/XL1881can be used to gen-lock video camera/VTR signals with graphics sources, provide identification of video fields for memory storage, recover suppressed or contaminated sync signals, and provide timing references for the extraction of coded or uncoded data on specific video scan lines.

8. APPLICATION AND IMPLEMENTATION

NOTE

Information in the following applications sections is not part of the XINLUDA component specification, and XINLUDA does not warrant its accuracy or completeness. XINLUDA's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

Apart from extracting a composite sync signal free of video information, the XD/XL1881 outputs allow a number of interesting applications to be developed. As mentioned above, the burst gate or back porch clamp pulse allows DC restoration of the original video waveform for display or remodulation on an R.F. carrier, and retrieval of the color burst for color synchronization and decoding into R.G.B. components. For frame memory storage applications, the odd and even field lever allows identification of the appropriate field ensuring the correct read or write sequence. The vertical pulse output is particularly useful since it begins at a precise time—the rising edge of the first vertical serration in the sync waveform. This means that individual lines within the vertical blanking period (or anywhere in the active scan line period) can easily be extracted by counting the required number of transitions in the composite sync waveform following the start of the vertical output pulse.

The vertical blanking interval is proving popular as a means to transmit data which will not appear on a normal T.V. receiver screen. Data can be inserted beginning with line 10 (the first horizontal scan line on which the color burst appears) through to line 21. Usually lines 10 through 13 are not used which leaves lines 14 through 21 for inserting signals, which may be different from field to field. In the U.S., line 19 is normally reserved for a vertical interval reference signal (VIRS) and line 21 is reserved for closed caption data for the hearing impaired. The remaining lines are used in a number of ways. Lines 17 and 18 are frequently used during studio processing to add and delete vertical interval test signals (VITS) while lines 14 through 18 and line 20 can be used for Videotex/Teletext data. Several institutions are proposing to transmit financial data on line 17 and cable systems use the available lines in the vertical interval to send decoding data for descrambler terminals.

Because the vertical output pulse from the XD/XL1881 coincides with the leading edge of the first vertical serration, sixteen positive or negative transitions later will be the start of line 14 in either field. At this point simple counters can be used to select the desired line(s) for insertion or deletion of data.

8.2 Typical Applications

8.2.1 Video Line Selector

The circuit in Figure 8 puts out a singe video line according to the binary coded information applied to line select bits b0–b7. A line is selected by adding two to the desired line number, converting to a binary equivalent and applying the result to the line select inputs. The falling edge of the XD/XL1881's vertical pulse is used to load the appropriate number into the counters (MM74C193N) and to set a start count latch using two NAND gates. Composite sync transitions are counted using the borrow out of the desired number of counters. The final borrow out pulse is used to turn on the analog switch (XD4066) during the desired line. The falling edge of this signal also resets the start count latch, thereby terminating the counting.

The circuit, as shown, will provide a single line output for each field in an interlaced video system (television) or a single line output in each frame for a non-interlaced video system (computer monitor). When a particular line in only one field of an interlaced video signal is desired, the odd and even field index output must be used instead of the vertical output pulse (invert the field index output to select the odd field). A single counter is needed for selecting lines 3 to 14; two counters are needed for selecting lines 15 to 253; and three counters will work for up to 2046 lines. An output buffer is required to drive low impedance loads.

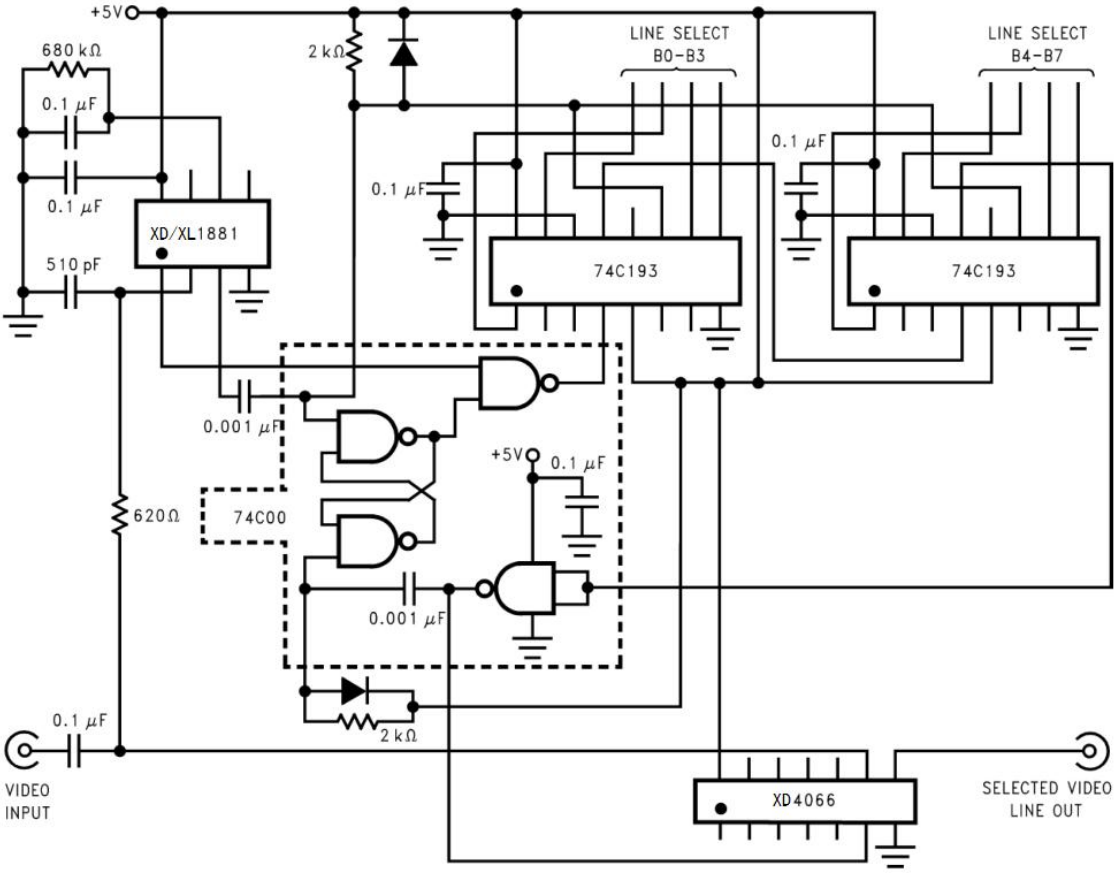


Figure 8. Video Line Selector

8.2.1.1 Design Requirements

The design must have a single line output in an interlaced video system. The use case can be used for televisions of computer monitors.

8.2.1.2 Detailed Design Procedure

For the composite input pin, a 510-pF capacitor and 620-Ω resistor are selected to create a lowpass filter for 500 kHz.

For Rset, a 680-kΩ was selected to allow for the Vertical Default Sync Delay Time to be set for 64 uS. Please refer to Figure 2 for Rset value selection.

9. POWER SUPPLY RECOMMENDATIONS

The XD/XL1881 is designed to operate from an input voltage supply range between 5 VDC and 12 VDC. The XD/XL1881 requires external a decoupling capacitor at Pin 8 and another at Pin 6.

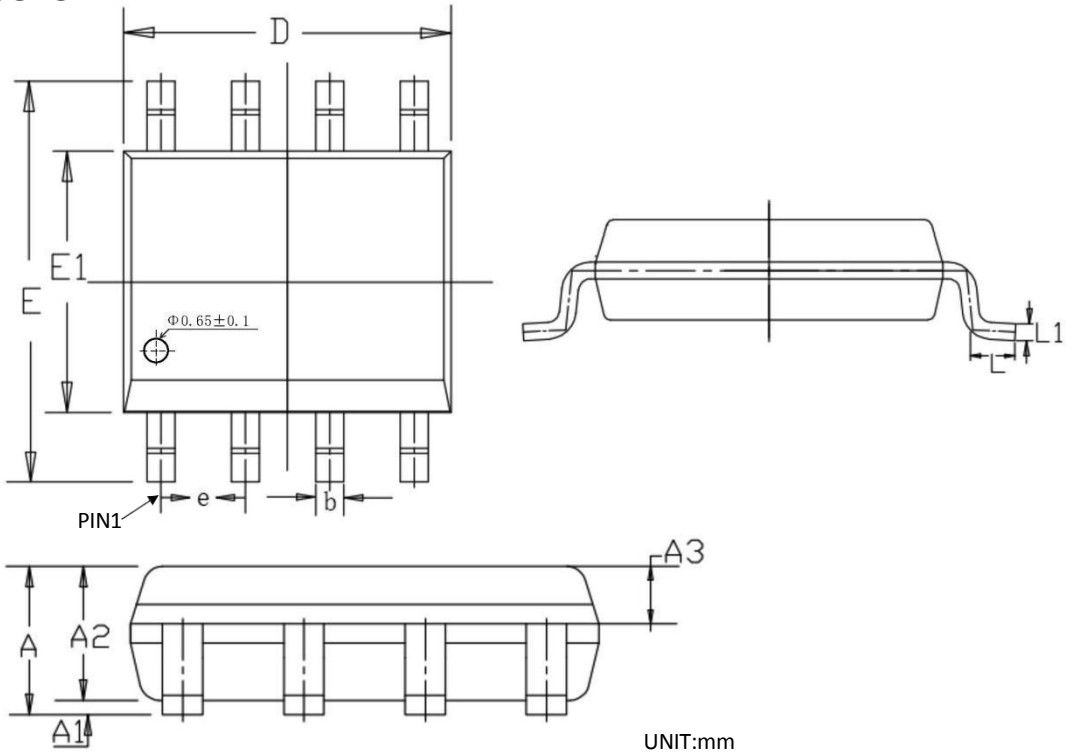
10. ORDERING INFORMATION

Ordering Information

Part Number	Device Marking	Package Type	Bodysize (mm)	Temperature (℃)	MSL	Transport Media	Package Quantity
XL1881	XL1881	SOP-8	4.90 * 3.90	- 0 to +70	MSL3	T&R	2500
XD1881	XD1881	DIP-8	9.25 * 6.38	- 0 to +70	MSL3	Tube 50	2000

11. DIMENSIONAL DRAWINGS

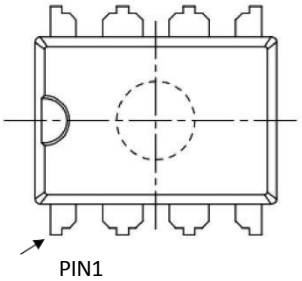
SOP8

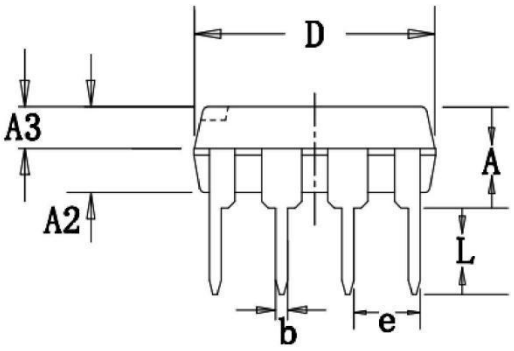


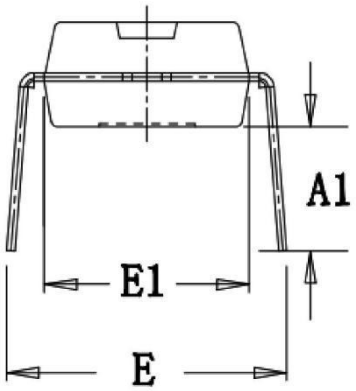
UNIT:mm

	MIN	NOM	MAX
A	1.450	1.550	1.650
A1	0.100	0.150	0.200
A2	1.300	1.400	1.500
A3	0.600	0.650	0.700
b	0.380	–	0.510
e	1.240	1.270	1.300
D	4.800	4.900	5.000
E	5.800	6.000	6.200
E1	3.800	3.900	4.000
L	0.450	0.600	0.750
L1	—	0.25BSC	—

DIP8







UNIT:mm

	MIN	NOM	MAX
A	3.600	3.800	4.000
A1	3.786	3.886	3.986
A2	3.200	3.300	3.400
A3	1.550	1.600	1.650
b	0.440	–	0.490
e	2.510	2.540	2.570
D	9.150	9.250	9.350
E	7.800	8.500	9.200
E1	6.280	6.380	6.480
L	3.000	–	–