74LVC2G07GM-TP
DUAL SCHMITT-TRIGGER BUFFER

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Features

- Wide Supply Voltage Range From 1.65V To 5.5V.
- 5 V tolerant input/output for interfacing with 5 V logic
- ±24-mA Output Drive at 3.3 V
- Latch-up performance exceeds 100mA
- ESD Protection Exceeds JESD 22
  -2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  -1000-V Charged-Device Model (C101)

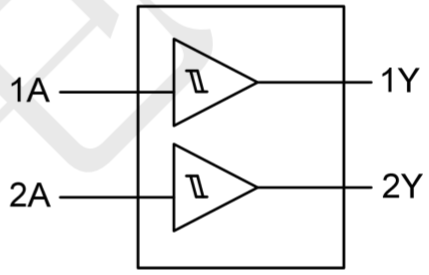
Applications

- AV Receiver
- Audio Dock:Portable
- Blu-ray Player and Home Theater
- Embedded PC
- Personal Digital Assistant(PDA)
- Power:Telecom/Server AC/DC Supply:Single Controller:Analog and Digital

General Description

The is a high-performance, low-power,low-voltage, Si-gate CMOS device which provides two independent buffers with Schmitt trigger action. It is capable of transforming slowly changed input signals into sharply defined, jitter-free output signals.

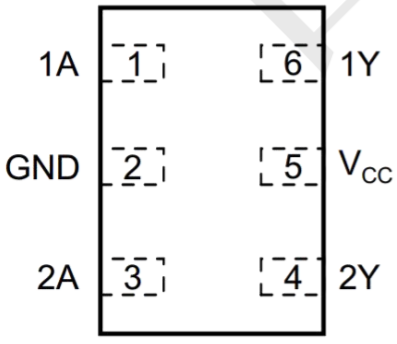
Logic Diagram



Ordering Information

ORDER NUMBER	PACKAGE DESCRIPTION	PACKAGE OPTION
74LVC2G07GM-TP	DFN1510-6	Tape and Reel,5000

Pin Configuratio



DFN1510-6

Function Table

INPUT(A)	OUTPUT(Y)
L	L
H	H

Note:H: HIGH voltage level;L: LOW voltage level.

Absolute Maximum Ratings (Unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	RATINGS	UNIT
Supply Voltage	V_{CC}		-0.5 ~ +6.5	V
Input Voltage	V_{IN}		-0.5 ~ +6.5	V
Output Voltage	V_{OUT}	High-Impedance & Power-Off State	-0.5 ~ +6.5	V
		High State & Low State	-0.5 ~ VCC+0.5	V
VCC or GND Current	I_{CC}		±100	mA
Continuous Output Current	I_{OUT}		±50	mA
Input Clamp Current	I_{IK}	V_{IN}<0	-50	mA
Output Clamp Current	I_{OK}	V_{OUT}<0	-50	mA
Storage Temperature Range	T_{STG}		-65 ~ +150	℃
Junction to Ambient	θ_{JA}	DFN1510-6	440	℃/W

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.
Absolute maximum ratings are stress ratings only and functional device operation is not implied.

Recommended Operating Conditions(Unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	VCC	Operating	1.65	--	5.5	V
Input Voltage	VIN		0	--	5.5	V
Output Voltage	VOUT	High or low state	0	--	VCC	V
High-Level Input Voltage	VT+	V_{CC} = 1.65 V	0.7	--	1.4	V
		V_{CC} = 2.3 V	1.0	--	1.7	V
		V_{CC} = 3.0 V	1.3	--	2.2	V
		V_{CC} = 4.5 V	1.9	--	3.1	V
		V_{CC} = 5.5 V	2.2	--	3.7	V
Low-Level Input Voltage	VT-	V_{CC} = 1.65 V	0.3	--	0.7	V
		V_{CC} = 2.3 V	0.4	--	1.0	V
		V_{CC} = 3.0 V	0.6	--	1.3	V
		V_{CC} = 4.5 V	1.1	--	2.0	V
		V_{CC} = 5.5 V	1.4	--	2.5	V
Hysteresis Voltage	ΔVT	V_{CC} = 1.65 V	0.3	--	0.8	V
		V_{CC} = 2.3 V	0.4	--	0.9	V
		V_{CC} = 3.0 V	0.4	--	1.1	V
		V_{CC} = 4.5 V	0.6	--	1.3	V
		V_{CC} = 5.5 V	0.7	--	1.4	V
Operating Temperature	TA		-40	--	+125	℃

Electrical Characteristics (unless otherwise specified)

PARAMETER	SYMBOL	TEST Conditions	MIN	TYP	MAX	UNIT
High-Level Output Voltage	V_{OH}	V_{CC}=1.65V~5.5V, I_{OH}=-100μA	V_{CC} -0.1	--	--	V
		V_{CC}=1.65V, I_{OH}=-4mA	1.2	--	--	V
		V_{CC}=2.3V, I_{OH}=-8mA	1.9	--	--	V
		V_{CC}=3.0V, I_{OH}=-16mA	2.4	--	--	V
		V_{CC}=3.0V, I_{OH}=-24mA	2.3	--	--	V
		V_{CC}=4.5V, I_{OH}=-32mA	3.8	--	--	V
Low-Level Output Voltage	V_{OL}	VCC=1.65 ~ 5.5V, IOL=100μA	--	--	0.1	V
		VCC=1.65V, IOL=4mA	--	--	0.45	V
		VCC=2.3V, IOL=8mA	--	--	0.3	V
		VCC=3.0V,IOH=16mA	--	--	0.4	V
		VCC=3.0V,IOH=24mA	--	--	0.55	V
		VCC=4.5V, IOH=32mA	--	--	0.55	V
Input Leakage Current	$I_{I(LEAK)}$	VCC=1.65V ~ 5.5V, VIN=5.5V or GND	--	±0.1	±5	uA
Power OFF Leakage Current	I_{OFF}	VCC=0V, VIN or VOUT=5.5V	--	±0.1	±10	uA
Quiescent Supply Current	I_{CC}	VCC=1.65 ~ 5.5V, VIN=VCC or GND, IOUT=0A	--	0.1	10	uA
Additional Quiescent Supply ent Per Input Pin	ΔI_{CC}	VCC=3.0 ~ 5.5V, VIN= VCC-0.6V, IO=0A,Other inputs at V_{CC} or GND	--	5	500	uA

OPERATING CHARACTERISTICS (f=10MHz, TA =25°C , unless otherwise specified)

PARAMETER	SYMBOL	TEST Conditions	MIN	TYP	MAX	UNIT
Input Capacitance	C_I	V_{IN}=V_{CC} or GND, V_{CC}=3.3V	--	4	--	pF
Power Dissipation Capacitance	C_{PD}	V_{CC}=5V, f=10MHz	--	21	--	pF

Notes: 1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}2 \times f_i \times N + \Sigma (C_L \times V_{CC}2 \times f_o)$ where:

f_i = Input Frequency in MHz; f_o= Output Frequency in MHz; C_L= Output Load Capacitance in PF;

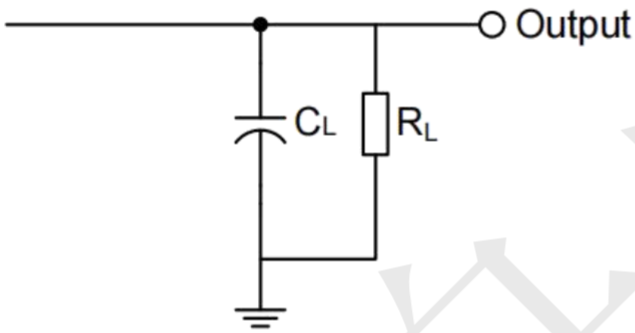
V_{CC} = Supply Voltage in Volts; N= Total Load Switching Outputs. $\Sigma (C_L \times V_{CC}2 \times f_o)$= Sum of Outputs.

2. The Condition is V_{IN} = GND to V_{CC}.

SWITCHING CHARACTERISTICS (see TEST CIRCUIT AND WAVEFORMS)

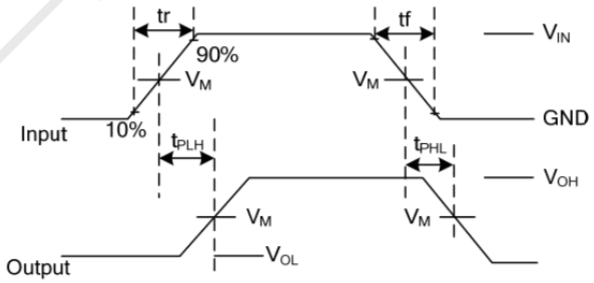
PARAMETER	SYMBOL	TEST Conditions	MIN	TYP	MAX	UNIT
Propagation delay nA to nY	t_{PLH} t_{PHL}	V_{CC} =1.8V±0.15V, C_L=30pF, R_L=1KΩ	3.9	--	9.3	nS
		V_{CC}=2.5V±0.2V, C_L=30pF, R_L=500Ω	1.9	--	5.7	nS
		V_{CC}=3.3V±0.3V, C_L=50pF, R_L=500Ω	2.2	--	5.4	nS
		V_{CC}=5V±0.5V , C_L=50pF, R_L=500Ω	1.5	--	4.3	nS

TEST CIRCUIT AND WAVEFORMS



V_{CC}	V_{IN}	t_R, t_F	V_M	C_L	R_L
1.65V~1.95V	V_{CC}	≤2ns	$V_{CC}/2$	30pF	1kΩ
2.3V~2.7V	V_{CC}	≤2ns	$V_{CC}/2$	30pF	500Ω
3.0V~3.6V	3V	≤2.5ns	1.5V	50pF	500Ω
4.5V~5.5V	V_{CC}	≤2.5ns	$V_{CC}/2$	50pF	500Ω

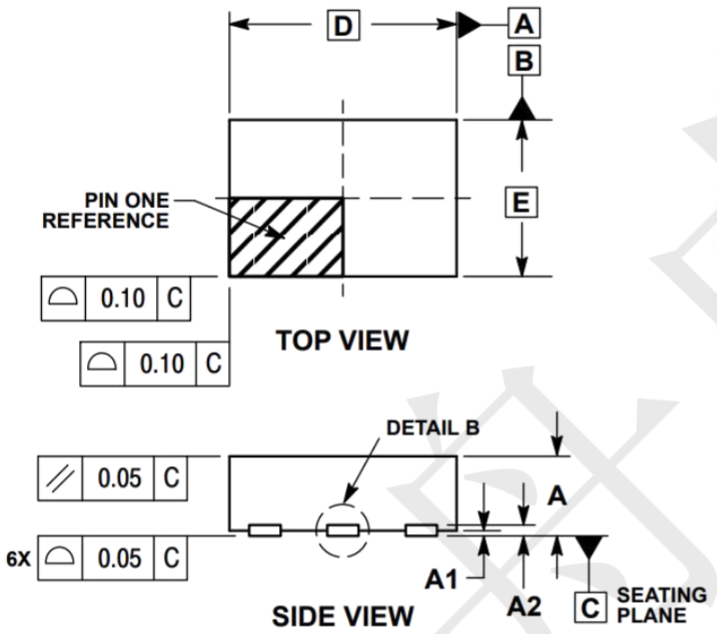
Definitions for test circuit:
R_L = Load resistance.
C_L = Load capacitance including jig and probe capacitance.



Notes: 1. V_{OL} and V_{OH} are typical output drop that occur with the output load.
2. t_{PLH} and t_{PHL} are the same as t_{PD} .

Package information

DFN1510-6 (unit: mm)



DIM	MILLIMETERS	
	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A2	0.07 REF	
b	0.20	0.30
D	1.45 BSC	
E	1.00 BSC	
e	0.50 BSC	
L	0.30	0.40
L1	---	0.15

Mounting Pad Layout (unit: mm)