60V/1.2MHz high-efficiency boost LED constant current driver

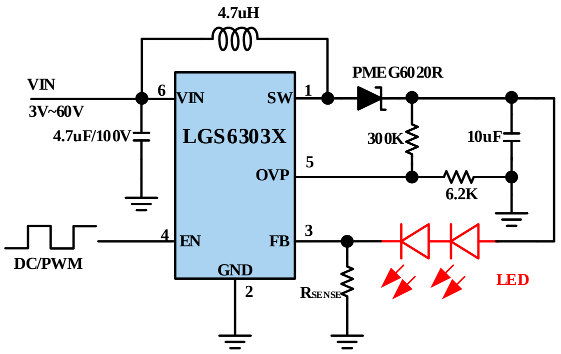
Check for Samples: LGS6303X

Features

- Wide input/output voltage range: 3.0V-60V
- Supports PWM dimming and analog dimming
- Built in 350m Ω low side metal oxide semiconductor field-effect transistor
- Maximum boost efficiency of 94%
- Periodic peak current limiting protection
- SKIP mode provides extremely high light load efficiency
- Provide ultra small SOT23-6 package and enhanced heat dissipation ESOP8 package.
- Built in soft start circuit to prevent overcurrent
- Thermal shutdown protection
- Input undervoltage protection
- Adjustable output overvoltage protection
- Internal loop compensation helps reduce solution size, cost, and design complexity
- All ports have ± 2000V (HBM) ESD protection
- The junction temperature range is -40 ℃ to+125 ℃

Application

- Boost type headlights
- Intelligent dimming LED light
- MR16 LED spotlight



SOT23-6 package typical application topology

Description

LGS6303X LGS6303X is an integrated power switch boost DC-DC LED driver chip with a wide input voltage range of 3V to 60V. It integrates soft start to minimize the need for external surge suppression components, making it an ideal choice for wide input power range LED drivers. The output current can be adjusted through an external resistor. The LGS6303X features an integrated 350m Ω power switch that can provide at least 1.5A of input peak current capability, with excellent load and line transient response. Equipped with SKIP control mode, it combines low static current with high switching frequency to achieve high efficiency over a wide range of load currents.

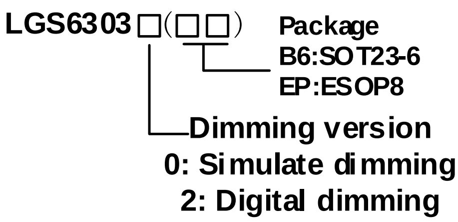
Additional features include: soft start, adjustable output overvoltage protection, thermal shutdown, UVLO undervoltage locking, and cycle by cycle peak current limiting protection.

LGS6303X can achieve high-precision digital and analog adjustment of output current by selecting sampling resistors RSET with different resistance values, including two specific models LGS63030 and LGS63032:

- LGS63030 supports DC dimming for analog inputs (0.6V~1.2V) and PWM dimming for digital inputs (100HZ~1KHZ).
- LGS63032 supports PWM dimming with digital input (100HZ~100KHZ), and there is no screen flicker under high-frequency PWM input. The dimming ratio is as high as 25000:1 at a PWM frequency of 100Hz.

LGS6303X can provide small-sized 6-pin SOT23-6 package and enhanced heat dissipation 8-pin ESOP8 package.

Purchasing information



Number	Package	Top mark	illustration
LGS63030B6	SOT23-6	63030	YX: Factory Version
LGS63030EP	ESOP8	63030 YX	
LGS63032B6	SOT23-6	63032	

Absolute maximum (†)

Table 3.1

parameter	range
Pin to GND voltage (VIN, SW)	-0.3V~60V
Pin to GND voltage (FB, EN, OVP)	-0.3V~6V
Maximum current of switch tube	3A
storage temperature	-65℃ to 150℃
operation temperature	-40℃ to 125℃
ESD rating (HBM)	±2KV
ESD rating (CDM)	±500V

† Note: If the operating conditions of the device exceed the "absolute maximum value" mentioned above, it may cause permanent damage to the device. This is only a limit parameter, and it is not recommended for the device to operate at or beyond the limit values mentioned above. Long term operation of the device under extreme conditions may affect its reliability.

ESD warning

ESD (electrostatic discharge) sensitive devices.

Charged components and circuit boards may discharge without being noticed. Although this product has patented or proprietary protection circuits, the device may be damaged in the event of high-energy ESD. Therefore, appropriate ESD prevention measures should be taken to avoid device performance degradation or functional loss.

Pin arrangement

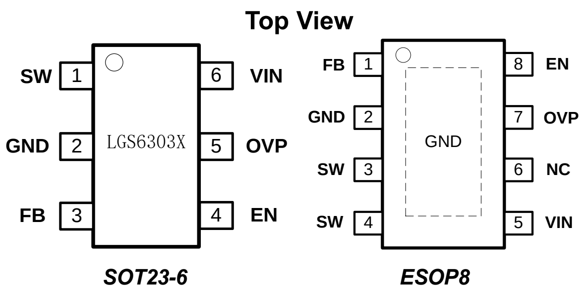


Figure 3.1 Packaging and Pin Arrangement

Table 3.2 Pin Function Description

Pin Numbering		Pin Name	说明
SOT23	**ESOP**		
1	3,4	SW	Internal power switch node. External connection power inductor and Schottky diode.
2	2	GND	Grounding pin.
3	1	FB	Feedback input pin. Connected to an external resistor, the output constant current value can be set through $R_{\_sense}$, and the output current is determined by $V_{\_FB}$ and $R_{\_sense}$, which can be set using this formula: $I_{OUT} = V_{FB}/R_{Sence}\ (A)$。
4	8	EN	Dimming input pin, can input DC and PWM square waves for dimming, see "Dimming Settings" for details.
5	7	OVP	Overvoltage protection pin, connected to the output pin and ground voltage divider resistor. Please ensure that the pin is less than 1V.
6	5	VIN	Drive power input pins, use 4.7uF or larger ceramic patches as close as possible to bypass VIN and GND.
-	6	NC	No external components are required, please ensure that the pin is suspended.

Technical specifications

Unless otherwise specified, the limit values apply to the working junction temperature (TJ) range of -40 ℃ to+125 ℃. The minimum and maximum limits are determined through experiments, verification, and statistical correlation regulations. The typical value represents the most likely parameter specification at TJ=25 ℃, for reference only. All voltages are relative to GND.

Table 4

parameter		test condition	MIN	TYP	MAX	Unit
Input Characteristic						
V_{IN}	Recommended input voltage range		3.0		60	V
V_{UVLO}	Input undervoltage locking rising edge	Rising		3.0		V
	Fall edge	Falling		2.6		V
I_Q	Quiescent current	No load，No switch,VIN=12V, EN=2V, FB=1V.		180		uA
I_S	ShutDown Current	EN=0, VIN=12V		10		uA
Switching characteristic						
$R_{DS(ON)}$	BOOST upper tube R_{DSON}	TJ= 25℃	330	350	410	mΩ
V_{FB}	FB feedback voltage		0.195	0.2	0.205	V
F_{SW}	switching frequency	PWM Operation	1.05	1.2	1.35	MHZ
F_{SW_FB}	Switching frequency of soft start	VIN=12V，EN=1		$1/4\,F_{sw}$		MHZ
D_{MAX}	Maximum duty cycle		85	90		%
$I_{LIMIT.SW(Peak)}$	SW current limit		1.5	1.7	2.1	A
V_{FB}	FB feedback voltage		0.195	0.2	0.205	V
$I_{FB.BIAS}$	FB bias current			50		nA
$I_{SW.LKG}$	SW leakage current				4	uA
Enable/Dimming (3V≤VIN≤60V)						
V_{EN_min}	Simulate dimming lower limit voltage	3V≤VIN≤60V	0.6	0.62	0.65	V
V_{EN_max}	Simulate dimming upper limit voltage	3V≤VIN≤60V	1.2	1.22	1.25	V
V_{EN_H}	Digital dimming rising edge 63032	EN=0 ↗ EN=1	0.31	0.5	0.54	V
V_{EN_L}	Digital dimming falling edge 63032	EN=1 ↘ EN=0	0.25	0.35	0.38	V
I_{EN}	EN input current	V_{EN}=5V	5		10	uA
OVP						
V_{OVP}	Overvoltage protection voltage rising edge			1		V
	Falling edge			0.86		V
Global thermal protection characteristics						
T_{OTP-R}	Over Temperature Protection	TJ Rising		150		℃
T_{OTP-F}	Over temperature protection released	TJ Falling		120		℃

Functional Block Diagram

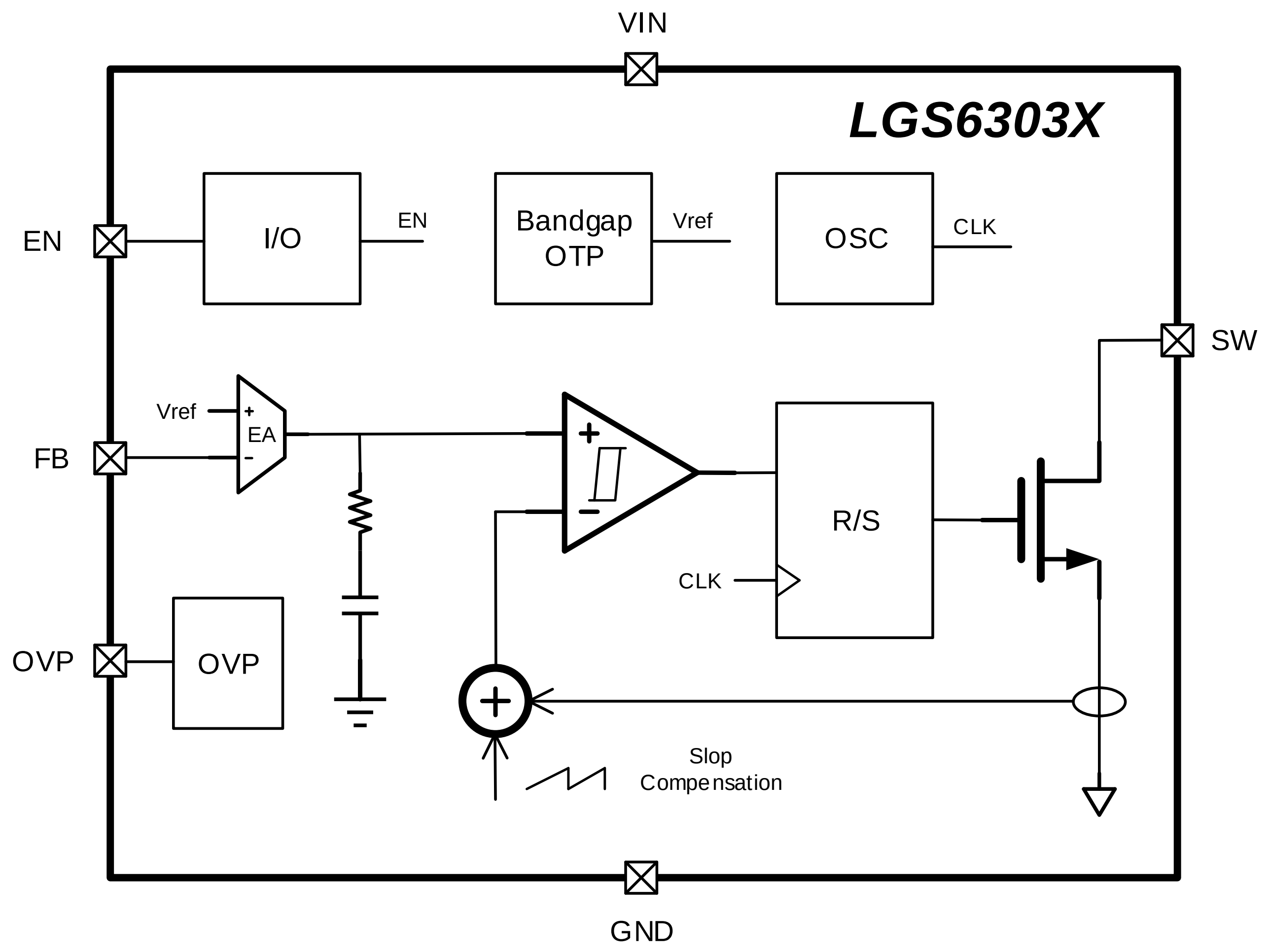


Figure 6 Internal functional block diagram

Application Information: Typical Application Circuits

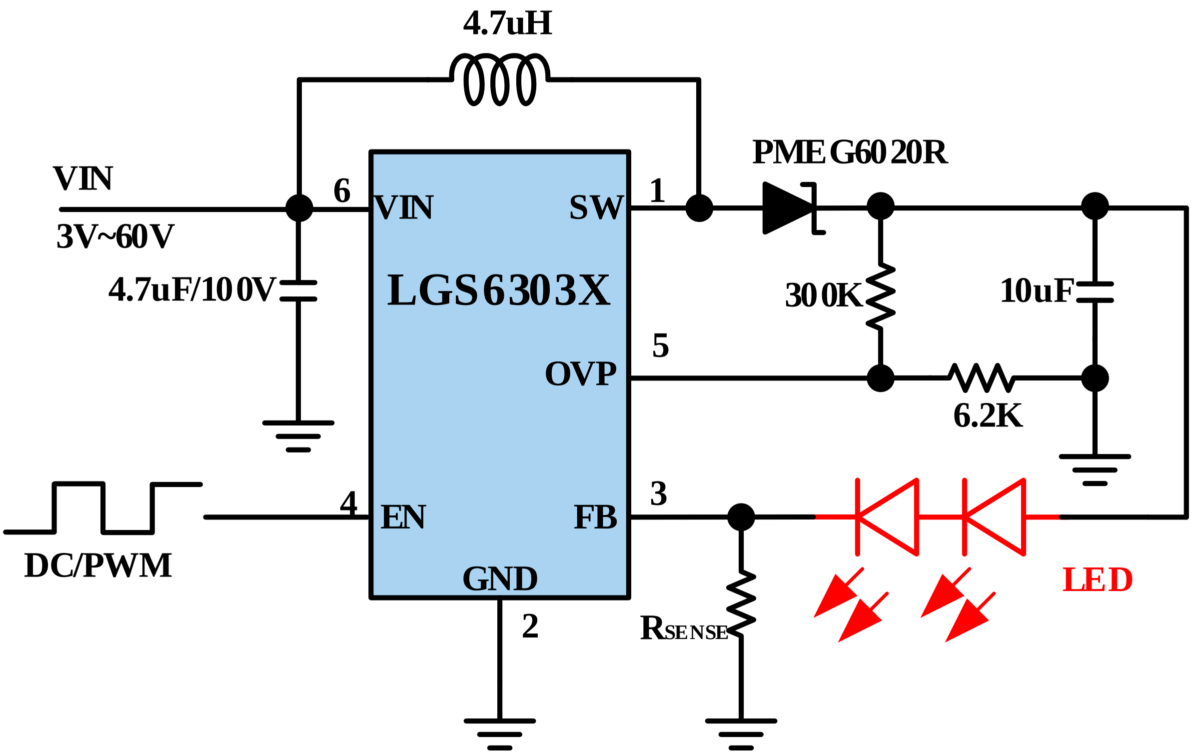


Figure 7 Typical application topology of DC-DC boost mode

NOTE：

- Feedback input pin. Connected to an external resistor, the output cross current value can be set by R_SENSE, and the output current is determined by VFB and R_SENSE, which can be set using this formula:

$$I_{OUT} = V_{FB}/R_{Sence}\ (A)。$$

- It is recommended to use 10uF X7R or X5R ceramic capacitors as input capacitors, and place them as close as possible to the power input pin and GND pin.

Application Information: High Efficiency Constant Current Boost Driver (Overview)

LGS6303X is an integrated power switch boost DC-DC LED driver chip with a wide input voltage range of 3V to 60V. It integrates soft start to minimize the need for external surge suppression components, making it an ideal choice for wide input power range LED drivers. The output current can be adjusted through an external resistor.
Equipped with an integrated 350m Ω power switch, it can provide an input peak current capability of at least 1.5A and has excellent load and line transient response. Equipped with SKIP control mode, it combines low static current with high switching frequency to achieve high efficiency over a wide range of load currents.
Additional features include: soft start, adjustable output overvoltage protection, thermal shutdown, UVLO undervoltage locking, and cycle by cycle peak current limiting protection.

Setting Output Current

The output current of LGS6303X can be adjusted by an external sampling resistor voltage divider, and its output current accuracy can reach ± 3%. The recommended output current values are shown in the table below.
The output current can be calculated based on V_{FB} and the selected R_SENSE. The typical value of V_{FB} is 0.2V

$$I_{OUT} = \frac{V_{FB}}{R_{Sence}} \quad (V)$$

Table 8 Fast configuration of output current setting

I_{OUT}	R_{SENSE}	Setting error (1)	
10mA	20Ω	10mA	0%
20mA	10Ω	20mA	0%
50mA	3.9Ω	51mA	-2%
100mA	2Ω	100mA	0%
200mA	1Ω	200mA	0%
300mA	0.68Ω	294mA	-2%
400mA	0.5Ω	400mA	0%

(1) Other sampling resistors and high-precision resistors can also be selected to achieve higher setting accuracy.

SKIP pulse skipping mode

LGS6303X has a built-in pulse skipping circuit; When under light load, the circuit is turned on; Only switch when necessary to maintain the output voltage within the specified range. This can reduce switch losses and allow the driver to maintain high efficiency under light load conditions.
In pulse skipping mode, when the output voltage drops below the specified value, LGS6303X enters PWM mode and stays for several oscillator cycles to raise the output voltage to the specified range. During the waiting time between sudden pulses, the power switch is turned off and all load currents are provided by the output capacitor. Due to the periodic sudden drops and recovery of the output voltage, the ripple of the output voltage in this mode is greater than that in the PWM working mode.

Input undervoltage protection (VULO)

There is an internal undervoltage lockout circuit on the VIN pin of the device. When the VIN voltage drops below the threshold of UVLO, UVLO protection will be triggered and the regulator output will be turned off. The rising threshold of the UVLO is about 3.0V. When VIN reaches this voltage and the UVLO is removed, the controller will enter the soft start process.

Maximum duty cycle DMAX

When the input voltage approaches the output voltage, BOOST switches to the maximum duty cycle operating state. At this time, the low-end N-channel MOSFET is in the open state, reducing the turn off time to the shortest. Under maximum duty cycle operating conditions, due to the input voltage being the product of the output voltage value and (1-D_MAX), the output voltage drops sharply below the regulation range.

Soft Start

The soft start of LGS6303X can prevent underdamped and overshoot of the input power supply of the converter during the startup process. When the chip starts up, the internal circuit generates a soft start voltage (SS), and the switching frequency decreases to 1/4 of the maximum switching frequency, causing the current to rise at a fixed rate. During soft start, the output voltage will track the internal node voltage ramp proportionally.
When it is smaller than the internal reference (REF), SS covers REF, so the error amplifier uses SS as a reference. When SS exceeds REF, REF resumes control. Throughout the entire startup phase, the switch current limitation remains effective, which can reliably avoid situations where power is applied and short circuits occur.
When the output has a very large capacitance (such as 2200uf or even larger), the output voltage rise speed will be slower than SS, limited by the maximum switch current limit, and the time to start to the target voltage setting value will be extended.

Application Information: High Efficiency Constant Current Boost Driver (Overview)

EN dimming instructions

EN is the enable input pin for BOOST. Drive EN to a high level state to turn on the driver; Drive EN to a low level state to turn off the driver. This pin has two independent thresholds. When the rising threshold is greater than 0.5V, the output is enabled. When the falling threshold is less than 0.4V, the regulator output is turned off and the low-power sleep mode is entered. This pin has an 800K pull-down inside.

External logic signals can also be used to drive EN inputs for system sorting and protection. Due to weak internal pull-down, it is not recommended to leave this pin hanging for reliable shutdown of external pull-down resistors.

Table 9 Operating Status of Pin EN

PIN	direction	Pin status	function
EN（Pin4）	input	High	BOOST Output enabled
		Low	BOOST Output off

Simulation dimming of LGS63030

LGS63030 supports analog dimming (0.6V~1.2V) and PWM dimming (100HZ~1KHZ) of LEDs by reusing EN pins. Simulated dimming is achieved through DC voltage. A DC voltage V_{EN} can be added to the EN end to reduce the LED output current. The maximum output LED current is determined by the sampling resistor. The calculation formula for the real-time average output current of LED simulated dimming is:

$$I_{OUT} = \frac{0.2 \times (V_{EN} - 0.6)}{0.6 \times R_{Sence}} \quad (0.6V \le V_{EN} \le 1.2V)$$

When V_{EN} is greater than 1.2V and less than the withstand voltage value of 6V, the LED current remains 100% equal to the set maximum average LED current.

PWM dimming of LGS6303X

Both LGS63030 and LGS63032 support PWM dimming, which allows the output current of the LED to vary from 0% to 100%. The brightness of LED is determined by the duty cycle of PWM signal. For example, the PWM signal has a 25% duty cycle, and the average current of the LED is 25% of (0.2/RSENSE). Suggest setting the PWM dimming frequency above 120Hz to avoid human interference

The eyes can see the flashing of the LED. The advantage of PWM dimming over analog dimming is that it does not change the chromaticity of the LED. The specific EN dimming range supported by the two chips is:

- LGS63030 supports PWM dimming for digital inputs (100HZ~1KHZ)
- LGS63032 supports PWM dimming with digital input (100HZ~25KHZ), and there is no screen flicker under high-frequency PWM input. The dimming ratio is as high as 25000:1 at a PWM frequency of 100Hz.

By comparison, it can be seen that the dimming frequency support range of LGS63032 is wider, up to 100KHZ, and the dimming ratio is also higher. For those who need PWM dimming, it is more recommended to choose LGS63032.

For the calculation formula of real-time average output current for PWM dimming of LGS63030:

If the EN high level is higher than 1.2V, then

$$I_{OUT} = \frac{0.2 \times D}{R_{Sence}} \quad \left(0\% \le D \le 100\%，1.2V \le V_{EN} \le 6V\right)$$

If the EN high level is less than 1.2V, then

$$I_{OUT} = \frac{(V_{EN} - 0.6) \times 0.2 \times D}{R_{Sence} \times 0.6}$$

$$\left(0\% \le D \le 100\%，0.6V \le V_{EN} \le 1.2V\right)$$

For the calculation formula of real-time average output current for PWM dimming of LGS63032:

$$I_{OUT} = \frac{0.2 \times D}{R_{Sence}} \quad \left(0\% \le D \le 100\%，0.6V \le V_{EN} \le 6V\right)$$

Among them:

D is the duty cycle of PWM.

Switch current limiting protection

The regulator output has a cycle by cycle overcurrent limitation. When SW current triggers

Limit. SW (Peak), BOOST output will enter a cycle by cycle current limiting state.

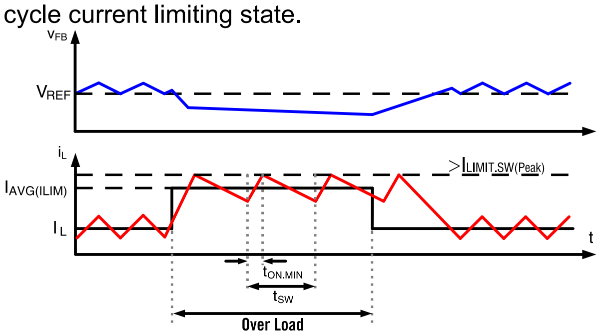


Figure 9 Description of BOOST output overcurrent to Mtop behavior

ILIMIT.SW (Peak) is related to inductance size and input voltage difference, while ILIMIT.SW (Peak) only

To reference the minimum value. When there is a prolonged overcurrent or short circuit, it may trigger global OTP protection.

Application Information: High Efficiency Constant Current Boost Driver (Overview)

OTP overheat protection

The thermal overload protection circuit limits the junction temperature to below 150 ℃ (typical value). Under extreme conditions (i.e. high ambient temperature and/or high power consumption), when the junction temperature starts to rise above 150 ℃, the over temperature protection is activated and the system will forcibly shut down the regulator output (if EN is enabled). When the junction temperature drops below 130 ° C, the OTP state will unlock, the regulator output will restart, and the output current will return to normal operating value. Thermal overload protection aims to protect devices from the effects of momentary accidental overload conditions.

The guaranteed operating junction temperature range of this device is -40 ° C to 125 ° C. High junction temperature will reduce the working life; When the junction temperature remains high at 125 ° C for a long time, the lifespan of the device will be shortened. Please note that the maximum ambient temperature consistent with these specifications depends on specific operating conditions, circuit board layout, rated package thermal resistance, and other environmental factors.

The junction temperature (TJ, unit: ℃) is calculated based on the ambient temperature (TA, unit: ℃) and power consumption (PD, unit: W), using the following formula:

$$\boldsymbol{T_J = T_A + (P_D \times \theta_{JA})}$$

Among them, θ JA (unit: ℃/W) is the thermal resistance of the package.

Output overvoltage protection (OVP)

The output overvoltage protection circuit prevents LED beads from disconnecting and damaging the chip. Set the overvoltage protection threshold based on the actual number of LED beads and the proportion of external circuits. The typical value of OVP trigger point voltage is 1V, and the recovery point voltage is 0.86V.

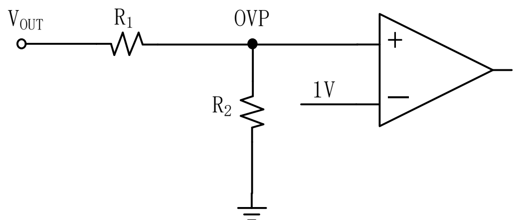


Figure 10 Setting OVP voltage

The overvoltage protection threshold can be calculated according to the following formula:

$$V_{OUT\_OVP} = \left(1 + \frac{R_1}{R_2}\right) \times 1 \ \ (V)$$

It is recommended to set the overvoltage protection threshold at 1.3 to 1.5 times the normal output voltage.

Application Information: High Efficiency Constant Current Boost Driver (Overview)

Input capacitance CIN

The typical value of input capacitance is 4.7 μ F. If further reduction of input/output ripple is required, larger capacitors can be selected. The rated voltage must be greater than the maximum input voltage required by the IC, preferably at least twice the maximum input voltage (1). The capacitance impedance of the input capacitor should be as small as possible at the switching frequency, and it is recommended to use X5R or X7R ceramic capacitors. To minimize potential input noise issues, please place this ceramic capacitor close to the IN and GND pins to reduce the loop area formed by the CIN and IN/GND pins.

(1) The DC bias effect of ceramic capacitors causes a decrease in the effective value of the capacitor.

Output capacitor COUT

Choose output capacitors to handle output current ripple noise. For the best performance requirements, it is recommended to use ceramic capacitors with a capacitance of 10 μ F and made of X5R or X7R material. If using a chip requires PWM dimming mode, there are two ways to reduce the whistling problem caused by the piezoelectric effect of the output capacitor in this situation:

(1) It is recommended to use capacitors such as tantalum capacitors and thin film capacitors that do not have piezoelectric effects, or ceramic plug-in capacitors instead of ceramic capacitors. This method abandons the advantages of MLCC's thinness, so in practical applications, issues such as volume space, reliability, and cost need to be considered.

(2) In scenarios where PWM dimming is required, it is recommended to use LGS63032. This chip can use a higher dimming frequency to avoid the human ear recognition range, thereby achieving the goal of eliminating capacitor howling.

Power inductor L

The selection of inductance needs to consider the following aspects:

(1) Choose an inductor to provide the required current ripple. It is recommended to choose a current ripple of about 20-50% of the current maximum output current, and the inductance calculation formula is as follows:

$$L = \left(\frac{V_{IN}}{V_{OUT}}\right)^2 \times \frac{(V_{OUT} - V_{IN})}{f_{SW} \times I_{OUT(MAX)} \times K}$$

Where F_SW is the switching frequency, I2 (OUT (MAX)) is the LED current, and the constant K is the percentage of inductor current ripples. For LGS6303X, the optimal selection range for Boost topology inductance in typical application circuits is 4.7 μ H to 47 μ H. For the best loop stability and efficiency curve, the recommended inductance value is 4.7 μ H.

(2) To ensure circuit safety, it is necessary to choose an inductor with a saturation current rating greater than the peak current under full load conditions. It is recommended to choose an inductor with a saturation current that exceeds the peak current of the inductor by 30% to 40% during normal operation. The peak current of an inductor can be calculated according to the following formula:

$$I_{L(PEAK)} = \frac{V_{OUT}}{V_{IN}} \times I_{OUT(MAX)} + \left(\frac{V_{IN}}{V_{OUT}}\right)^2 \times \frac{(V_{OUT} - V_{IN})}{2 \times f_{SW} \times L}$$

Power diode D

LGS6303X requires an external freewheeling diode between the SW pin and the output. The reverse voltage rating of the selected diode must be greater than VOUTMAX, and the peak rated current of the diode must be greater than the maximum inductor current. Due to the low forward voltage drop and fast switching speed of Schottky diodes, it is recommended to use Schottky diodes for optimal efficiency.

Application Information: Typical Application Features

Unless otherwise specified, L=4.7 μ H, COUP=10 μ F, TA=25 ℃

Figure 11.1 Efficiency vs Input Voltage

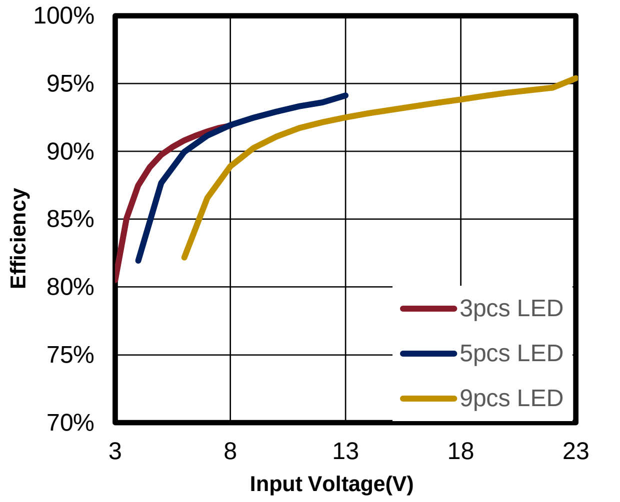


Figure 12.1.a I_{OUT}=200mA

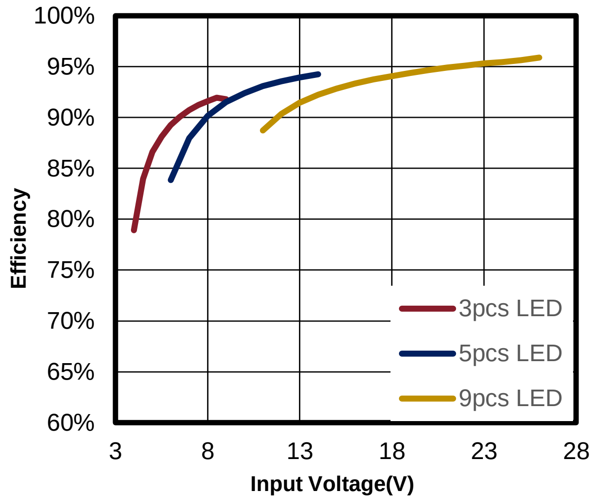


Figure 12.1.b I_{OUT}=400mA

Figure 11.2 LED Current vs Input Voltage

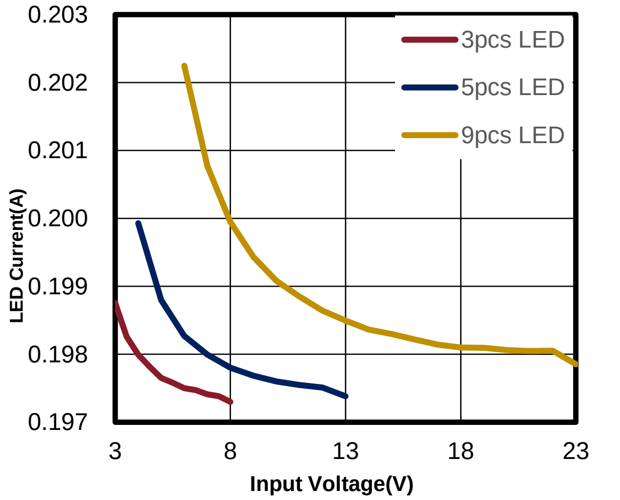


Figure 12.2.a I_{OUT}=200mA

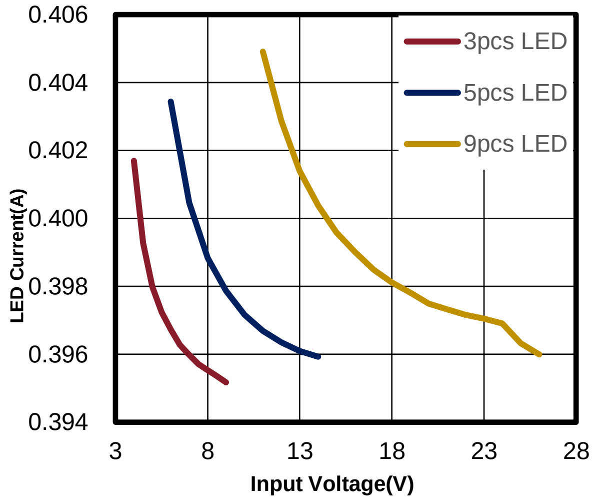


Figure 12.2.a I_{OUT}=400mA

Application Information: Typical Application Features

Unless otherwise specified, L=4.7 μ H, COUP=10 μ F, TA=25 ℃

Figure 12.1 Analog Dimming Curve

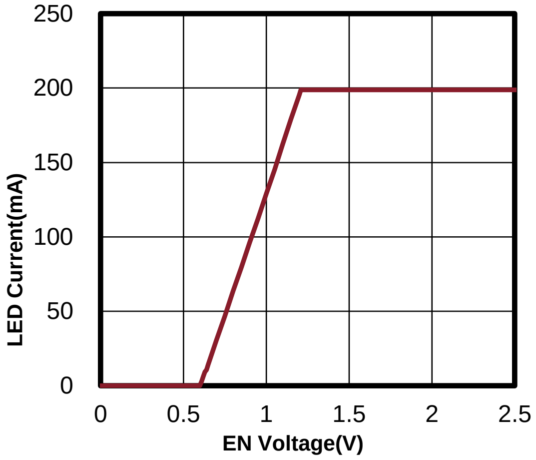


Figure 13.1.a LGS63030, V_{IN}=5V,3pcs LED Series

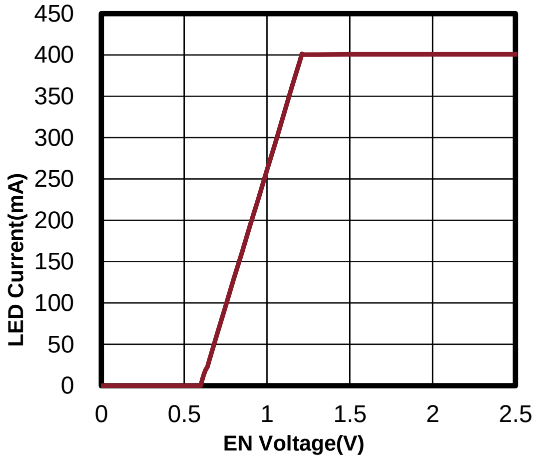


Figure 13.1.b LGS63030, V_{IN}=5V,3pcs LED Series

Figure 12.2 PWM Dimming Curve

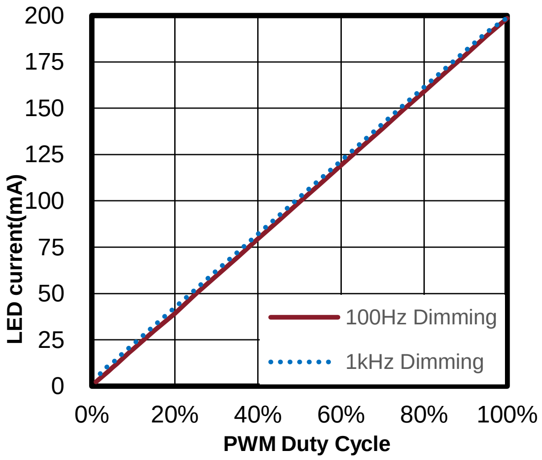


Figure 13.2.a LGS63030, V_{IN}=5V,3pcs LED Series

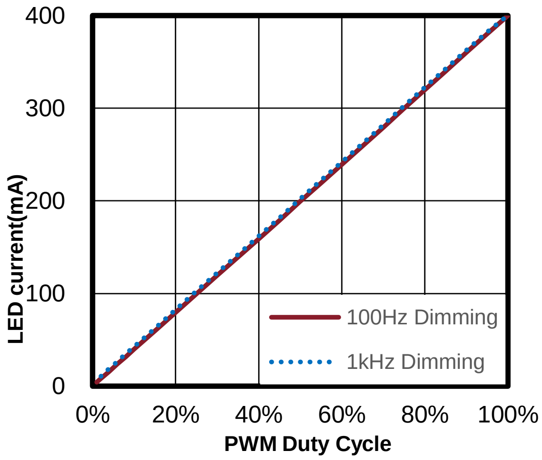


Figure 13.2.b LGS63030, V_{IN}=5V,3pcs LED Series

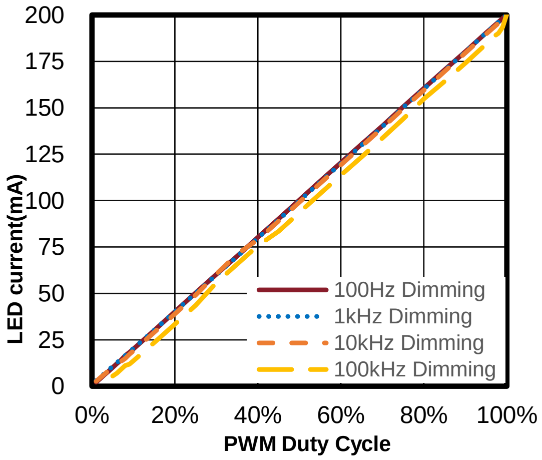


Figure 13.2.c LGS63032,V_{IN}=5V,3pcs LED Series

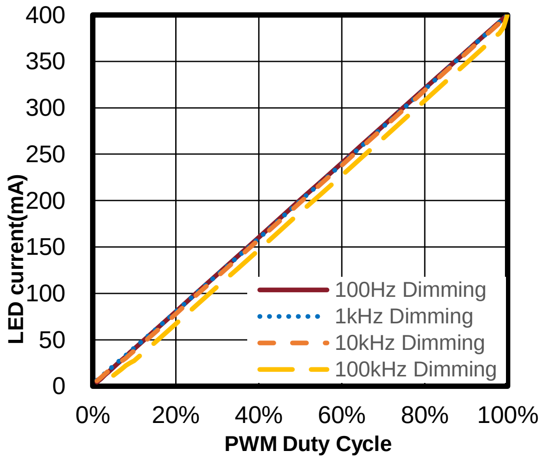


Figure 13.2.d LGS63032,V_{IN}=5V,3pcs LED Series

Application Information: Typical Application Features

Unless otherwise specified, L=4.7 μ H, COUP=10 μ F, TA=25 ℃

Figure 13.1 EN Start-Up/Shut-down Waveforms

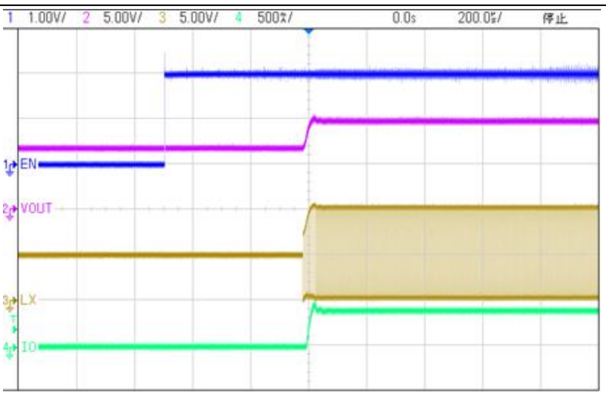


Figure 14.1.a V_{IN}=5V, I_{OUT}=400mA, 3pcs LED Series

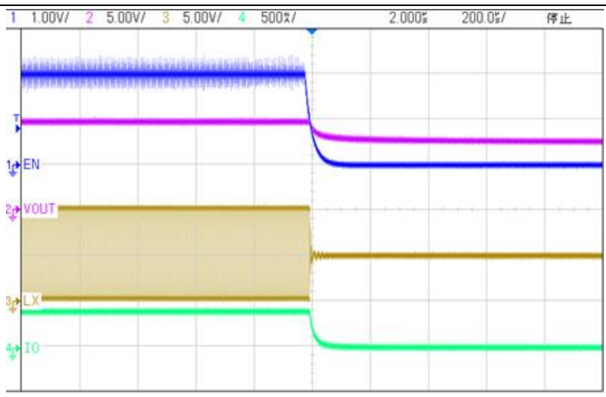


Figure 14.1.b V_{IN}=5V, I_{OUT}=400mA, 3pcs LED Series

Figure 13.2 Vin Start-Up/Shut-down Waveforms

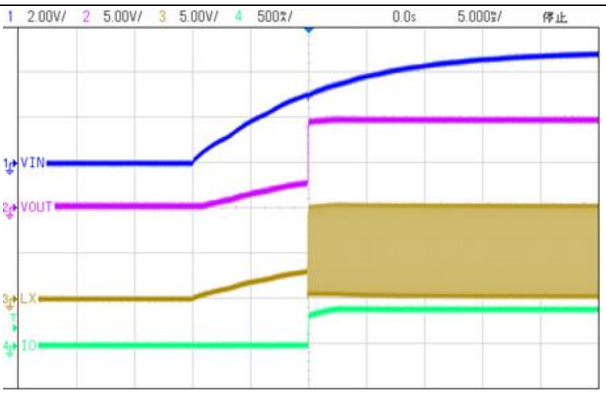


Figure 14.2.a V_{IN}=5V, I_{OUT}=400mA, 3pcs LED Series

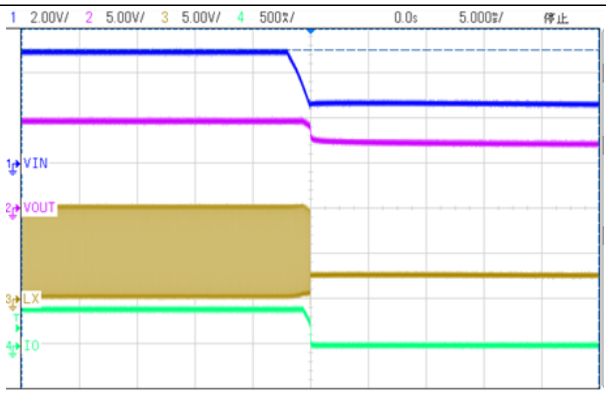


Figure 14.2.b V_{IN}=5V, I_{OUT}=400mA, 3pcs LED Series

Figure 13.3 Switching Waveforms

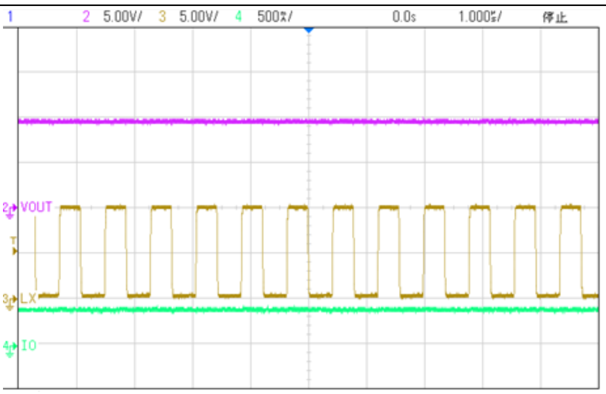


Figure 14.3.a V_{IN}=5V, I_{OUT}=400mA, 3pcs LED Series
CCM Mode

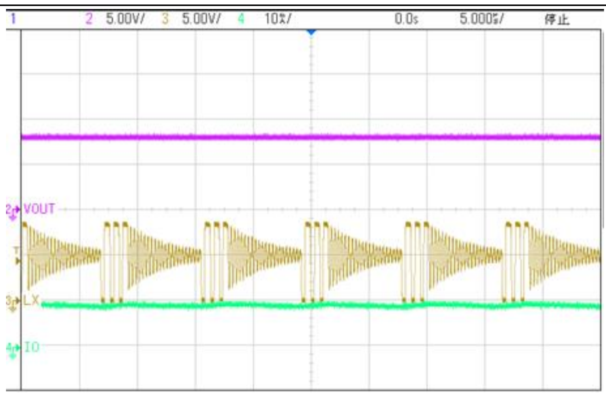


Figure 14.3.b V_{IN}=5V, I_{OUT}=10mA, 3pcs LED Series
Pulse Skip Mode

V

Figure 14.1 OTP Waveforms

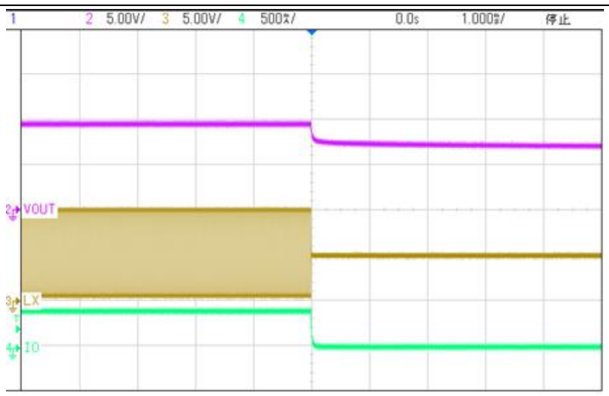


Figure 15.1.a V_{IN}=5V, I_{OUT}=400mA, 3pcs LED Series

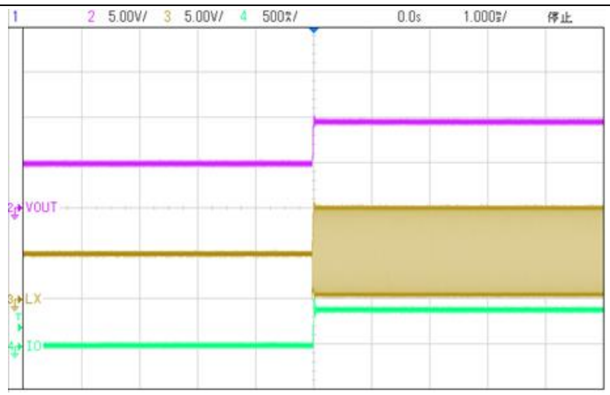


Figure 15.1.b V_{IN}=5V, I_{OUT}=400mA, 3pcs LED Series

Figure 14.2 PWM Dimming Transient

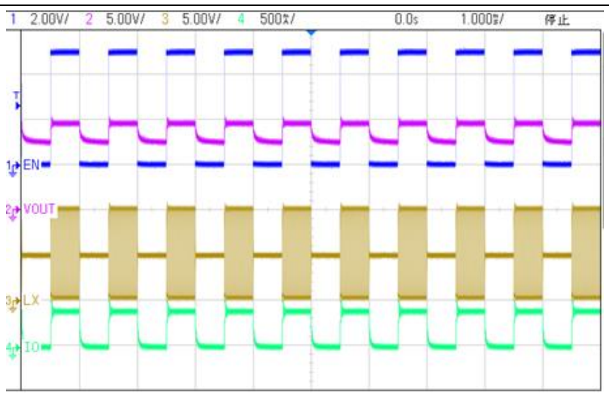


Figure 15.2.a LGS63030, V_{IN}=5V, I_{OUT}=400mA, 3pcs LED Series

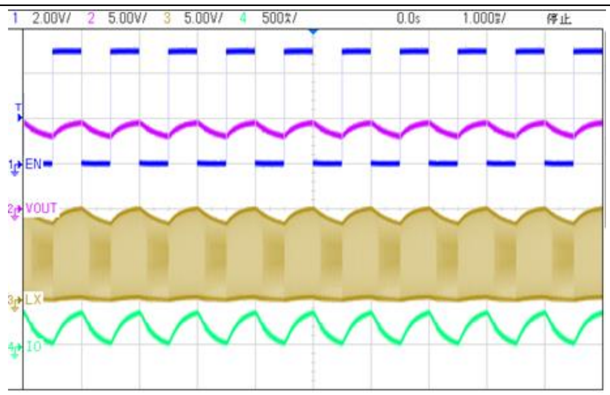


Figure 15.2.b LGS63032, V_{IN}=5V, I_{OUT}=400mA, 3pcs LED Series

Figure 14.3 OVP Waveforms

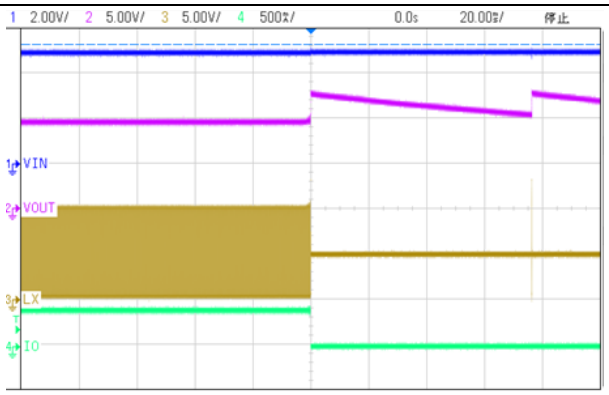


Figure 15.3.a V_{IN}=5V, I_{OUT}=400mA, 3pcs LED Series,

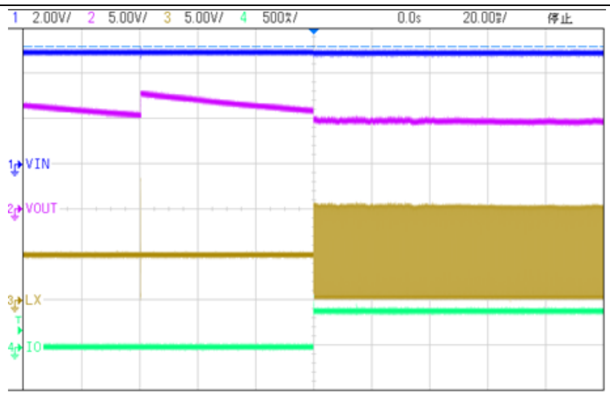


Figure 15.3.b V_{IN}=5V, I_{OUT}=400mA, 3pcs LED Series,

Application Information: Reference Layout

Summary

The high integration of LGS6303X makes PCB board layout very simple and easy. Poor layout can affect the performance of LGS6303X, causing electromagnetic interference (EMI), poor electromagnetic compatibility (EMC), ground jumping, and voltage loss, which in turn affects voltage regulation and stability. In order to optimize its electrical and thermal performance, the following rules should be applied to achieve good PCB layout and wiring, ensuring optimal performance:

- The high-frequency ceramic input capacitor CIN must be placed as close as possible to the VIN and GND pins to minimize high-frequency noise.
- It is necessary to reduce the PCB copper plating area related to SW pins to avoid potential noise interference issues.
- For high current paths, a larger PCB copper-clad area should be used, including the GND pin. This helps to minimize PCB conduction losses and thermal stress to the greatest extent possible.
- To minimize via conduction loss and reduce module thermal stress, multiple vias should be used to achieve interconnection between the top layer and other power layers or strata.
- The impedance of the FB pin is relatively high, and the lead trajectory should be as short as possible and kept away from high noise LX nodes or shielded.
- The bottom heat dissipation pads of ESOP8 packaged chips with through-hole openings help improve the efficiency of chip heat dissipation.

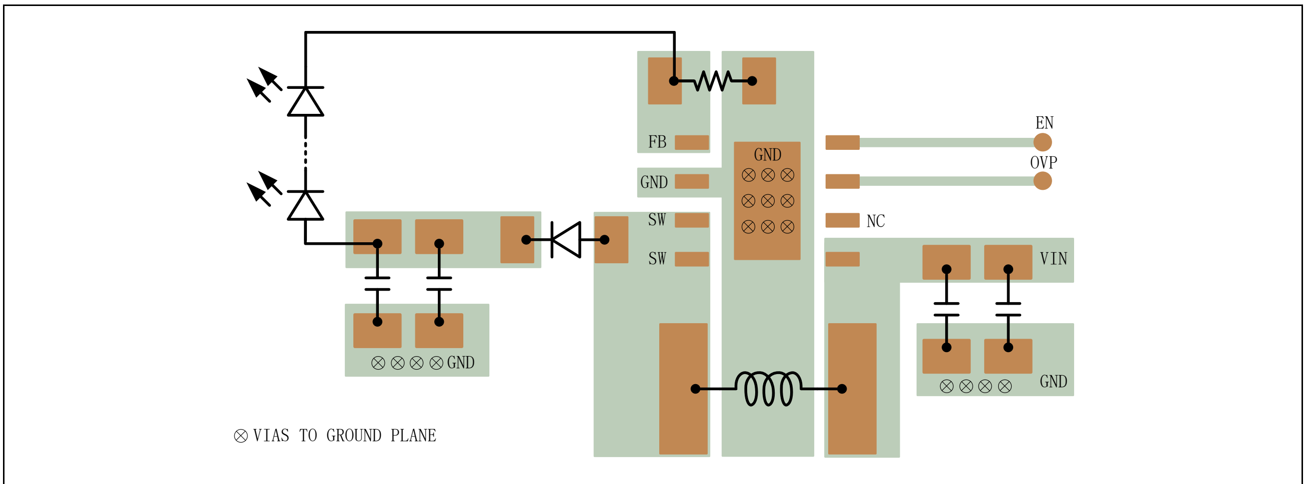


Figure 15.1 Typical Application PCB Reference Layout of Boost ESOP8 Package

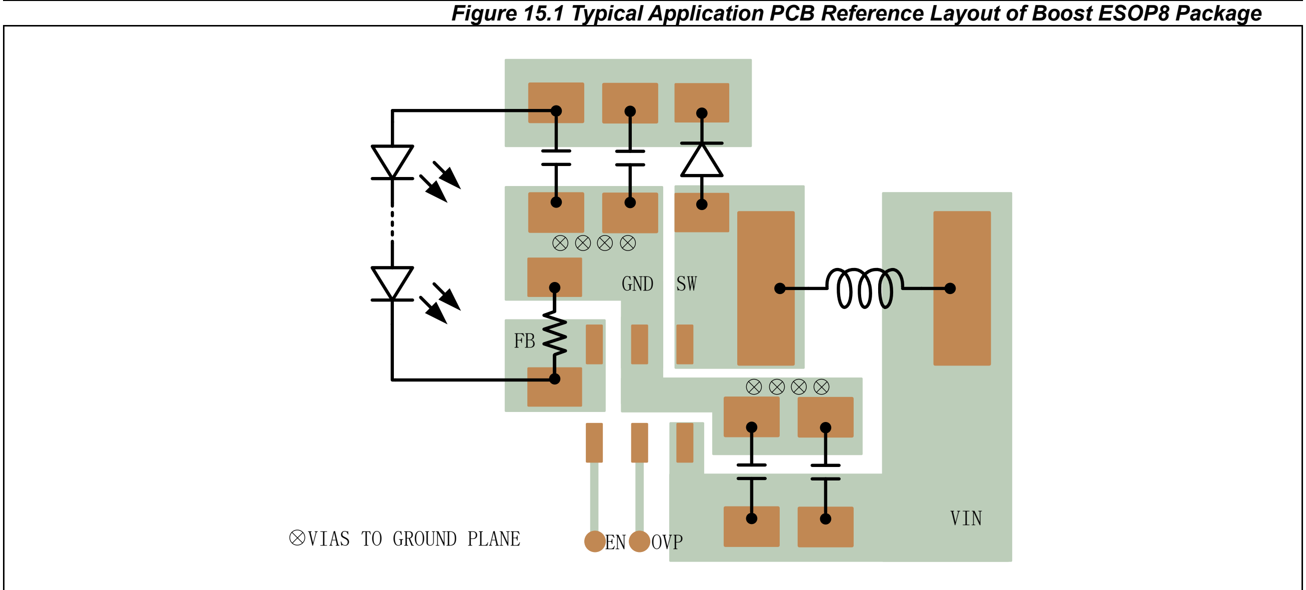
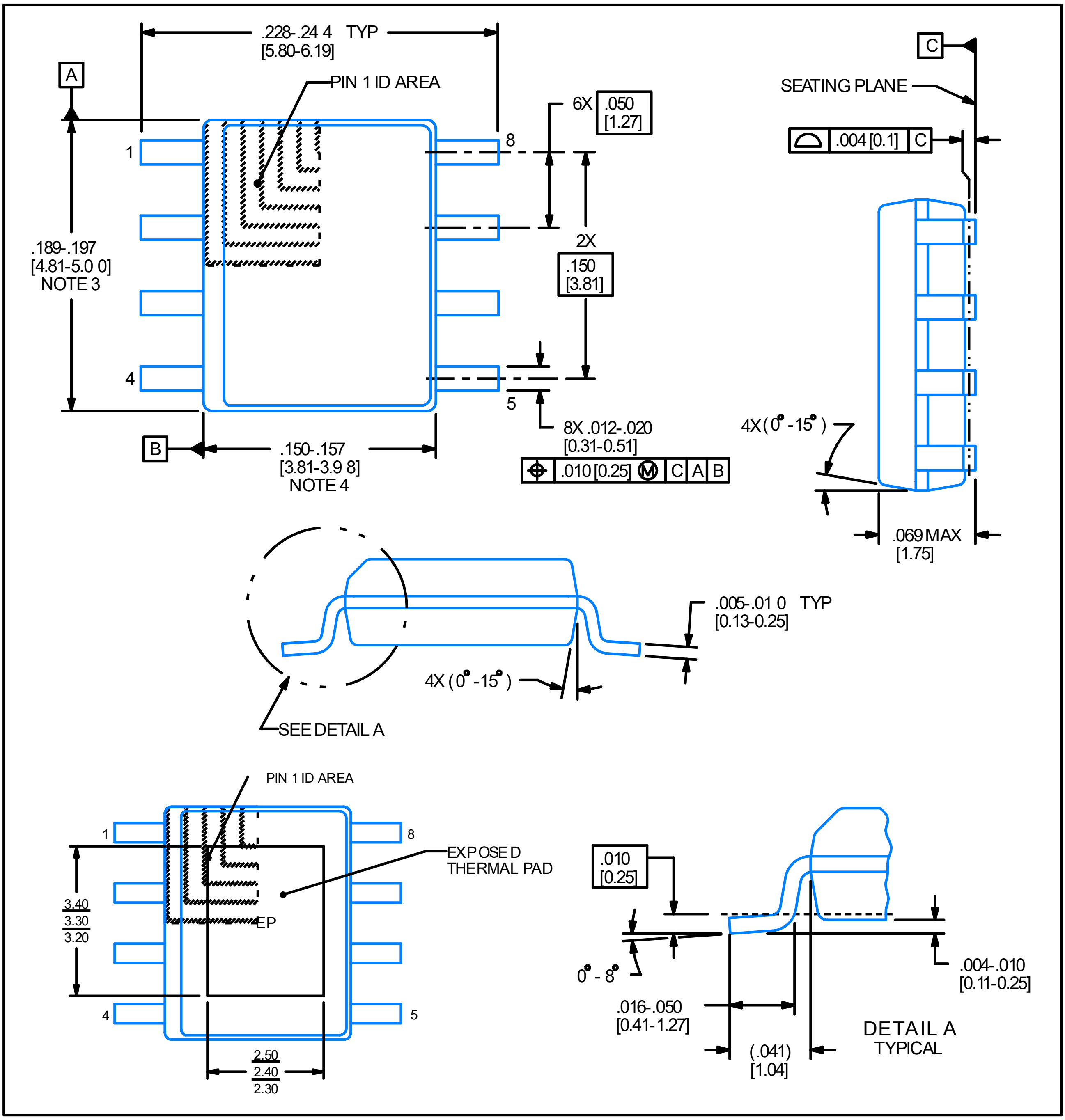


Figure 15.2 Typical Application PCB Reference Layout of Boost SOT23-6 Package

Package Description (ESOP8)

8-pin plastic encapsulated SOIC with bottom EPAD



Note:

(1) All data units are in millimeters, and any dimensions in parentheses are for reference only. The dimensions and tolerances comply with ASME Y14.5M

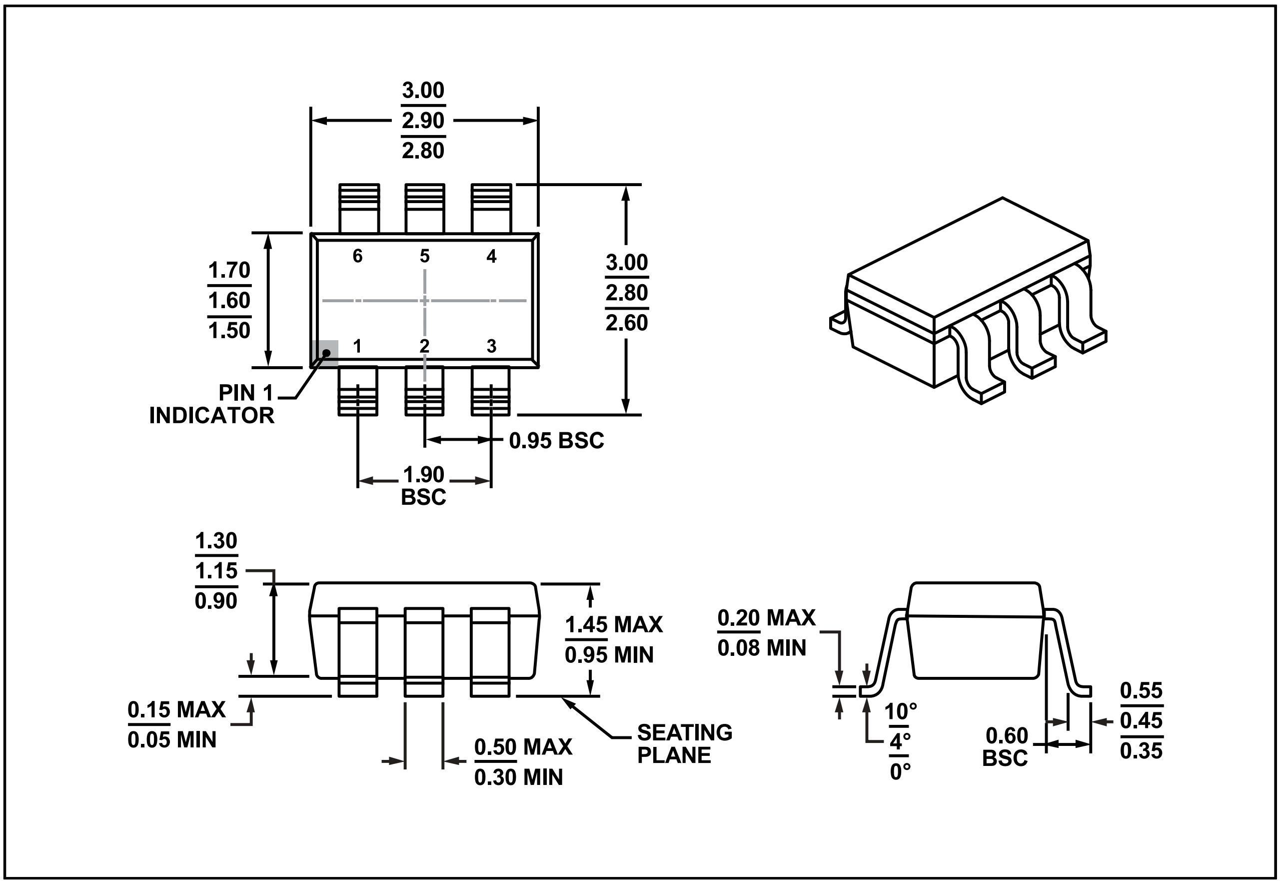
(2) This image is subject to change without prior notice.

(3) This size does not include mold burrs, protrusions, or nozzle burrs. The burrs or protrusions on each side of the mold shall not exceed 0.15 millimeters.

(4) This size does not include mold burrs, and the burrs or protrusions on each side of the mold should not exceed 0.25 millimeters.

Package Description (SOT23-6)

1.45mm height 6-pin SOT-23 plastic encapsulated SOIC



Note:

(1) All data units are in millimeters, and any dimensions in parentheses are for reference only. The dimensions and tolerances comply with ASME Y14.5M

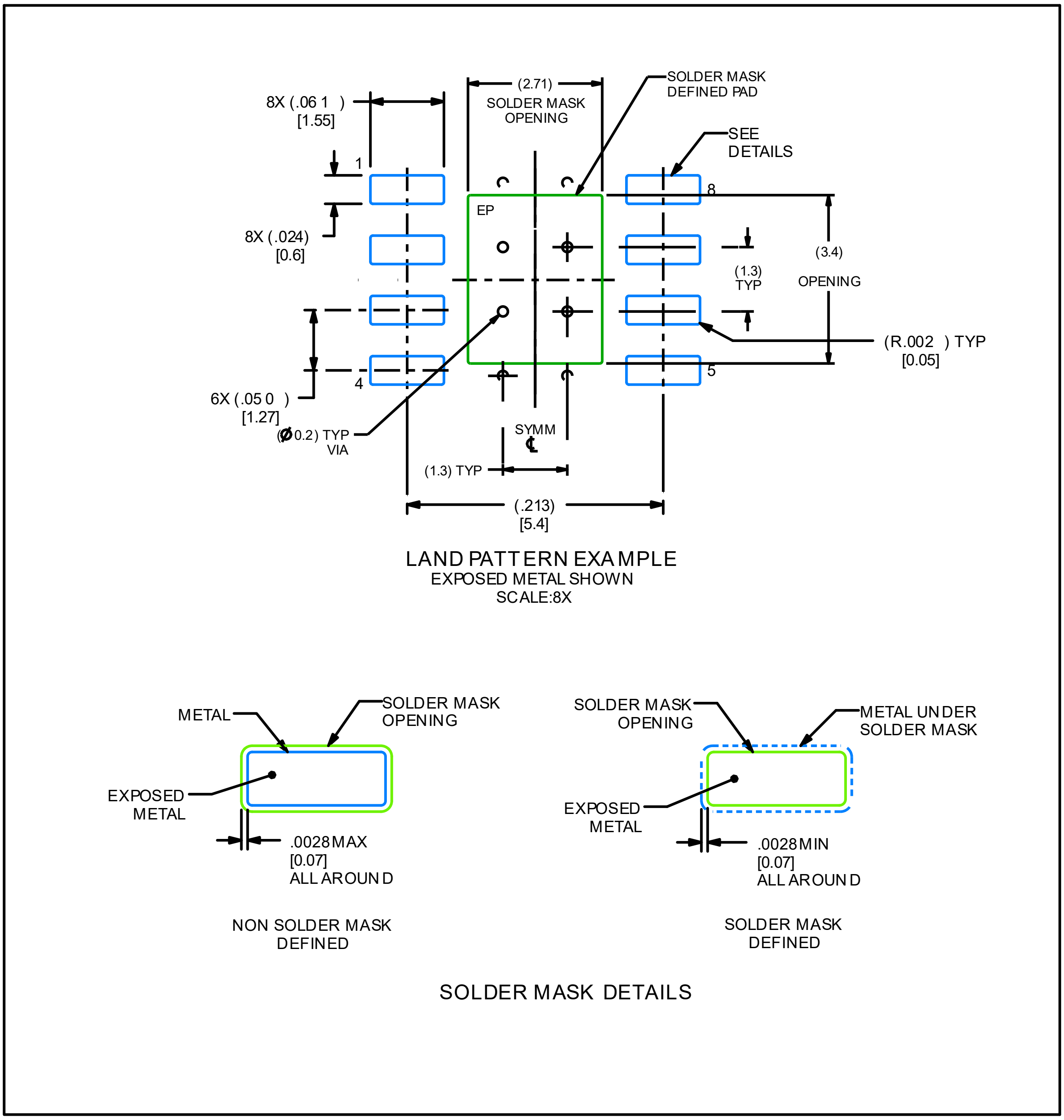
(2) This image is subject to change without prior notice.

(3) This size does not include mold burrs, protrusions, or nozzle burrs. The burrs or protrusions on each side of the mold shall not exceed 0.15 millimeters.

(4) This size does not include mold burrs, and the burrs or protrusions on each side of the mold should not exceed 0.25 millimeters.

Example of Device Packaging Pad Layout (ESOP8)

8-pin plastic encapsulated SOIC with bottom EPAD



Note:

(1) Based on IPC-7351, which relies on proven mathematical algorithms and comprehensively considers manufacturing, assembly, and component tolerances, the solder pad pattern is accurately calculated.

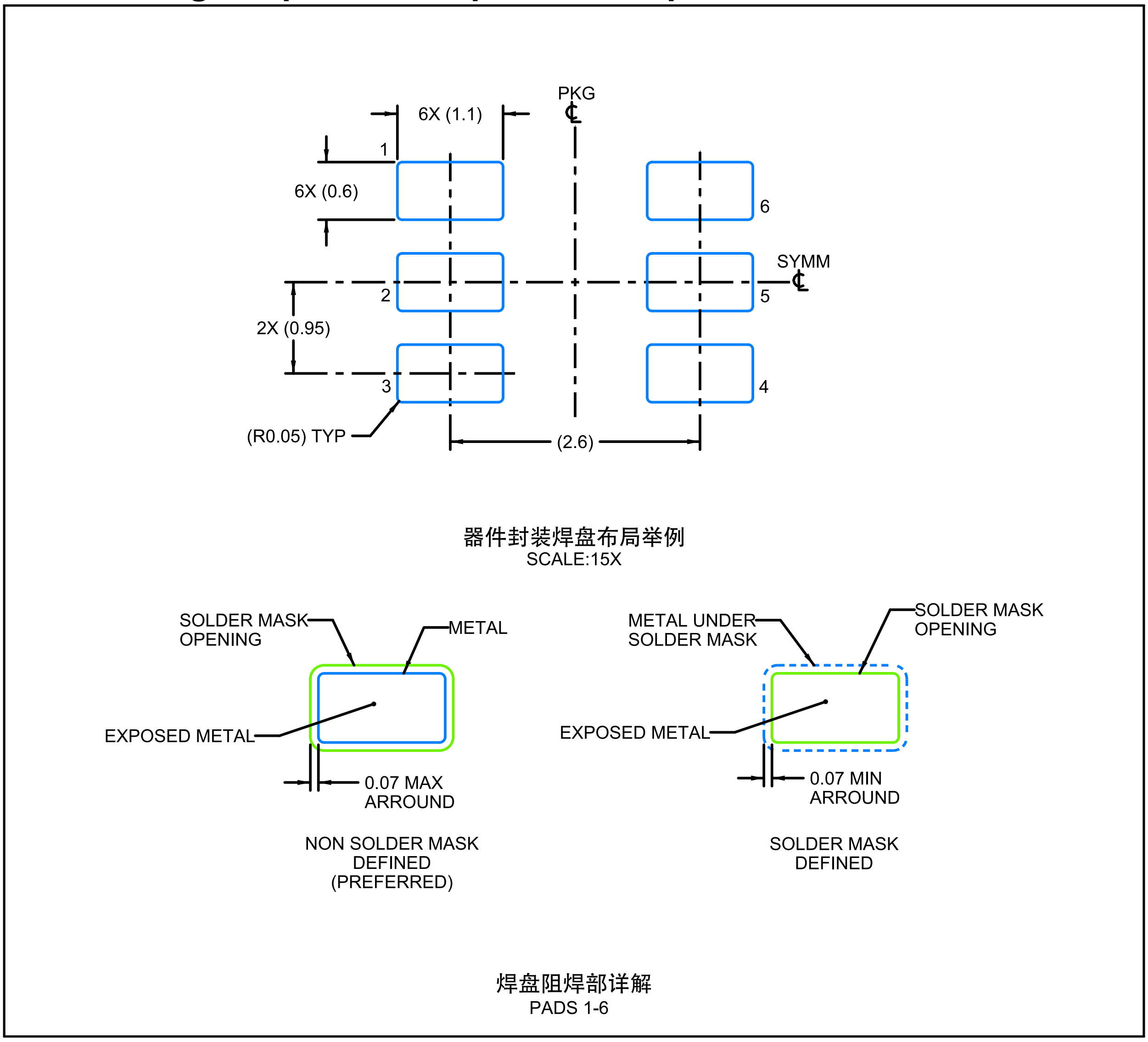
(2) The tolerance of the solder mask between and around signal pads may vary depending on the manufacturing of the circuit board.

(3) The size of the metal pad may vary due to creepage requirements.

(4) Through holes are optional, depending on the application, please refer to the device data sheet. If via holes are used, please refer to the via hole positions shown in this view. Suggest filling or covering the via under the solder pad with solder paste.

Example of Device Packaging Pad Layout (SOT23-6)

1.45mm height 6-pin SOT-23 plastic encapsulated SOIC



Note:

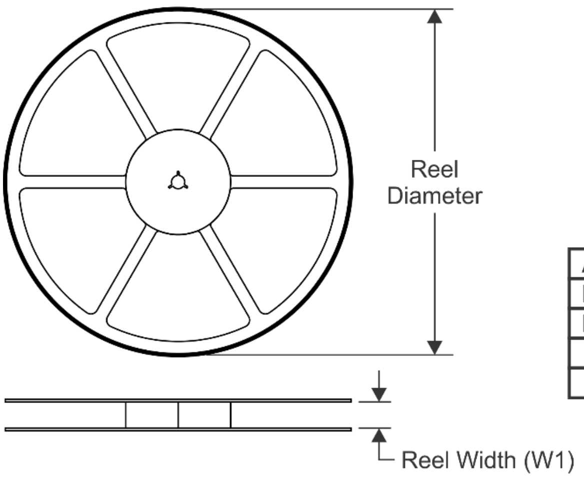
(1) Based on IPC-7351, which relies on proven mathematical algorithms and comprehensively considers manufacturing, assembly, and component tolerances, the solder pad pattern is accurately calculated.

(2) The tolerance of the solder mask between and around signal pads may vary depending on the manufacturing of the circuit board.

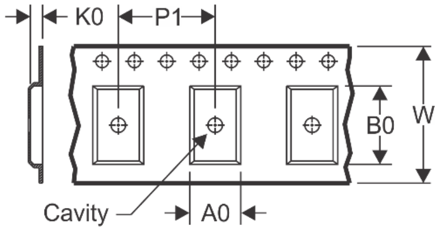
(3) The size of the metal pad may vary due to creepage requirements.

TAPE AND REEL INFORMALEGEND-SION

REEL DIMENSIONS

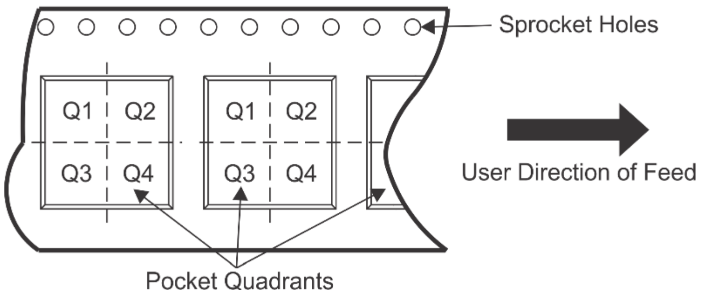


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*ALL dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Width W1(mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LGS63030	SOT23-6	B6	6	3000	180.0	8.4	3.2	3.2	1.4	1.4	Q3
LGS63032	SOT23-6	B6	6	3000	180.0	8.4	3.2	3.2	1.4	1.4	Q3
LGS63030	ESOP8L	EP	8	4000	330	6.5	5.3	2.1	8	12	Q1

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