



钜地半导体
Tudi Semiconductor

Product Specification

TUDI-ICL7662

Switched-Capacitor Voltage Converters With Regulators

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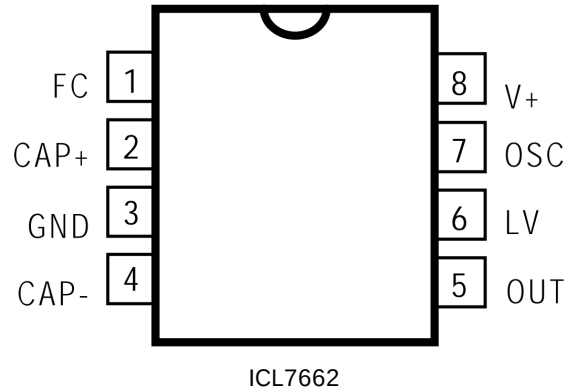
**semiconductor device
manufacturer**

- Design
- research and development
- production
- and sales



Features

- Output Current, 100 mA
- Low Loss, 1.1 V at 100 mA
- Operating Range, 3.5 V to 15 V
- Reference and Error Amplifier for Regulation
- External Shutdown
- External Oscillator Synchronization
- Devices Can Be Paralleled



General Description

The ICL7662 device is a bipolar, switched-capacitor voltage converter with regulator. It provides higher output current and significantly lower voltage losses than previously available converters. An adaptive-switch drive scheme optimizes efficiency over a wide range of output currents. Total voltage drop at 100-mA output current typically is 1.1 V. This applies to the full supply-voltage range of 3.5 V to 15 V. Quiescent current typically is 2.5 mA.

The ICL7662 also provides regulation, a feature previously not available in switched-capacitor voltage converters. By adding an external resistive divider, a regulated output can be obtained. This output is regulated against changes in both input voltage and output current. The ICL7662 can also shut down by grounding the feedback terminal. Supply current in shutdown typically is 100 μ A.

The internal oscillator of the ICL7662 runs at a nominal frequency of 25 kHz. The oscillator terminal can be used to adjust the switching frequency or to externally synchronize the ICL7662. The ICL7662C is characterized for operation over a free-air temperature range of 0 °C to 70 °C. The ICL7662I is characterized for operation over a free-air temperature range of 40 °C to 85 °C.

Applications

- Industrial Communications (RS232)
- Data Acquisition Supply
- Voltage Inverters
- Voltage Regulators
- Negative Voltage Doublers
- Positive Voltage Doublers

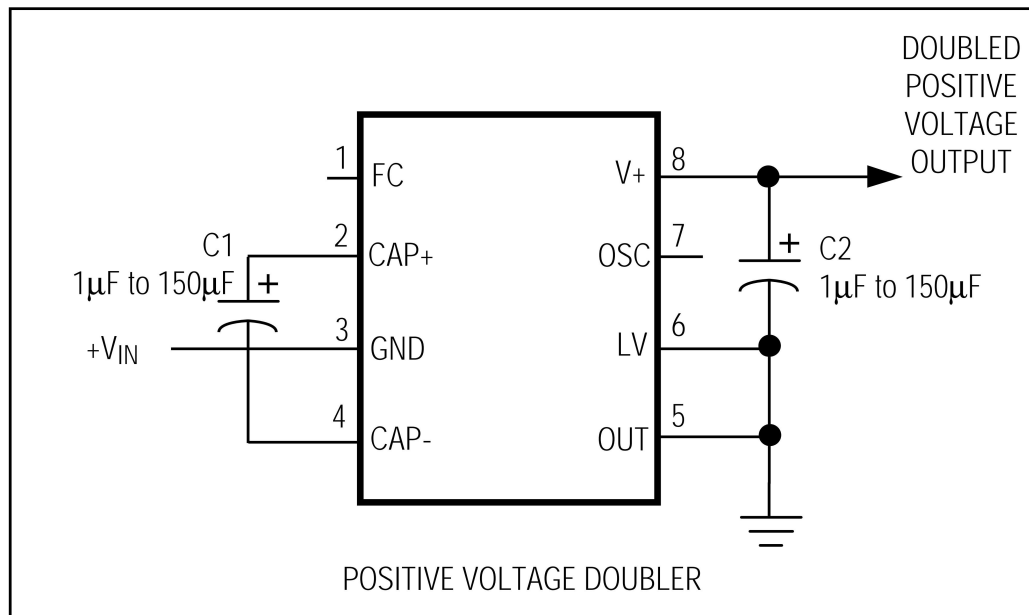
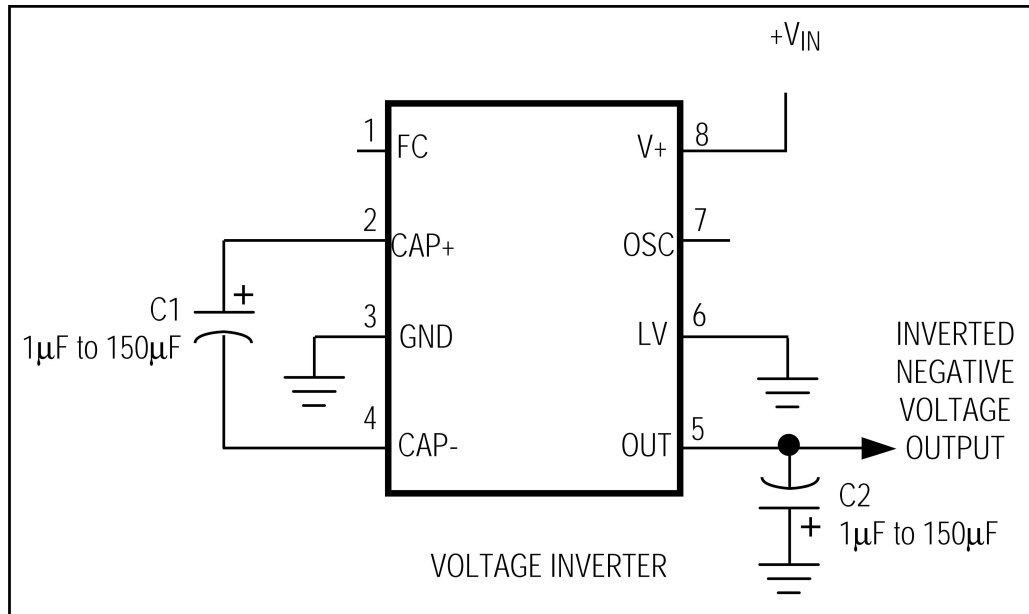


Pin Description

PIN	NAME	FUNCTION	
		INVERTER	DOUBLER
1	FC	Frequency Control for internal oscillator, FC=open, $f_{osc} = 10\text{kHz typ}$; FC=V+, $f_{osc} = 80\text{kHz typ}(40\text{kHz min})$, FC has no effect when OSC pin is driven externally.	Same as Inverter
2	CAP+	Charge-Pump Capacitor, Positive Terminal	Same as Inverter
3	GND	Power-Supply Ground Input	Power-Supply Positive Voltage Input
4	CAP-	Charge-Pump Capacitor, Negative Terminal	Same as Inverter
5	OUT	Output, Negative Voltage	Power-Supply Ground Input
6	LV	Low-Voltage Operation Input. Tie LV to GND when input voltage is less than 3V. Above 3V, LV may be connected to GND or left open; when overdriving OSC, LV must be connected to GND.	LV must be tied to OUT for all input voltages.
7	OSC	Oscillator Control Input. OSC is connected to an internal 15pF capacitor. An external capacitor can be added to slow the oscillator. Take care to minimize stray capacitance. An external oscillator may also be connected to overdrive OSC.	Same as Inverter; however, do not overdrive OSC in voltage-doubling mode.
8	V+	Power-Supply Positive Voltage Input	Positive Voltage Output



Typical Operating Circuits





ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V+ to GND, or GND to OUT)	15V
LV Input Voltage	(OUT - 0.3V) to (V+ + 0.3V)
FC and OSC Input Voltages	The least negative of (OUT - 0.3V) or (V+ - 6V) to (V+ + 0.3V)
OUT and V+ Continuous Output Current	120mA
Output Short-Circuit Duration to GND (Note 1)	1sec
Continuous Power Dissipation (T_A = +70°C)	
Plastic DIP (derate 9.09mW/°C above + 70°C)	727mW
SO (derate 5.88mW/°C above +70°C)	471mW
CERDIP (derate 8.00mW/°C above +70°C)	640mW
Operating Temperature Ranges	
7662C	0°C to +70°C
7662E	-40°C to +85°C
Storage Temperature Range	-65°C to +160°C
Lead Temperature (soldering, 10sec)	+300°C

NOTE 1. OUT may be shorted to GND for 1sec without damage, but shorting OUT to V+ may damage the device and should be avoided. Also, for temperatures above +85°C, OUT must not be shorted to GND or V+, even instantaneously, or device damage may result.

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability



ELECTRICAL CHARACTERISTICS

(V+ = 5V, C1 = C2 = 150 μ F, test circuit of Figure 1, FC = open, TA = TMIN to TMAX, unless otherwise noted.) (Note 2)

PARAMETER			MIN	TYP	MAX	UNITS
Operating Supply Voltage	RL=1k Ω	Inverter,LV=open	3.0		15	V
		Inverter,LV=GND	1.5		15	
		Doubler,LV=OUT	2.5		15	
Supply Current	No load	FC=open,LV=open		0.12	0.5	mA
		FC=V+,LV=open		1	3	
Output Current	TA $\leq$ +85 $^{\circ}$ C,OUT more negative than -4V		100			mA
	TA>+85 $^{\circ}$ C,OUT more negative than-3.8V		100			
Output Resistance(Note 3)	IL=100mA	TA $\leq$ +85 $^{\circ}$ C,C1=C2=10 μ F,FC=V+(Note 4)			15	Ω
		TA $\leq$ +85 $^{\circ}$ C,C1=C2=150 μ F		6.5	10.0	
		TA $\leq$ +85 $^{\circ}$ C			12	
Oscillator Frequency	FC=open		5	10		kHz
	FC=V+		40	80		
OSC Input Current	FC=open			± 1		μ A
	FC=V+			± 8		
Power Efficiency	RL=1k Ω connected between V+and OUT		96	98		%
	RL=500 Ω connected between OUT and GND		92	96		
	IL=100mA to GND			88		
Voltage-Conversion Efficiency	No load		99.00	99.96		%

Note 2: In the test circuit, capacitors C1 and C2 are 150 μ F, 0.2 Ω maximum ESR, aluminum electrolytics. Capacitors with higher ESR may reduce output voltage and efficiency. See Capacitor Selection section.

Note 3: Specified output resistance is a combination of internal switch resistance and capacitor ESR. See Capacitor Selection section.

Note 4: The ESR of C1 = C2 $\leq$ 0.5 Ω . Guaranteed by correlation, not production tested.



Typical Operating Characteristics

All curves are generated using the test circuit of Figure 1 with $V_+ = +5V$, $LV = GND$, $FC = open$, and $T_A = +25^\circ C$, unless otherwise noted. The charge-pump frequency is one-half the oscillator frequency. Test results are also valid for doubler mode with $GND = +5V$, $LV = OUT$, and $OUT = 0V$, unless otherwise noted; however, the input voltage is restricted to $+2.5V$ to $+5.5V$.

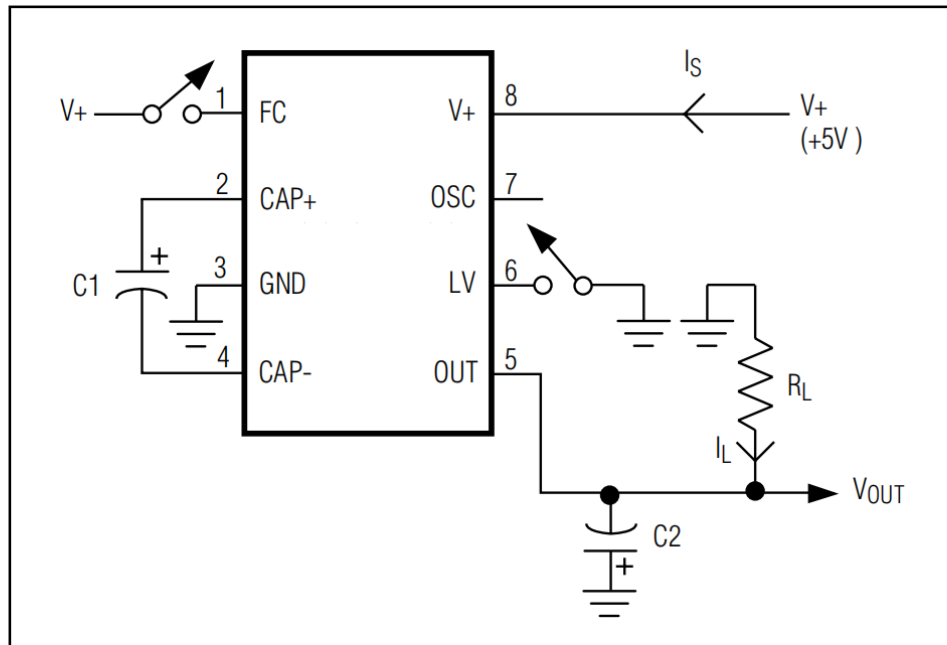


Figure 1. ICL7662 Test Circuit

Detailed Description

The ICL7662 capacitive charge-pump circuit either inverts or doubles the input voltage (see Typical Operating Circuits). For highest performance, low effective series resistance (ESR) capacitors should be used. See Capacitor Selection section for more details.

When using the inverting mode with a supply voltage less than 3V, LV must be connected to GND. This bypasses the internal regulator circuitry and provides best performance in low-voltage applications. When using the inverter mode with a supply voltage above 3V, LV may be connected to GND or left open. The part is typically operated with LV grounded, but since LV may be left open, the substitution of the ICL7662 for the ICL7660 is simplified. LV must be grounded when over-driving OSC (see Changing Oscillator Frequency section). Connect LV to OUT (for any supply voltage) when using the doubling mode.



Applications Information

Negative Voltage Converter

The most common application of the ICL7662 is as a charge-pump voltage inverter. The operating circuit uses only two external capacitors, C1 and C2 (see Typical Operating Circuits). Even though its output is not actively regulated, the ICL7662 is very insensitive to load current changes. A typical output source resistance of 6.5Ω means that with an input of +5V the output voltage is -5V under light load, and decreases only to -4.35V with a load of 100mA. Output source resistance vs. temperature and supply voltage are shown in the Typical Operating Characteristics graphs.

Output ripple voltage is calculated by noting the output current supplied is solely from capacitor C2 during one-half of the charge-pump cycle. This introduces a peak-to-peak ripple of:

$$V_{\text{RIPPLE}} = \frac{I_{\text{OUT}}}{2(f_{\text{PUMP}})(C2)} + I_{\text{OUT}}(\text{ESR}_{C2})$$

For a nominal f_{PUMP} of 5kHz (one-half the nominal 10kHz oscillator frequency) and $C2 = 150\mu\text{F}$ with an ESR of 0.2Ω , ripple is approximately 90mV with a 100mA load current. If C2 is raised to $390\mu\text{F}$, the ripple drops to 45mV.

Positive Voltage Doubler

The ICL7662 operates in the voltage-doubling mode as shown in the Typical Operating Circuit. The no-load output is $2 \times V_{\text{IN}}$.



Changing Oscillator Frequency

Four modes control the ICL7662 ' s clock frequency, as listed below:

FC	OSC	Oscillator Frequency
Open	Open	10kHz
FC=V+	Open	80kHz
Open or FC = V+	External Capacitor	See Typical Operating Characteristics
Open	External Clock	External Clock Frequency

When FC and OSC are unconnected (open), the oscillator runs at 10kHz typically. When FC is connected to V+, the charge and discharge current at OSC changes from 1.0 μ A to 8.0 μ A, thus increasing the oscillator frequency eight times. In the third mode, the oscillator frequency is lowered by connecting a capacitor between OSC and GND. FC can still multiply the frequency by eight times in this mode, but for a lower range of frequencies (see Typical Operating Characteristics). In the inverter mode, OSC may also be overdriven by an external clock source that swings within 100mV of V+ and GND. Any standard CMOS logic output is suitable for driving OSC. When OSC is overdriven, FC has no effect. Also, LV must be grounded when overdriving OSC. Do not overdrive OSC in voltage-doubling mode.

Note: In all modes, the frequency of the signal appearing at CAP+ and CAP- is one-half that of the oscillator. Also, an undesirable effect of lowering the oscillator frequency is that the effective output resistance of the charge pump increases. This can be compensated by increasing the value of the charge-pump capacitors (see Capacitor Selection section and Typical Operating Characteristics).

In some applications, the 5kHz output ripple frequency may be low enough to interfere with other circuitry. If desired, the oscillator frequency can then be increased through use of the FC pin or an external oscillator as described above. The output ripple frequency is one-half the selected oscillator frequency. Increasing the clock frequency increases the ICL7662 ' s quiescent current, but also allows smaller capacitance values to be used for C1 and C2.



Capacitor Selection

Three factors (in addition to load current) affect the ICL7662 output voltage drop from its ideal value:

- 1) ICL7662 output resistance
- 2) Pump (C1) and reservoir (C2) capacitor ESRs
- 3) C1 and C2 capacitance

The voltage drop caused by ICL7662 output resistance is the load current times the output resistance. Similarly, the loss in C2 is the load current times C2 ' s ESR. The loss in C1, however, is larger because it handles currents that are greater than the load current during charge-pump operation. The voltage drop due to C1 is therefore about four times C1 ' s ESR multiplied by the load current. Consequently, a low (or high) ESR capacitor has a much greater impact on performance for C1 than for C2.

Generally, as the pump frequency of the ICL7662 increases, the capacitance values required to maintain comparable ripple and output resistance diminish pro-portionately. The curves of Figure 2 show the total circuit output resistance for various capacitor values (the pump and reservoir capacitors ' values are equal) and oscillator frequencies. These curves assume 0.25 Ω capacitor ESR and a 5.25 Ω ICL7662 output resistance, which is why the flat portion of the curve shows a 6.5 Ω ($R_{O\ ICL7662} + 4 (ESRC1) + ESRC2$) effective output resistance. Note: $R_O = 5.25\Omega$ is used, rather than the typical 6.5 Ω , because the typical specification includes the effect of the ESRs of the capacitors in the test circuit.

In addition to the curves in Figure 2, four bar graphs in the Typical Operating Characteristics show output cur-rent for capacitances ranging from 0.33 μF to 220 μF . Output current is plotted for inputs of 4.5V (5V-10%) and 3.0V (3.3V-10%), and allow for 10% and 20% output droop with each input voltage. As can be seen from the graphs, the ICL7662 6.5 Ω series resistance limits increases in output current vs. capacitance for values much above 47 μF . Larger values may still be useful, however, to reduce ripple.

To reduce the output ripple caused by the charge pump, increase the reservoir capacitor C2 and/or reduce its ESR. Also, the reservoir capacitor must have low ESR if filtering high-frequency noise at the output is important.

Not all manufacturers guarantee capacitor ESR in the range required by the ICL7662. In general, capacitor ESR is inversely proportional to physical size, so larger capaci-tance values and higher voltage ratings tend to reduce ESR.

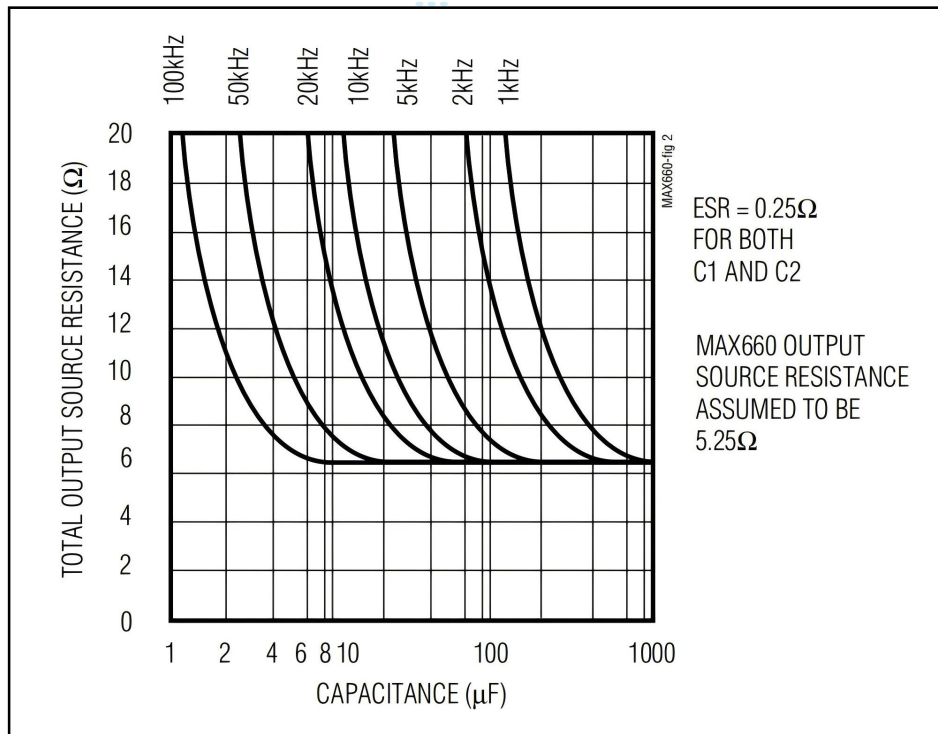


Figure 2. Total Output Source Resistance vs. C1 and C2 Capacitance (C1 = C2)

Cascading Devices

To produce larger negative multiplication of the initial supply voltage, the ICL7662 may be cascaded as shown in Figure 3. The resulting output resistance is approximately equal to the sum of the individual ICL7662 R_{OUT} values. The output voltage, where n is an integer representing the number of devices cascaded, is defined by $V_{OUT} = -n (V_{IN})$.

Paralleling Devices

Paralleling multiple ICL7662 reduces the output resistance. As illustrated in Figure 4, each device requires its own pump capacitor C1, but the reservoir capacitor C2 serves all devices. The value of C2 should be increased by a factor of n, where n is the number of devices. Figure 4 shows the equation for calculating output resistance.

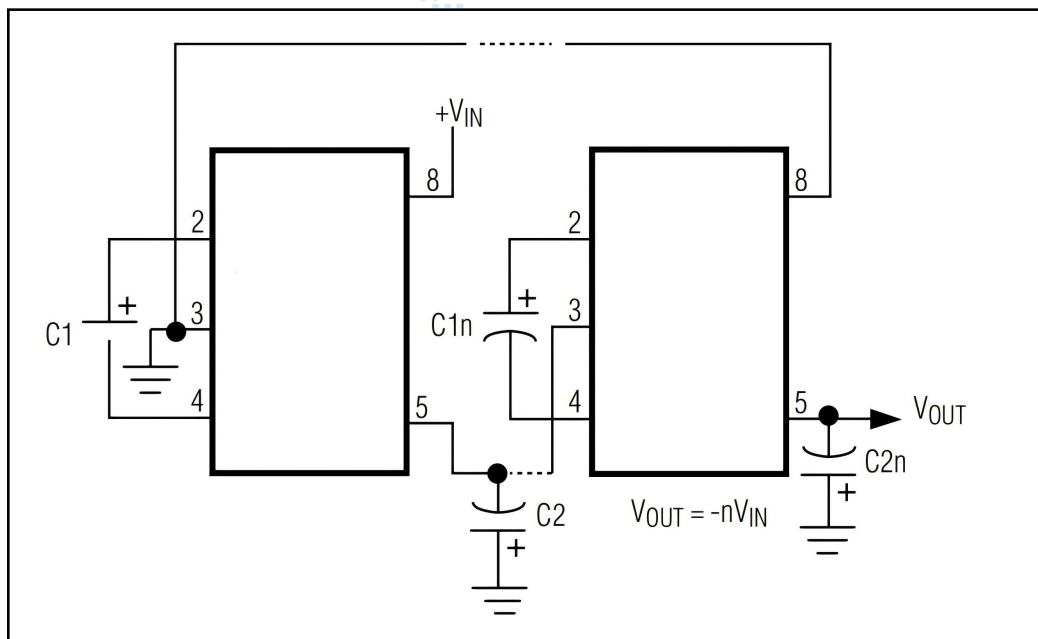


Figure 3. Cascading ICL7662 to Increase Output Voltage

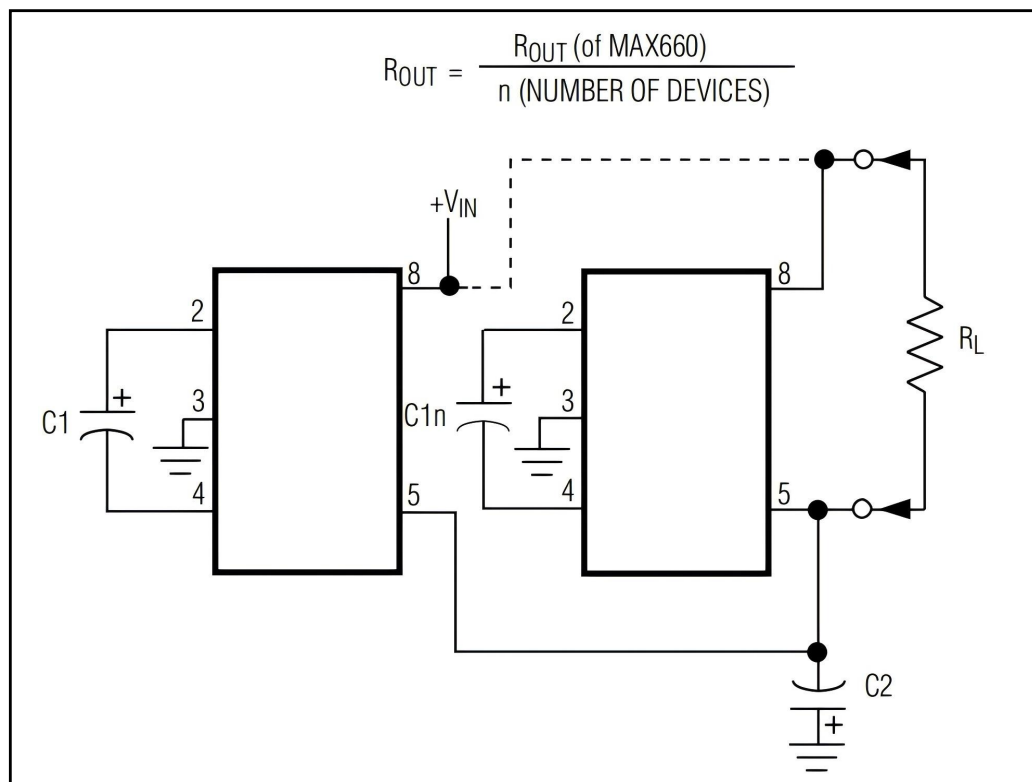


Figure 4. Paralleling ICL7662 to Reduce Output Resistance



Combined Positive Supply Multiplication and Negative Voltage Conversion

This dual function is illustrated in Figure 5. In this circuit, capacitors C1 and C3 perform the pump and reservoir functions respectively for generation of the negative voltage. Capacitors C2 and C4 are respectively pump and reservoir for the multiplied positive voltage. This circuit configuration, however, leads to higher source impedances of the generated supplies. This is due to the finite impedance of the common charge-pump driver.

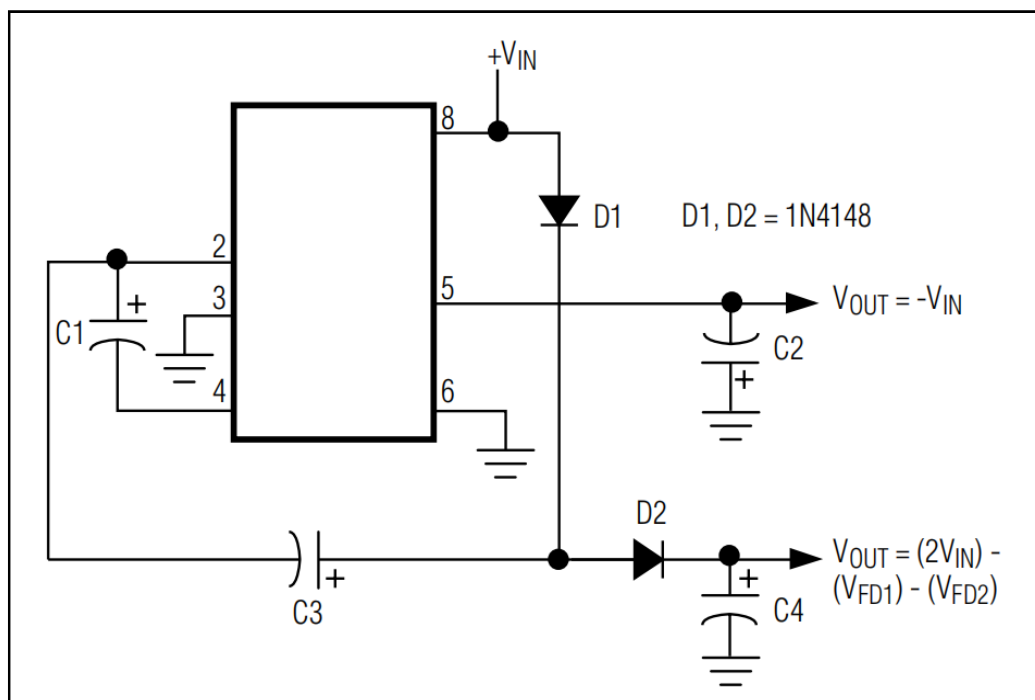


Figure 5. Combined Positive Multiplier and Negative Converter

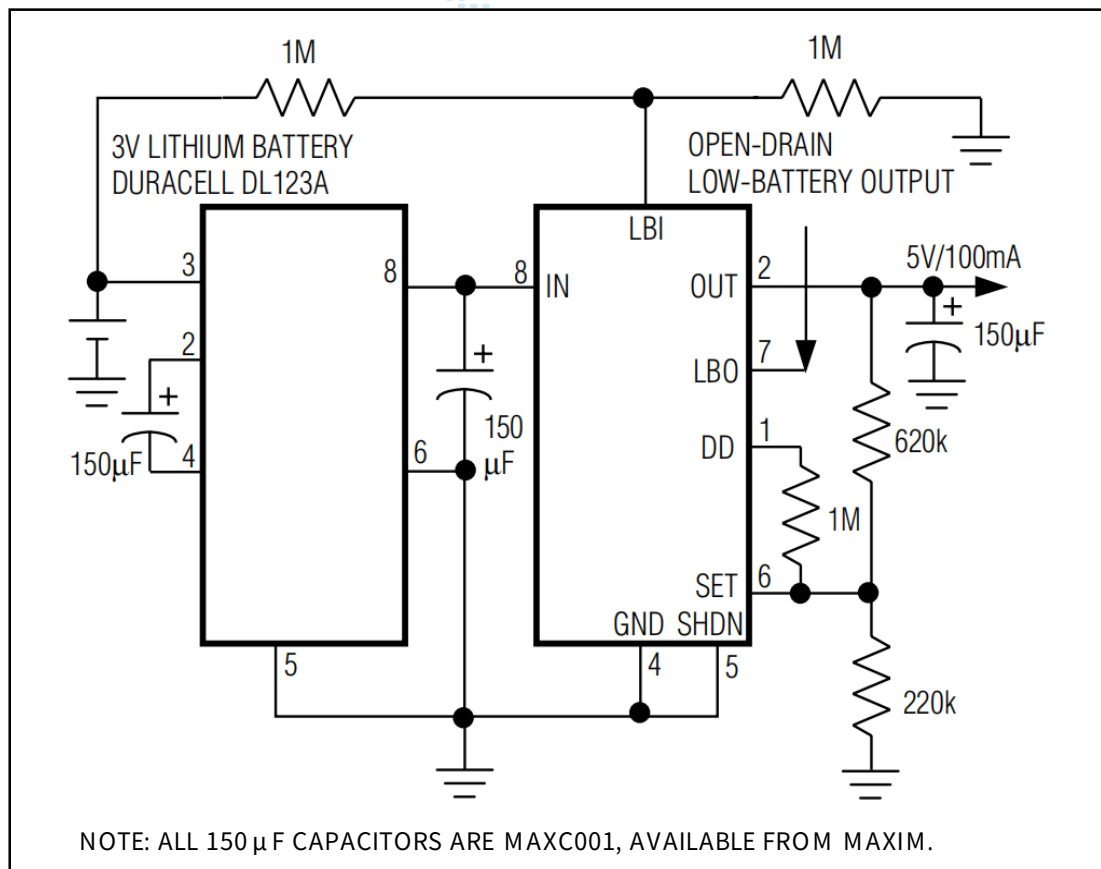
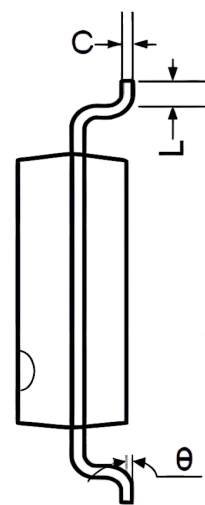
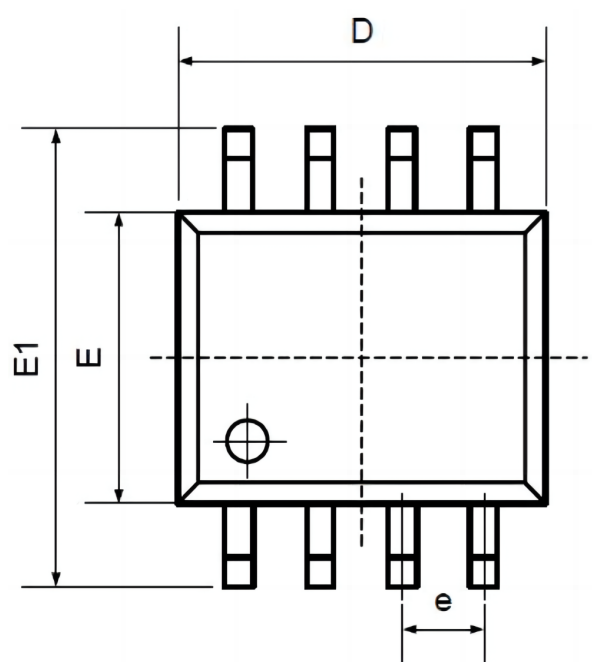


Figure 6. ICL7662 generates a +5V regulated output from a 3V lithium battery and operates for 16 hours with a 40mA load.

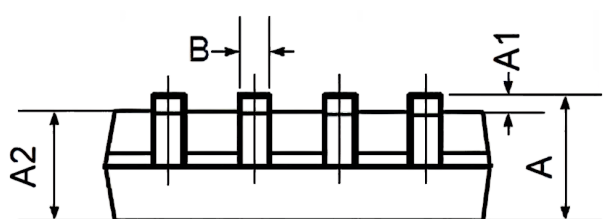
Ordering Information

Order Number	Package	Package Quantity	Marking On The park	Temperature
ICL7662CBA+T-TUDI	SOP8	Tape,Reel,4000	ICL7662CBA	0°C to +70°C
ICL7662CPA-TUDI	DIP8	Tube,50,A box of 2000	ICL7662CPA	
ICL7662EBA+T-TUDI	SOP8	Tape,Reel,4000	ICL7662EBA	-40°C to +85°C
ICL7662EPA-TUDI	DIP8	Tube,50,A box of 2000	ICL7662EPA	

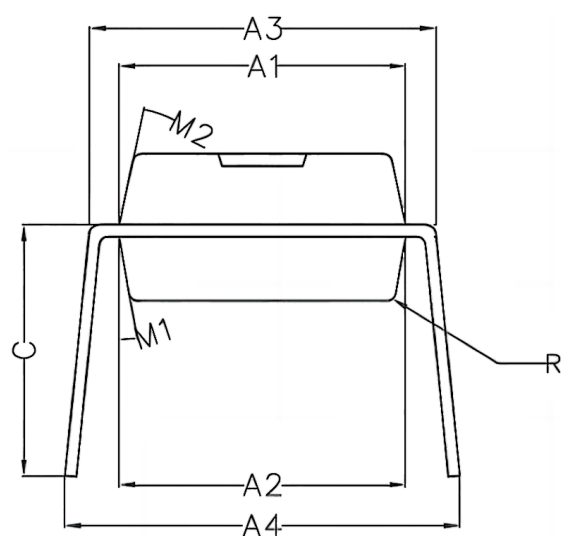
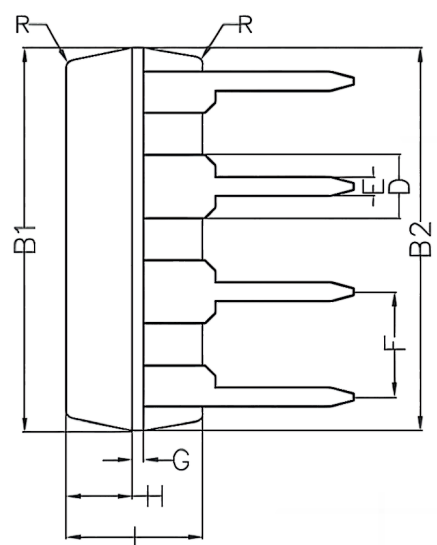
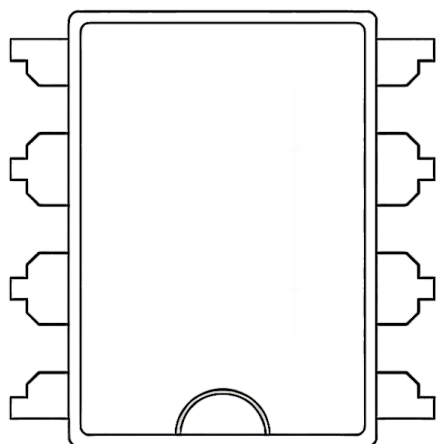
Package SOP8



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
B	0.330	0.510	0.013	0.020
C	0.190	0.250	0.007	0.010
D	4.780	5.000	0.188	0.197
E	3.800	4.000	0.150	0.157
E1	5.800	6.300	0.228	0.248
e	1.270TYP		0.050TYP	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°



Package DIP8



Symbol	Min	Non	Max
A1	6.28	6.33	6.38
A2	6.33	6.38	6.43
A3	7.52	7.62	7.72
A4	7.80	8.40	9.00
B1	9.15	9.20	9.25
B2	9.20	9.25	9.30
C		5.57	
D		1.52	
E	0.43	0.45	0.47
F		2.54	
G		0.25	
H	1.54	1.59	1.64
I	3.22	3.27	3.32
R		0.20	
M1	9°	10°	11°
M2	11°	12°	13°



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