NCN4555

1.8V / 3V SIM Card Power Supply and Level Shifter

The NCN4555 is a level shifter analog circuit designed to translate the voltages between a SIM Card and an external microcontroller or MPU. A built−in LDO−type DC−DC converter makes the NCN4555 useable to drive 1.8 V and 3.0 V SIM card. The device fulfills the ISO7816−3 smart card interface standard as well as GSM 11.11 and related (11.12 and 11.18) and 3G mobile requirements (IMT−2000/3G UICC standard). With the $\overline{\text{STOP}}$ pin a low current shutdown mode can be activated making the battery life longer. The Card power supply voltage (SIM_V_{CC}) is selected using a single pin (MOD_V_{CC}).

Features

- Supports 1.8 V or 3.0 V Operating SIM Card
- The LDO is able to Supply More than 50 mA under 1.8 V and 3.0 V
- Built−in Pullup Resistor for I/O Pin in Both Directions
- All Pins are Fully ESD Protected According to ISO−7816 Specifications – ESD Protection on SIM Pins in Excess of 7 kV (Human Body Model)
- Supports up to More than 5 MHz Clock
- Low−Profile 3x3 QFN−16 Package
- These are Pb−Free Devices*

Typical Applications

- SIM Card Interface Circuit for 2G, 2.5G and 3G Mobile Phones
- Identification Module
- Smart Card Readers
- Wireless PC Cards

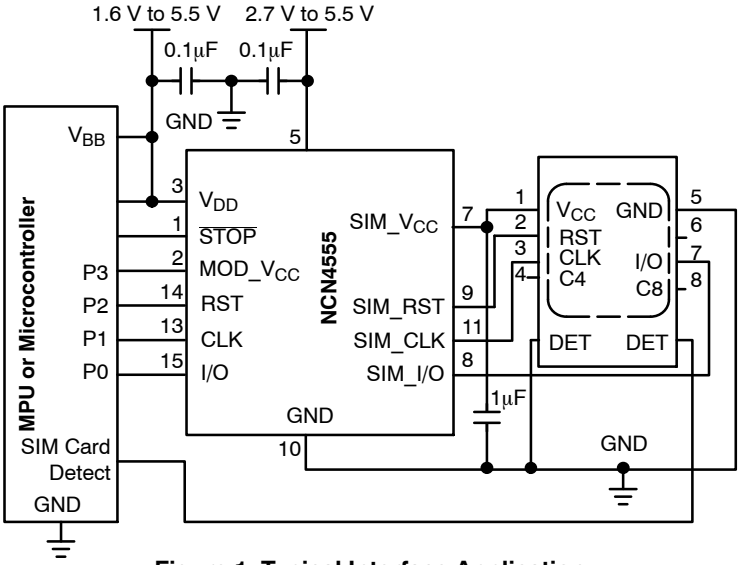


Figure 1. Typical Interface Application

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

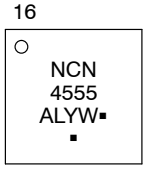
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MARKING DIAGRAM



QFN−16
MN SUFFIX
CASE 488AK



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
NCN4555MNG	QFN−16 (Pb−Free)	123 Units / Rail
NCN4555MNR2G	QFN−16 (Pb−Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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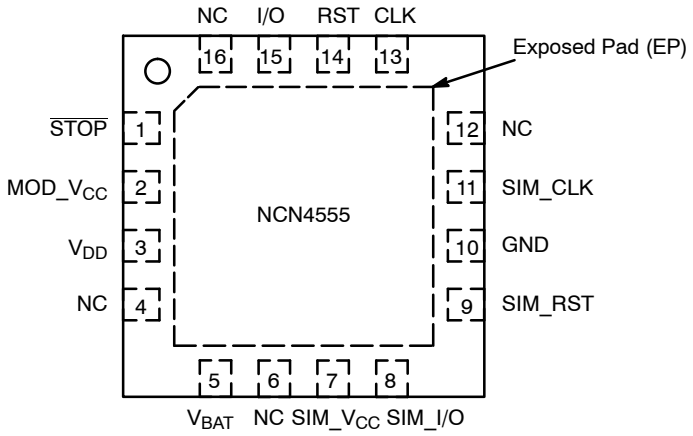


Figure 2. QFN−16 Pinout (Top View)

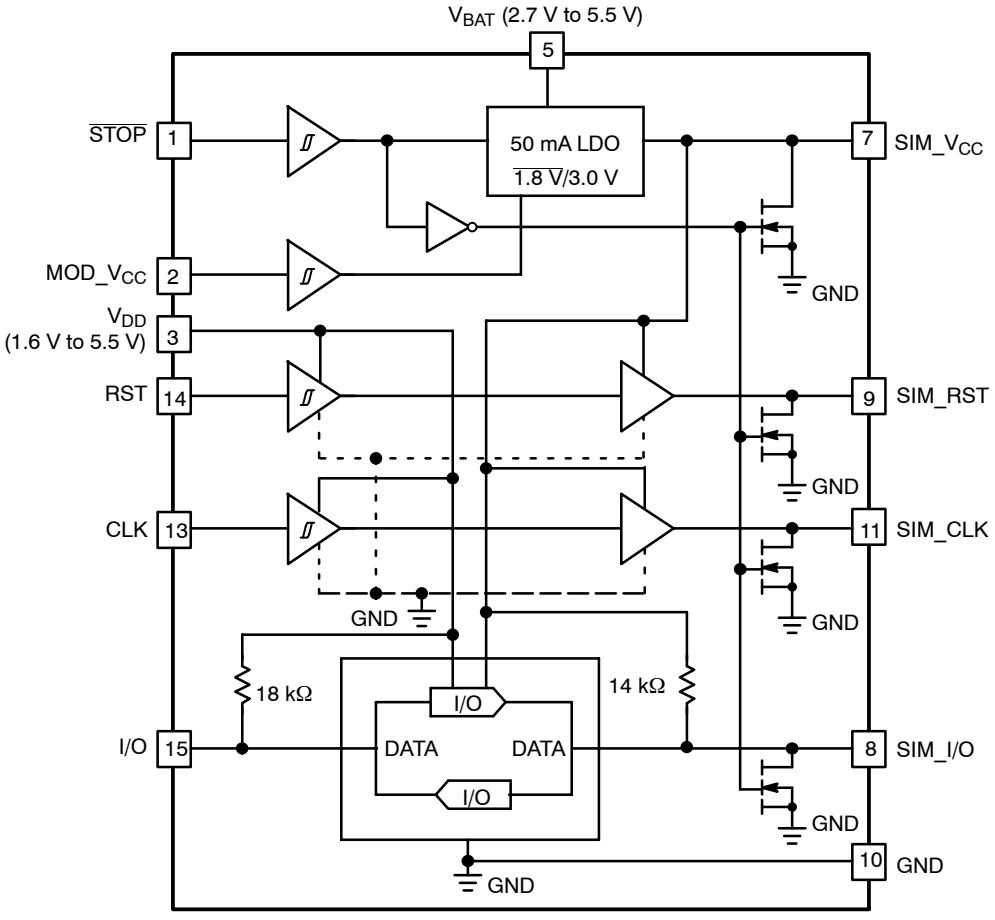


Figure 3. NCN4555 Block Diagram

PIN DESCRIPTIONS

PIN	Name	Type	Description
1	$\overline{\text{STOP}}$	INPUT	Power Down Mode pin: $\overline{\text{STOP}}$ = Low → Low current shutdown mode activated $\overline{\text{STOP}}$ = High → Normal Operation A Low level on this pin resets the SIM interface, switching off the SIM_V_{CC}.
2	MOD_V_{CC}	INPUT	The signal present on this pin programs the SIM_V_{CC} value: MOD_V_{CC} = Low → SIM_V_{CC} = 1.8 V MOD_V_{CC} = High → SIM_V_{CC} = 3 V
3	V_{DD}	POWER	This pin is connected to the system controller power supply. It configures the level shifter input stage to accept the signals coming from the microprocessor. A 0.1 μF capacitor shall be used to bypass the power supply voltage. When V_{DD} is below 1.1 V typical the SIM_V_{CC} is disabled. The NCN4555 comes into a shutdown mode.
4	NC		No Connect
5	V_{BAT}	POWER	DC−DC converter supply input. The input voltage ranges from 2.7V up to 5.5V. This pin has to be bypass by a 0.1 μF capacitor.
6	NC		No Connect
7	SIM_V_{CC}	POWER	This pin is connected to the SIM card power supply pin. An internal LDO converter is programmable by the external MPU to supply either 1.8 V or 3.0 V output voltage. An external 1.0 μF minimum ceramic capacitor recommended must be connected across SIM_V_{CC} and GND. During a normal operation, the SIM_V_{CC} voltage can be set to 1.8 V followed by a 3.0 V value, or can start directly to any of these two values.
8	SIM_I/O	INPUT/ OUTPUT	This pin handles the connection to the serial I/O of the card connector. A bidirectional level translator adapts the serial I/O signal between the card and the micro controller. A 14 kΩ (typical) pullup resistor provides a High impedance state for the SIM card I/O link.
9	SIM_RST	OUTPUT	This pin is connected to the RESET pin of the card connector. A level translator adapts the external Reset (RST) signal to the SIM card.
10	GND	GROUND	This pin is the GROUND reference for the integrated circuit and associated signals. Care must be taken to avoid voltage spikes when the device operates in a normal operation.
11	SIM_CLK	OUTPUT	This pin is connected to the CLOCK pin of the card connector. The CLOCK (CLK) signal comes from the external clock generator, the internal level shifter being used to adapt the voltage defined for the SIM_V_{CC}.
12	NC		No Connect
13	CLK	INPUT	The clock signal, coming from the external controller, must have a Duty Cycle within the Min/Max values defined by the specification (typically 50%). The built−in level shifter translates the input signal to the external SIM card CLK input.
14	RST	INPUT	The RESET signal present at this pin is connected to the SIM card through the internal level shifter which translates the level according to the SIM_V_{CC} programmed value.
15	I/O	INPUT/ OUTPUT	This pin is connected to an external microcontroller or cellular phone management unit. A bidirectional level translator adapts the serial I/O signal between the smart card and the external controller. A built−in constant 18 kΩ (typical) resistor provides a high impedance state when not activated.
16	NC		No Connect

ATTRIBUTES

Characteristics	Values
ESD protection HBM, SIM card pins (7, 8, 9, 10 & 11) (Note 1) HBM, All other pins (Note 1) MM, SIM card pins (7, 8, 9, 10 & 11) (Note 2) MM, All other pins (Note 2) CDM, SIM card pins (7, 8, 9, 10 & 11) (Note 3) CDM , All other pins (Note 3)	 > 7 kV > 2 kV > 600 V > 200 V > 2 kV > 600 V
Moisture sensitivity (Note 4) QFN−16	Level 1
Flammability Rating Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test	

1. Human Body Model, R =1500 Ω, C = 100 pF.
2. Machine Model.
3. CDM, Charged Device Model.
4. For additional information, see Application Note AND8003/D.

MAXIMUM RATINGS (Note 5)

Rating	Symbol	Value	Unit
LDO Power Supply Voltage	V_{BAT}	$-0.5 \le V_{BAT} \le 6$	V
Power Supply from Microcontroller Side	V_{DD}	$-0.5 \le V_{DD} \le 6$	V
External Card Power Supply	SIM_V_{CC}	$-0.5 \le$ SIM_$V_{CC} \le 6$	V
Digital Input Pins	V_{in} I_{in}	$-0.5 \le V_{in} \le V_{DD} + 0.5$ but < 6.0 ±5	V mA
Digital Output Pins	V_{out} I_{out}	$-0.5 \le V_{out} \le V_{DD} + 0.5$ but < 6.0 ±10	V mA
SIM card Output Pins	V_{out} I_{out}	$-0.5 \le V_{out} \le$ SIM_V_{CC} + 0.5 but < 6.0 15 (internally limited)	V mA
QFN−16 Low Profile package Power Dissipation @ T_A = + 85°C Thermal Resistance Junction−to−Air	 P_D $R_{\theta JA}$	 440 90	 mW °C/W
Operating Ambient Temperature Range	T_A	−40 to +85	°C
Operating Junction Temperature Range	T_J	−40 to +125	°C
Maximum Junction Temperature	T_{Jmax}	+125	°C
Storage Temperature Range	T_{stg}	−65 to + 150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

5. Maximum electrical ratings are defined as those values beyond which damage to the device may occur at T_A = +25°C

POWER SUPPLY SECTION (−40°C to +85°C)

Pin	Symbol	Rating	Min	Typ	Max	Unit
5	V_{BAT}	Power Supply	2.7		5.5	V
5	I_{VBAT}	Operating current – I_{CC} = 0 mA (Note 6)		22	30	μA
5	I_{VBAT_SD}	Shutdown current – $\overline{STOP}$= Low (Note 7)			3.0	μA
3	V_{DD}	Operating Voltage	1.6		5.5	V
3	I_{VDD}	Operating Current – f_{CLK} = 1 MHz (Note 8)		7.0	12	μA
3	I_{VDD_SD}	Shutdown Current – $\overline{STOP}$ = Low			1.0	μA
3	V_{DD}	Undervoltage Lockout	0.6		1.5	V
7	SIM_V_{CC}	MOD_V_{CC} = High, V_{BAT} = 3.0 V, I_{SIM_VCC} = 50 mA MOD_V_{CC} = High, V_{BAT} = 3.3 V to 5.5 V, I_{SIM_VCC} = 0 mA to 50 mA MOD_V_{CC} = Low, V_{BAT} = 2.7 V to 5.5 V, I_{SIM_VCC} = 0 mA to 50 mA	 2.8 1.7	2.8 3.0 1.8	 3.2 1.9	V V V
7	$I_{SIM_VCC_SC}$	Short –Circuit Current – SIM_V_{CC} shorted to ground , T_A=25°C			175	mA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

6. As long as $V_{BAT} - V_{DD} \leq$ 2.5 V. For $V_{BAT} - V_{DD}$ > 2.5 V the maximum value increases up to 35 μA (typical being in the +25 μA range).
7. As long as $V_{BAT} - V_{DD} \leq$ 2.5 V.
8. Guaranteed by design over the operating temperature range specified.

DIGITAL INPUT/OUTPUT SECTION CLOCK, RESET, I/O, $\overline{STOP}$, MOD_V_{CC}

Pin	Symbol	Rating	Min	Typ	Max	Unit
1,2, 13, 14, 15	V_{in}	Input Voltage Range ($\overline{STOP}$, MOD_V_{CC}, RST, CLK, I/O)	0		V_{DD}	V
	I_{IH} & I_{IL}	Input Current ($\overline{STOP}$, MOD_V_{CC}, RST, CLK)	−100		100	nA
13, 14	V_{IH} V_{IL}	High Level Input Voltage (RST, CLK) Low Level Input Voltage (RST, CLK)	0.7 * V_{DD} (Note 9)		V_{DD} 0.4	V V
1, 2	V_{IH}	High Level Input Voltage ($\overline{STOP}$, MOD_V_{CC})	0.7 * V_{DD} (Note 9)		V_{DD}	V
	V_{IL}	Low Level Input Voltage ($\overline{STOP}$, MOD_V_{CC})	0		0.4	V
15	$V_{OH_I/O}$ $V_{OL_I/O}$ I_{IH} I_{IL}	High Level Output Voltage (SIM_I/O = SIM_V_{CC}, $I_{OH_I/O}$ = −20 μA) Low Level Output Voltage (SIM_I/O = 0 V, $I_{OH_I/O}$ = 200 μA) High Level Input Current (I/O) Low Level Input Current (I/O)	0.7 * V_{DD} 0 −20		V_{DD} 0.4 20 1.0	V V μA mA
15	$R_{pu_I/O}$	I/0 Pullup Resistor	12	18	24	kΩ

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

9. If 1.6 V ≤ V_{DD} ≤ 1.8 V then V_{IHmin} = 1.26 V.

SIM INTERFACE SECTION (Note 10)

Pin	Symbol	Rating	Min	Typ	Max	Unit
9	SIM_RST	SIM_V_{CC} = +3.0 V (MOD_V_{CC} = High)				
		Output RESET V_{OH} @ I_{sim_rst} = −20 μA	0.9 * SIM_V_{CC}		SIM_V_{CC}	V
		Output RESET V_{OL} @ I_{sim_rst} = +200 μA	0		0.4	V
		Output RESET Rise Time @ Cout = 30 pF			1	μs
		Output RESET Fall Time @ Cout = 30 pF			1	μs
		SIM_V_{CC} = +1.8 V (MOD_V_{CC} = Low)				
		Output RESET V_{OH} @ I_{sim_rst} = −20 μA	0.9 * SIM_V_{CC}		SIM_V_{CC}	V
		Output RESET V_{OL} @ I_{sim_rst} = +200 μA	0		0.4	V
		Output RESET Rise Time @ Cout = 30 pF			1	μs
		Output RESET Fall Time @ Cout = 30 pF			1	μs
11	SIM_CLK	SIM_V_{CC} = +3.0 V (MOD_V_{CC} = High)				
		Output Duty Cycle	40		60	%
		Max Output Frequency	5			MHz
		Output V_{OH} @ I_{sim_clk} = −20 μA	0.9 * SIM_V_{CC}		SIM_V_{CC}	V
		Output V_{OL} @ I_{sim_clk} = +200 μA	0		0.4	V
		Output SIM_CLK Rise Time @ Cout = 30 pF			18	ns
		Output SIM_CLK Fall Time @ Cout = 30 pF			18	ns
		SIM_V_{CC} = +1.8 V (MOD_V_{CC} = Low)				
		Output Duty Cycle	40		60	%
		Max Output Frequency	5			MHz
		Output V_{OH} @ I_{sim_clk} = −20 μA	0.9 * SIM_V_{CC}		SIM_V_{CC}	V
		Output V_{OL} @ I_{sim_clk} = +200 μA	0		0.4	V
		Output SIM_CLK Rise Time @ Cout = 30 pF			18	ns
		Output SIM_CLK Fall Time @ Cout = 30 pF			18	ns
8	SIM_I/O	SIM_V_{CC} = +3.0 V (MOD_V_{CC} = High)				
		Output V_{OH} @ I_{SIM_IO} = −20 μA, $V_{I/O} = V_{DD}$	0.8 * SIM_V_{CC}		SIM_V_{CC}	V
		Output V_{OL} @ I_{SIM_IO} = +1 mA, $V_{I/O}$ = 0 V	0		0.4	V
		SIM_I/O Rise Time @ C_{out} = 30 pF			1	μs
		SIM_I/O Fall Time @ C_{out} = 30 pF			1	μs
		SIM_V_{CC} = +1.8 V (MOD_V_{CC} = High)				
		Output V_{OH} @ I_{SIM_IO} = −20 μA, $V_{I/O} = V_{DD}$	0.8 * SIM_V_{CC}		SIM_V_{CC}	V
		Output V_{OL} @ I_{SIM_IO} = +1.0 mA, $V_{I/O}$ = 0 V	0		0.3	V
		SIM_I/O Rise Time @ C_{out} = 30 pF			1	μs
		SIM_I/O Fall Time @ C_{out} = 30 pF			1	μs
8	$R_{pu_SIM_I/O}$	Card I/O Pullup Resistor	10	14	18	kΩ

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

10. All the dynamic specifications (AC specifications) are guaranteed by design over the operating temperature range.

TYPICAL CHARACTERISTICS

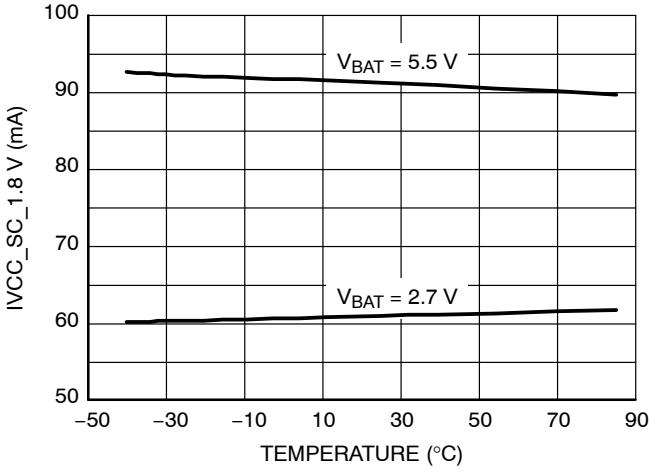


Figure 4. Short Circuit Current IV_{CC}_SC vs Temperature at SIM_V_{CC} = 1.8 V (MOD_V_{CC} = LOW)

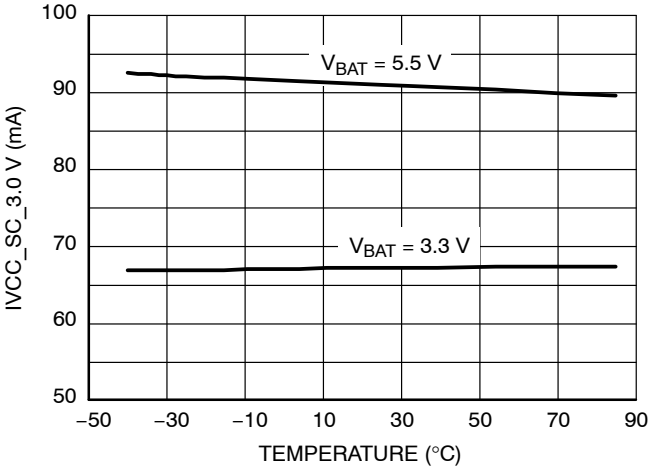


Figure 5. Short Circuit Current IV_{CC}_SC vs Temperature at SIM_V_{CC} = 3.0 V (MOD_V_{CC} = HIGH)

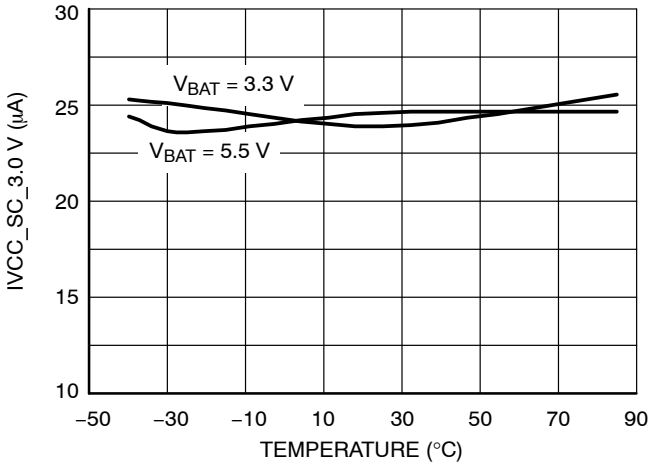


Figure 6. I_{BAT} vs temperature at 3.0 V

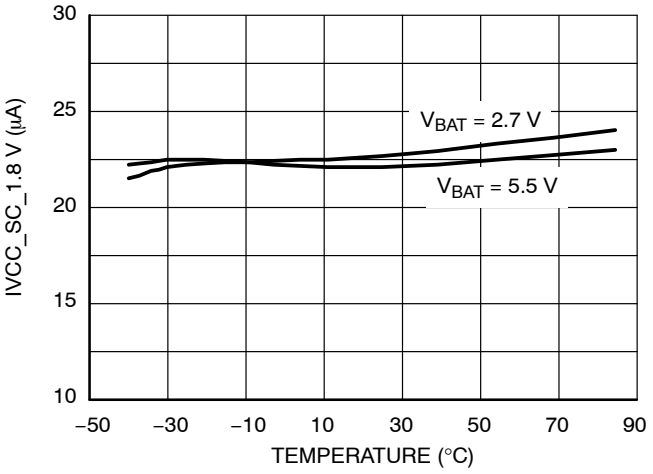


Figure 7. IV_{BAT} vs Temperature at 1.8 V

APPLICATION INFORMATION

CARD SUPPLY CONVERTER

The NCN4555 interface DC−DC converter is a Low Dropout Voltage Regulator capable of suppling a current in excess of 50 mA under 1.8 V or 3.0 V. This device features a very low quiescent current typically lower than 25 μA (Figure 6 and 7). MOD_V_{CC} is a select input allowing a logic level signal to select a regulated voltage of 1.8 V (MOD_V_{CC} = LOW) or 3.0 V (MOD_V_{CC} = HIGH). Additionally, the NCN4555 has a shutdown input allowing it to turn off or turn on the regulator output. The shutdown mode power consumption is typically in the range of a few tens of nA (30 nA Typical). Figure 8 shows a simplified view of the NCN4555 voltage regulator. The SIM_V_{CC} output is internally current limited and protected against short circuits. The short−circuit current IV_{CC} is constant over the temperature and SIM_V_{CC}. It varies with V_{BAT} typically in the range of 60 mA to 90 mA (Figure 4 and 5).

In order to guarantee a stable and satisfying operating of the LDO the SIM_V_{CC} output will be connected to a 1.0 μF bypass ceramic capacitor to the ground. At the input, V_{BAT} will be bypassed to the ground with a 0.1 μF ceramic capacitor.

LEVEL SHIFTERS

The level shifters accommodate the voltage difference that might exist between the microcontroller and the smart card. The RESET and CLOCK level shifters are monodirectional and feature both the same architecture.

The bidirectional I/O line provides a way to automatically adapt the voltage difference between the MCU and the SIM card in both directions. In addition with the pullup resistor, an active pullup circuit (Figure 8, Q1 and Q2) provides a fast charge of the stray capacitance, yielding a rise time fully within the ISO7816 specifications.

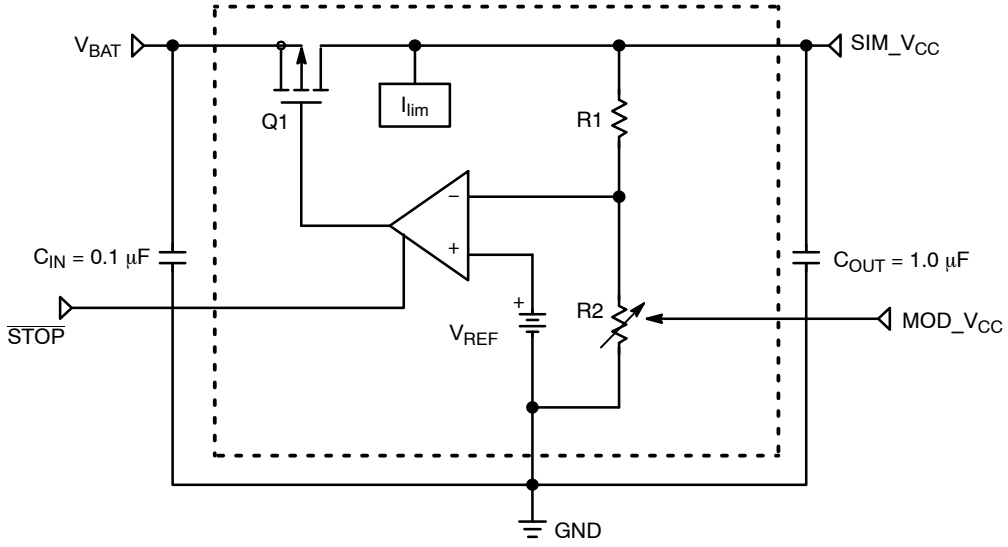


Figure 8. Simplified Block Diagram of the LDO Voltage Regulator

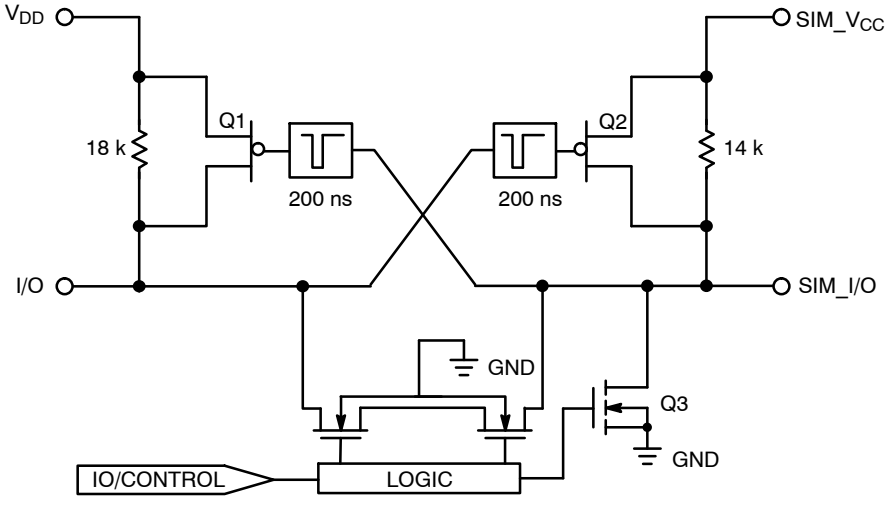


Figure 9. Basic I/O Line Interface

The typical waveform provided in Figure 10 shows how the accelerator operates. During the first 200 ns (typical), the slope of the rise time is solely a function of the pullup resistor associated with the stray capacitance. During this period, the PMOS devices are not activated since the input voltage is below their V_{gs} threshold. When the input slope crosses the V_{gsth}, the opposite one shot is activated, providing a low impedance to charge the capacitance, thus increasing the rise time as depicted in Figure 10. The same mechanism applies for the opposite side of the line to make sure the system is optimum.

INPUT SCHMITT TRIGGERS

All the Logic input pins (excepted I/O and SIM_I/O, See Figure 3) have built−in Schmitt trigger circuits to prevent the NCN4555 against uncontrolled operation. The typical dynamic characteristics of the related pins are depicted Figure 11.

The output signal is guaranteed to go High when the input voltage is above 0.7 x V_{DD}, and will go Low when the input voltage is below 0.4 V.

SHUTDOWN OPERATING

In order to save power or for other purpose required by the application it is possible to put the NCN4555 in a shutdown mode by setting Low the pin $\overline{STOP}$. On the other hand the device enters automatically in a shutdown mode when V_{DD} becomes lower than 1.1 V typically.

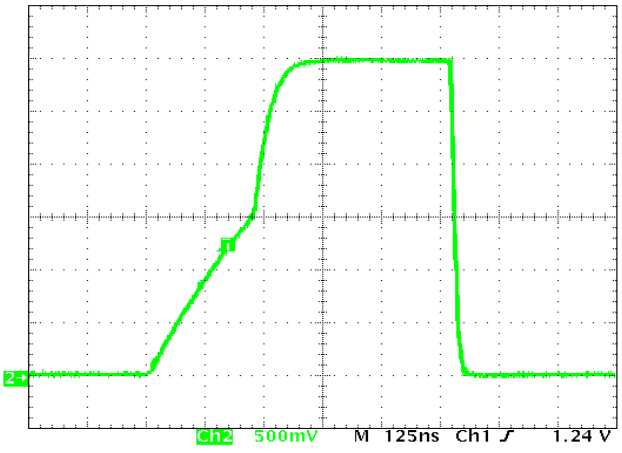


Figure 10. SIM_IO Typical Rise and Fall Times with Stray Capacitance > 30 pF (33 pF Capacitor Connected on the Board)

ESD PROTECTION

The NCN4555 SIM interface features an HBM ESD voltage protection in excess of 7 kV for all the SIM pins (SIM_IO, SIM_CLK, SIM_RST, SIM_V_{CC} and GND). All the other pins (microcontroller side) sustain at least 2 kV. These values are guaranteed for the device in its full integrity without considering the external capacitors added to the circuit for a proper operating. Consequently in the operating conditions it is able to sustain much more than 7 kV on its SIM pins making it perfectly protected against electrostatic discharge well over the HBM ESD voltages required by the ISO7816 standard (4 kV).

PRINTED CIRCUIT BOARD LAYOUT

Careful layout routing will be applied to achieve a good and efficient operating of the device in its mobile or portable environment and fully exploit its performance.

The bypass capacitors have to be connected as close as possible to the device pins (SIM_V_{CC}, V_{DD} or V_{BAT}) in order to reduce as much as possible parasitic behaviors (ripple and noise). It is recommended to use ceramic capacitors.

The exposed pad of the QFN−16 package will be connected to the ground as well as the unconnected pins (NC). A relatively large ground plane is recommended.

Figures 12 and 13 shows an example of PCB device implementation in an evaluation environment.

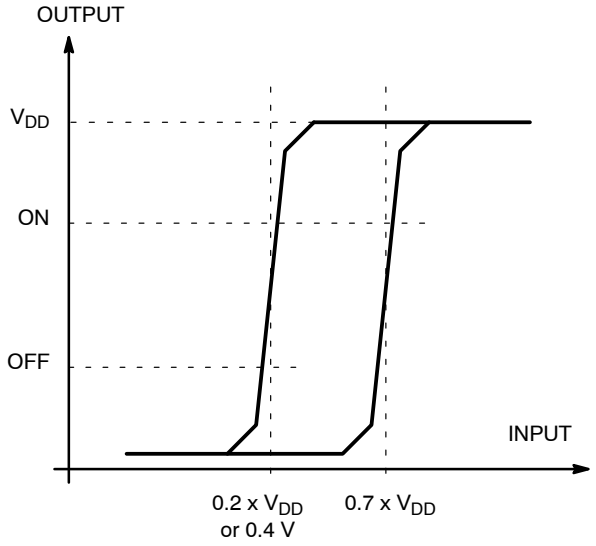


Figure 11. Typical Schmitt Trigger Characteristics

EVALUATION BOARD AND PCB GUIDELINES

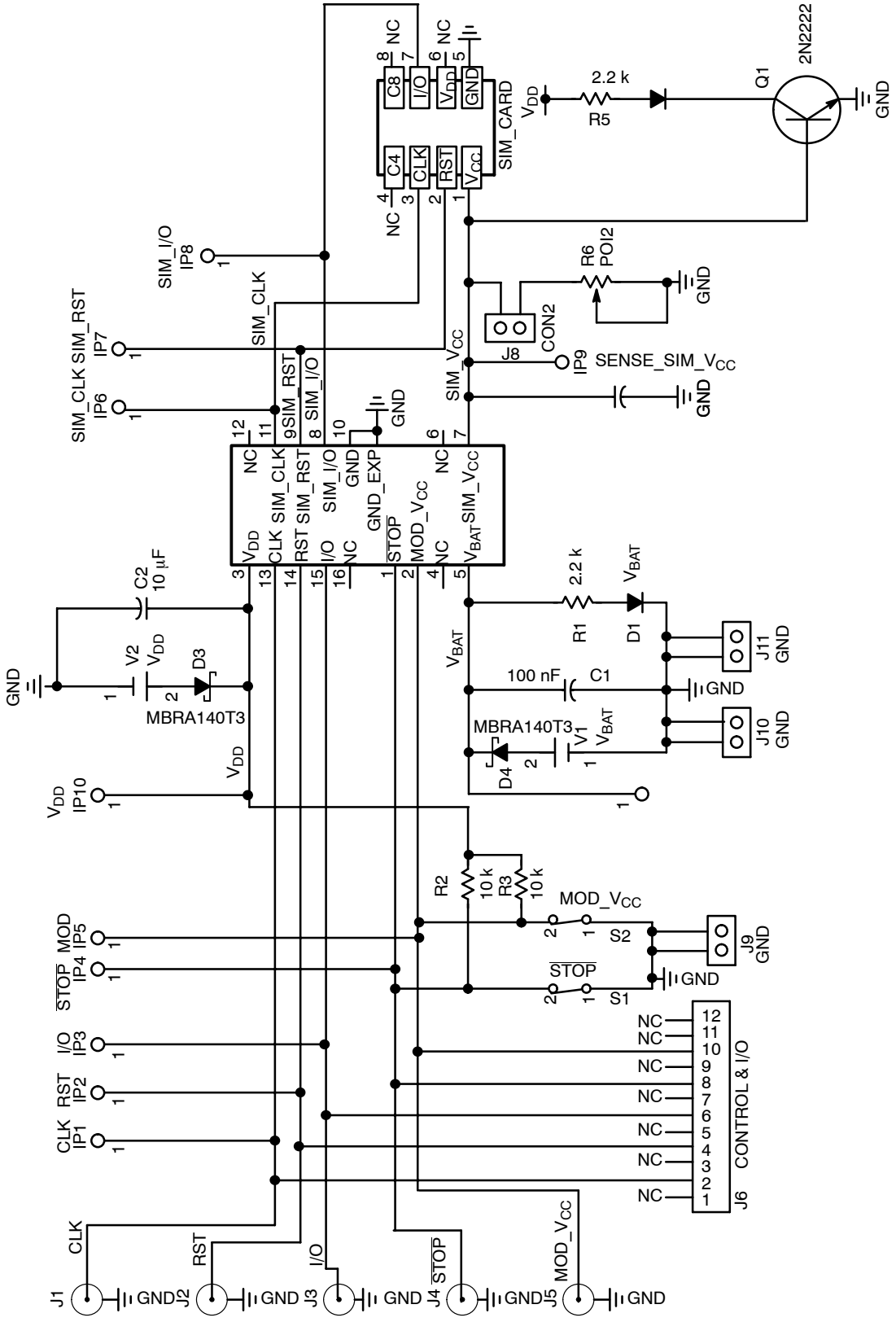
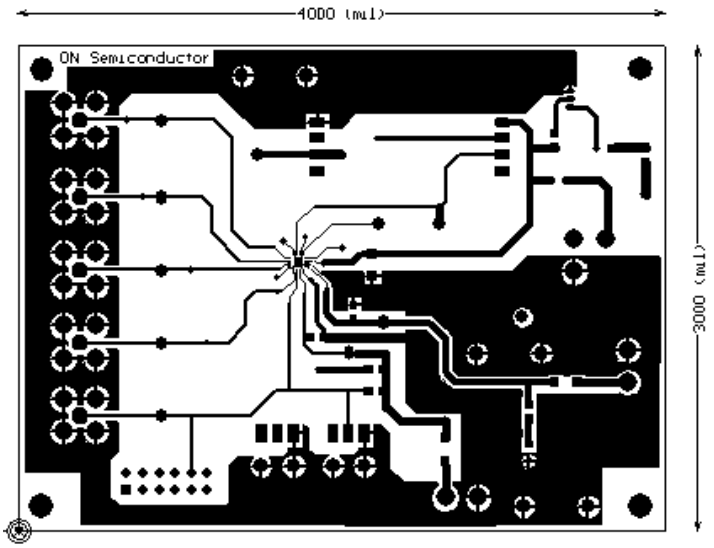
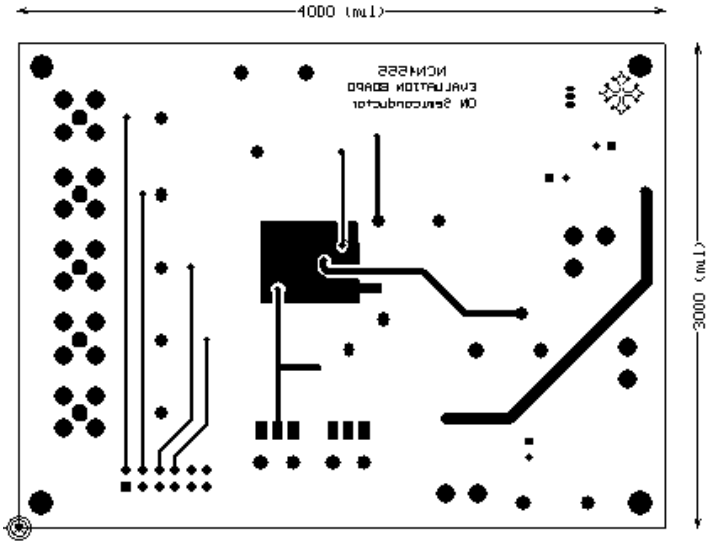


Figure 12. NCN4555 engineering test board schematic diagram

EVALUATION BOARD AND PCB GUIDELINES



Top Layer



Bottom Layer

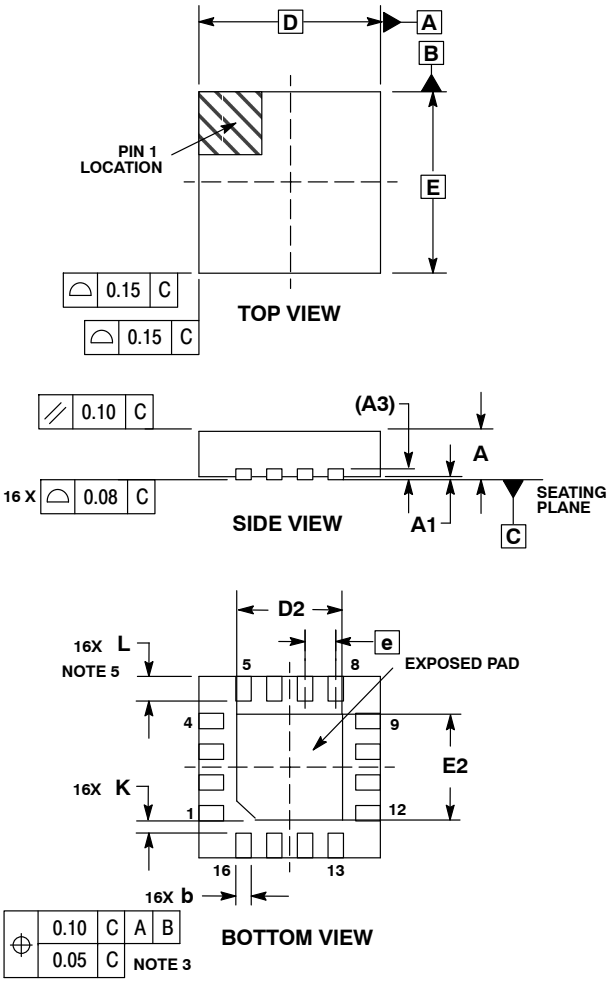
Figure 13. NCN4555 Printed Circuit Board Layout (Engineering board)

QFN16 3*3*0.75 MM, 0.5 P
CASE 488AK−01
ISSUE O

DATE 13 SEP 2004



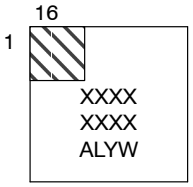
SCALE 2:1



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. L_{max} CONDITION CAN NOT VIOLATE 0.2 MM SPACING BETWEEN LEAD TIP AND FLAG.

	MILLIMETERS	
DIM	MIN	MAX
A	0.70	0.80
A1	0.00	0.05
A3	0.20 REF	
b	0.18	0.30
D	3.00 BSC	
D2	1.65	1.85
E	3.00 BSC	
E2	1.65	1.85
e	0.50 BSC	
K	0.20	−−−
L	0.30	0.50

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G”, may or not be present.

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DESCRIPTION:	**QFN16, 3*3*0.75 MM, 0.5 PITCH**		**PAGE 1 OF 1**

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