NCL30185FLYGEVB, NCL30188FLYGEVB

10 W High Power Factor Isolated LED Driver Evaluation Board User's Manual

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EVAL BOARD USER'S MANUAL

Overview

This manual covers the specification, theory of operation, testing and construction of the NCL30185/88FLYGEVB demonstration board. The NCL30185/88 board demonstrates a 10 W high PF isolated flyback LED driver in a typical A19 outline. The 2 demo boards are nearly identical in construction except for the controller and Vcc bulk capacitor. The NCL30188 controller is a non−dimming version while the NCL30185 supports 3 levels of step dimming.

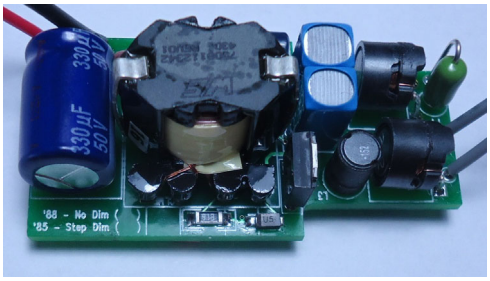


Figure 1. NCL30185FLYGEVB/ NCL30188FLYGEVB Evaluation Board

Specifications

Input voltage (Class 2 Input, no ground)	90 – 265 V ac	
Line Frequency	50 Hz/60 Hz	
Power factor (100% Load)	0.9	Min
THD (100% Load)	20%	Max
Class 2 Output Mains Isolated		
Output Voltage Range	14 – 28 V dc	
Output Current	350 mA dc	±2%
Efficiency	85%	Typ.
Start Up Time	< 500 msec	Typ.
EMI (conducted)	Class B	FCC/CISPR

As illustrated, the key features of this demo board include:

- Wide Mains
- Low THD across line and load
- High Power Factor across wide line and load
- Integrated auto recovery fault protection (can be letched by choice A version)
  - Programmable over temperature thermal foldback (NTC mounted on PCB)
  - Cycle by cycle current limiting
  - Open LED and shorted output protection

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THEORY OF OPERATION

Power Stage

The power stage for the demo boards is an isolated flyback. The controller has a built in control algorithm that is specific to the flyback transfer function. Specifically:

$$\frac{Vout}{Vin} = \frac{Duty}{(1 - Duty)} \quad \text{(eq. 1)}$$

This is applicable to flyback, buck boost, and SEPIC converters. The control is very similar to the control of the NCL30080−83 with the addition of a power factor correction control loop. The controller has a built in hardware algorithm that relates the output current to a reference on the primary side.

$$Iout = \frac{Vref \times Nps}{2 \times Rsense} \quad \text{(eq. 2)}$$

$$Nps = \frac{Npri}{Nsec} \quad \text{(eq. 3)}$$

Where Npri = Primary Turns & Nsec = Secondary Turns

We can now find Rsense for a given output current.

$$Rsense = \frac{Vref \times Nps}{2 \times Iout} \quad \text{(eq. 4)}$$

Line Feedforward

R3 sets the line feedforward which compensates for power stage delay times by reducing the current threshold as the line voltage increases. R3 is also used by the shorted pin detection. At start up the controller generates a current from the CS pin to check for a short to ground. If R3 is zero, the current sense resistor is too low a value and the controller will not start because it will detect a shorted pin. So R3 is required to make the controller operate properly.

Voltage Sense

The voltage sense pin has several functions:

1. Basis for the reference of the PFC control loop
2. Line Range detection

The reference scaling is automatically controller inside the controller. While the voltage on Vs is not critical for the PFC loop control it is important for range detection. Generally the voltage on Vs should be 3.5 V peak at the highest input voltage of interest. The voltage on Vs determines which valley the power stage will operate at in full load. At low line and maximum load, the power stage operates in the first valley (standard CrM operation). At the higher line range, the power stage moves to the second valley to lower the switching frequency while retaining the advantage of CrM soft switching.

Auxiliary Winding

The auxiliary winding has 3 functions:

1. CrM timing
2. Vcc Power
3. Output voltage sense

CrM Timing

In the off time, the voltage on the transformer/inductor forward biases Dout and D9. When the current in the magnetic has reached zero, the voltage collapses to zero. This voltage collapse triggers a comparator on the ZCD pin to start a new switching cycle. The ZCD pin also counts rings on the auxiliary winding for higher order valley operation. A failure of the ZCD pin to reach a certain threshold also indicates a shorted output condition fault.

Vcc Power

The auxiliary winding forward biases D9 to provide power for the controller. This arrangement is called a “bootstrap”. Initially the Cvcc, is charged through R4 and R5. When the voltage on Cvcc reaches the startup threshold, the controller starts switching and providing power to the output circuit and the Cvcc. Cvcc discharges as the controller draws current. As the output voltage rises, the auxiliary winding starts to provide all the power to the controller. Ideally, this happens before Cvcc discharges to the undervoltage threshold where the controller stops operating to allow Cvcc to recharge once again. The size of the output capacitor will have a large effect on the rise of the output voltage. Since the LED driver is a current source, the rise of output voltage is directly dependent on the size of the output capacitor.

There are tradeoffs in the selection of Cout and Cvcc. A low output ripple will require a large Cout value. This requires that Cvcc be large enough to support Vcc power to the controller while Cout is charging up. A large value of Cvcc requires that R4 and R5 be lower in value to allow a fast enough startup time. Smaller values of R4 and R5 have higher static power dissipation which lowers efficiency of the driver.

Output Voltage Sense

The auxiliary winding voltage is proportional to the output voltage by the turns ratio of the output winding and the auxiliary winding. The controller has an overvoltage limit on the Vcc pin at about 26 V minimum. Above that threshold, the controller will stop operation and enter a fault mode for overvoltage. This is the open load protection.

In cases where the output has a lot of ripple current and the LED has high dynamic resistance, the peak output voltage can be much higher than the average output voltage. The auxiliary winding will charge the Cvcc to the peak of the output voltage which may trigger the OVP sooner than expected.

SD Pin

The SD pin is a multifunction protection input.

1. Thermal Foldback protection
2. Programmable OVP

Thermal Foldback

The OCV of the SD pin is 1.35 V. There is an internal current source connected to the SD pin even though the voltage is soft clamped to 1.35 V. Output current is reduced when the voltage on the SD pin drops below 1 V. Placing an NTC on the SD pin will allow the designer to choose the level of protection from over temperature. Below 0.5 volts on SD, the controller stops. Series or parallel resistors on the NTC can shape the foldback curve. An online EXCEL® based design tool is available at onsemi.com which provides support to select the appropriate value.

Programmable OVP

While the SD pin has a current source for the OTP, it can be overcome raising the voltage on the SD pin. At about 2.75 V, the SD pin detects an OVP and shuts down the controller. Typically, a zener to Vcc is used for this. In this way, the designer can set the OVP to a lower value that the OVP threshold built into the Vcc pin.

Step Dimming

Step dimming is only available on the NCL30185FLYGEVB. Cbulk is added to keep Vcc active for brief AC power interruptions. There are 3 dimming current levels for the NCL30185FLYGEVB after the driver is powered on.

ON	100%
1.	70%
2.	25%
3.	4%

AC power interruption is detected on Vs when the voltage on Vs is below 1 V for 30 ms. Internally, the controller steps the internal Vref down to the next dimming level. After the lowest level, Vref cycles back to 100%. Issues with step dimming can be traced to Vcc dropping below the undervoltage cutoff before the input has been detected as off for 35 ms minimum.. This is caused by one of the following:

1. Operating Vcc too low (related to Vled)
2. Cbulk too small
3. Cout too large and discharges too much during the AC interruption. This is particularly seen at the lowest dim levels where the output current cannot recharge Cout fast enough.

For a more detailed discussion of step dimming, refer to DN05065/D.

Circuit Modifications

Output Current

The output current is set by the value of Rsense as shown above. It's possible to adjust easily change the output current within ±10% of the set value by changing R7. Further adjustments may require changes to the transformer depending on the LED V_F and current.

SCHEMATIC

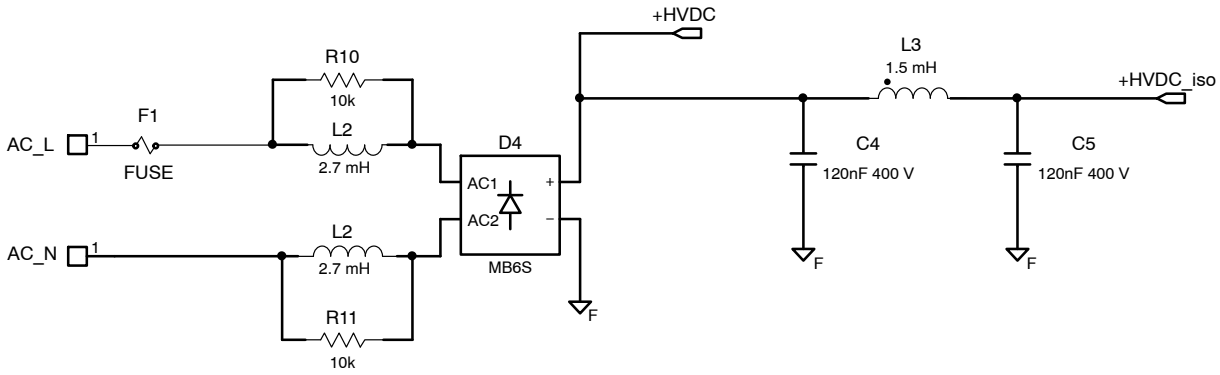


Figure 2. Input Circuit

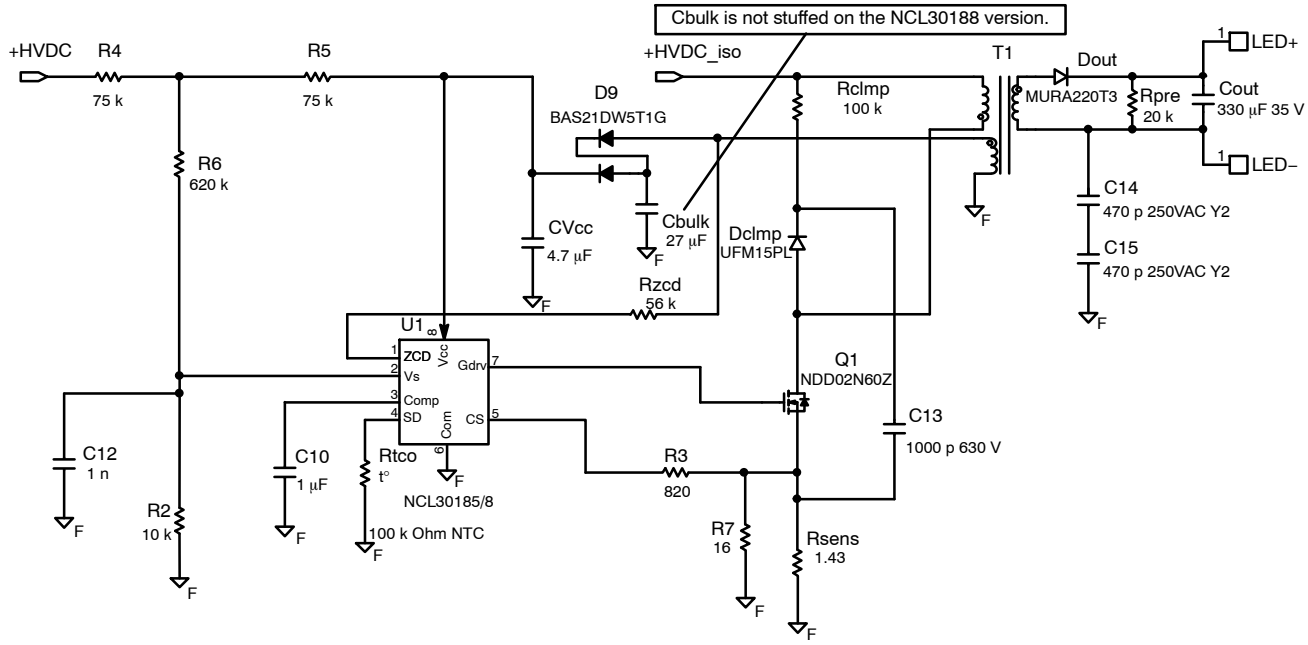


Figure 3. Main Schematic

BILL OF MATERIAL

Table 1. BILL OF MATERIAL

Quantity	Reference	Part	Manufacturer	Mfr_PN	PCB Footprint	Substitution Allowed
1	CVcc	4.7 μF	AVX	TAJB475M035RNJ	1210	Yes
1	Cbulk	27 μF	Panasonic	EEU−FC1E270	CAP−ALEL−4X11−HOR	Yes
1	Cout	330 μF 35 V	Nichicon	UHE1V331MPD	CAP−ALEL−10X16−HOR	Yes
2	C4, C5	120 nF 400 V	Epcos	B32559C6124+***	CAP−BOX−LS5−5M0X7M2	Yes
1	C10	1 μF	Taiyo Yuden	GMK107AB7105KAHT	603	Yes
1	C12	1 nF	Kemet	C0402C102K3GACTU	402	Yes
1	C13	1000 p 630 V	Kemet	C0805C102KBRACTU	805	Yes
2	C14, C15	470 p 250 VAC Y2	Murata	GA342QR7GF471KW01L	1808	Yes
1	Dclmp	UFM15PL	MCC	UFM15PL	SOD123FL	Yes
1	Dout	MURA2230T3	ON Semiconductor	MURA220T3	SMA	No
1	D4	MB6S	MCC	MB6S	MB6S	Yes
1	D9	BAS21DW5T1G	ON Semiconductor	BAS21DW5T1G	SC−88A	No
1	F1	FUSE	Littelfuse	0263.500WRT1L	FUSE−HAIRPIN−LS250	Yes
2	L1, L2	2.7 mH	Bourns	RL875S−272K	Drum_Core_Hor_LS5_875S	Yes
1	L3	1.5 mH	Wurth	7447462152	IND−UPRIGHT−LS25	Yes
1	Q1	NDD02N60Z	ON Semiconductor	NDD02N60Z	IPAK	No
1	Rclmp	100 kΩ	Yaego	RC1206FR−07100KL	1206	Yes
1	Rpre	20 kΩ	Yaego	RC0603FR−0720KL	603	Yes
1	Rsens	1.43 Ω	Yaego	RC1206FR−071R43L	1203	Yes
1	Rtco	100 kΩ NTC	Epcos	B57331V2104J60	603	Yes
1	Rzcd	56 kΩ	Yaego	RC0805FR−0756KL	805	Yes
1	R2	10 kΩ	Yaego	RC0402FR−0710KL	402	Yes
1	R3	820 Ω	Yaego	RC0402FR−07820RL	402	Yes
2	R4, R5	75 kΩ	Yaego	RC1206FR−0775KL	1206	Yes
1	R6	620 kΩ	Yaego	RC1206FR−07620KL	1206	Yes
1	R7	16 Ω	Yaego	RT0402FRE0716RL	603	Yes
2	R10, R11	10 kΩ	Yaego	RC0805JR−0710KL	805	Yes
1	T1	XFRM_LINEAR	Wurth	7508112342	RM6−4P−THFLYLEADS	Yes
1	U1	NCL30185B	ON Semiconductor	NCL30185B	SO8	No
		NCL30185B		NLC30188B		
6″	W1	Wire, Red, 24 AWG	McMaster Carr	7587K922	UL1569	Yes
6″	W2	Wire, Blk, 24 AWG	McMaster Carr	7587K921	UL1569	Yes
12″	W3, W4	Wire, Wht, 24 AWG	McMaster Carr	7587K924	UL1569	Yes
Note: All Components to comply with RoHS 2002/95/EC						

GERBER VIEWS

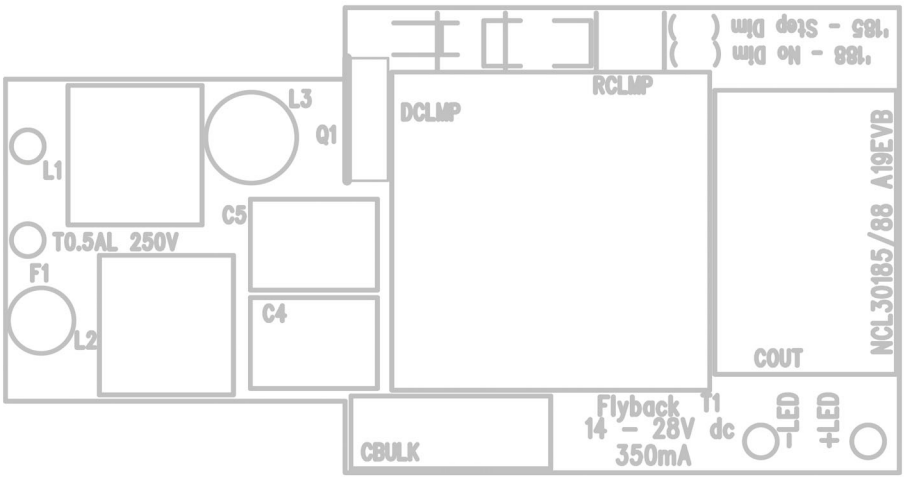


Figure 4. Top Side PCB

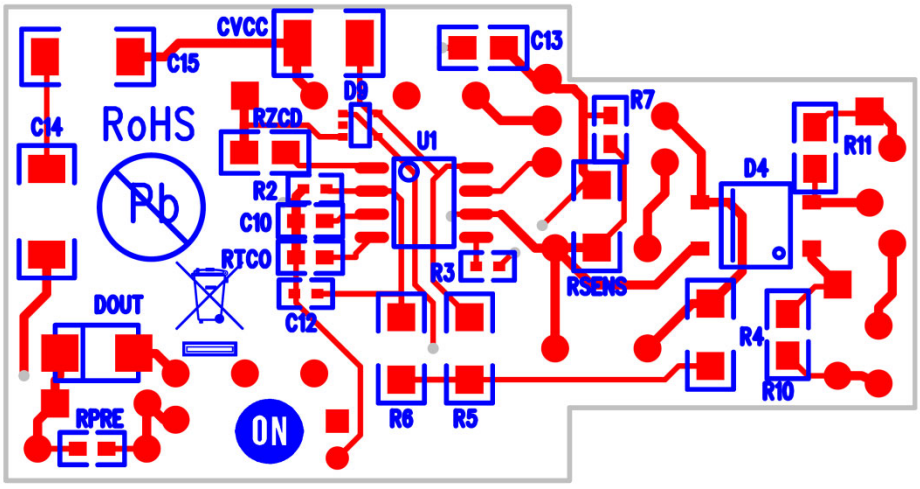


Figure 5. Bottom Side PCB

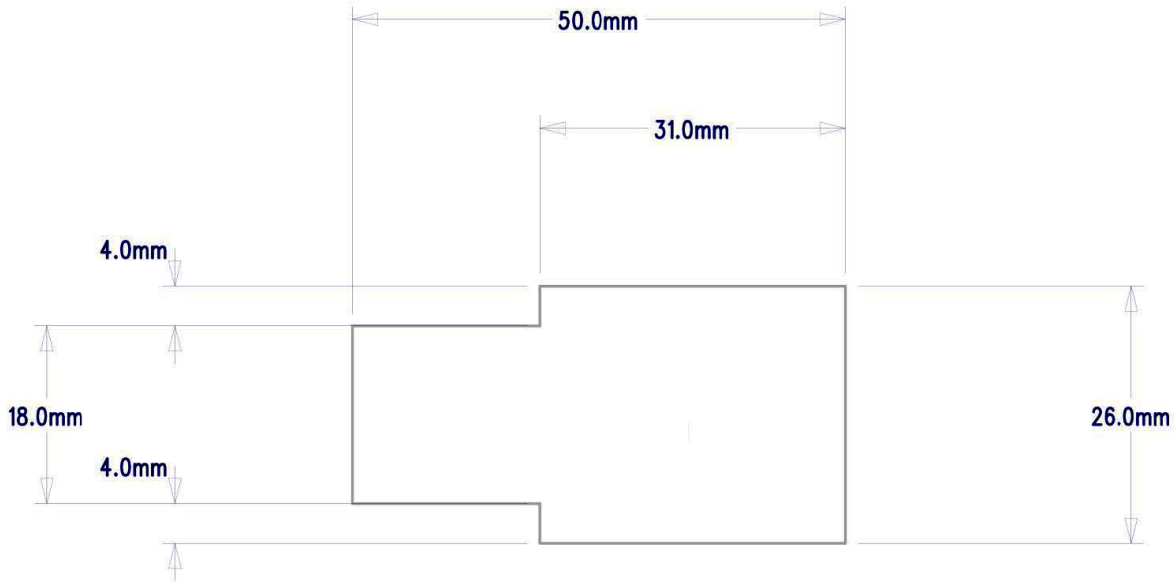
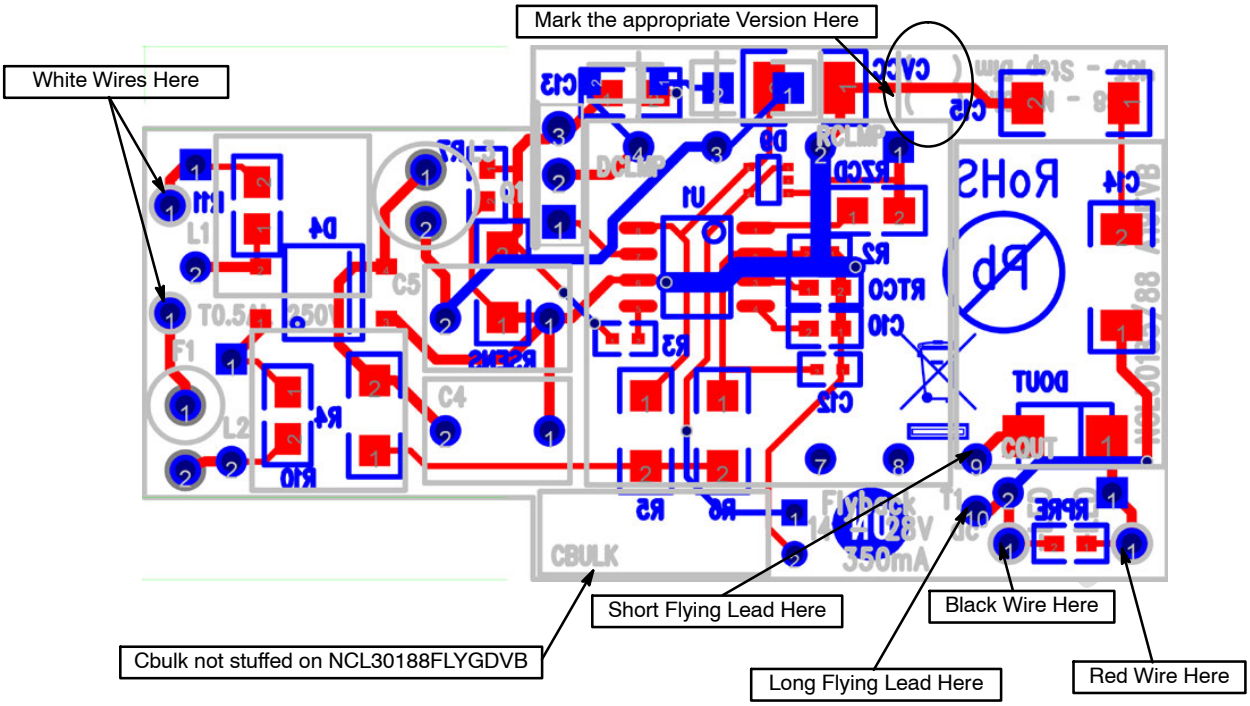


Figure 6. PCB Outline



NOTES:

1. Trim Transformer flying leads for minimum length.
2. Strip and tin lead wires to 6″ ±0.5″ 4 Places.

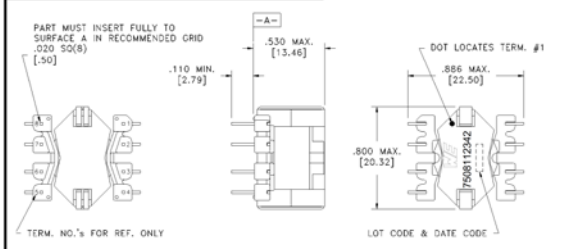
Figure 7. Assembly Notes

CIRCUIT BOARD FABRICATION NOTES

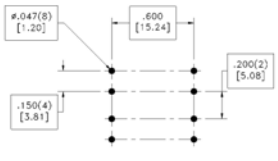
1. Fabricate per IPC−6011 and IPC6012. Inspect to IPA−A−600 Class 2 or updated standard.
2. Printed Circuit Board is defined by files listed in fileset.
3. Modification to copper within the PCB outline is not allowed without permission, except where noted otherwise. The manufacturer may make adjustments to compensate for manufacturing process, but the final PCB is required to reflect the associated gerber file design ±0.001 in. for etched features within the PCB outline.
4. Material in accordance with IPC−4101/21, FR4, Tg 125°C min.
5. Layer to layer registration shall not exceed ±0.004 in.
6. External finished copper conductor thickness shall be 0.0026 in. min. (ie 2 oz)
7. Copper plating thickness for through holes shall be 0.0013 in. min. (ie 1 oz)
8. All holes sizes are finished hole size.
9. Finished PCB thickness 0.031 in.
10. All un-dimensioned holes to be drilled using the NC drill data.
11. Size tolerance of plated holes: ±0.003 in.: non−plated holes ±0.002 in.
12. All holes shall be ±0.003 in. of their true position U.D.S.
13. Construction to be SMOBC, using liquid photo image (LPI) solder mask in accordance with IPC−SM−B40C, Type B, Class 2, and be green in color.
14. Solder mask mis−registration ±0.004 in. max.
15. Silkscreen shall be permanent non−conductive white ink.
16. The fabrication process shall be UL approved and the PCB shall have a flammability rating of UL94V0 to be marked on the solder side in silkscreen with date, manufactures approved logo, and type designation.
17. Warp and twist of the PCB shall not exceed 0.0075 in. per in.
18. 100% electrical verification required.
19. Surface finish: electroless nickel immersion gold (ENIG)
20. RoHS 2002/95/EC compliance required.

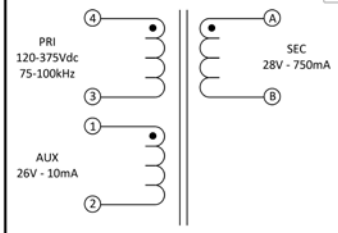
FLYBACK TRANSFORMER SPECIFICATION

CUSTOMER TERMINAL	RoHS	LEAD(Pb)--FREE
Sn 96%, Ag 4%	Yes	Yes



Views need to include flying leads. Short lead indicates lead A. JLV 8/27/14





ELECTRICAL SPECIFICATIONS @ 25° C unless otherwise noted:

PARAMETER		TEST CONDITIONS	VALUE
D.C. RESISTANCE	4-3	@20°C	0.680 ohms ±10%
D.C. RESISTANCE	A-B	@20°C	0.065 ohms ±15%
D.C. RESISTANCE	1-2	@20°C	0.360 ohms ±10%
INDUCTANCE	4-3	10KHz, 100mV, Ls	640.0µH ±10%
SATURATION CURRENT	4-3	20% rolloff from initial	1.0A
LEAKAGE INDUCTANCE	4-3	tie(A+B),100KHz, 100mV, Ls	15.0µH max.
LEAKAGE INDUCTANCE	1-2	tie(A+B),100KHz, 100mV, Ls	1.5µH max.
DIELECTRIC	4-A	tie(2+3), 4000VAC, 1 second	4000VAC, 1 minute
DIELECTRIC	4-1	625VAC, 1 second	
TURNS RATIO		(4-3):(1-2)	4.31:1, ±1%
TURNS RATIO		(4-3):(A-B)	4:1, ±1%

GENERAL SPECIFICATIONS:

OPERATING TEMPERATURE RANGE: -40°C to +125°C including temp rise.

Designed to comply with the following requirements as defined by IEC61347-2-13:
- Reinforced insulation for a primary circuit at a working voltage of 375VDC.

Wire insulation & RoHS status not affected by wire color. Wire insulation color may vary depending on availability.

DFM	SP	Packaging Specifications	CONVENTION PLACEMENT	Tolerances unless otherwise specified: Angles: ±1° Decimals: ±.005 [.13] Fractions: ±1/64 Footprint: ± .001 [.03]	DRAWING TITLE: TRANSFORMER
DATE	8/27/2014	Method: Tray			PART NO.: 7508112342
ENG	JLV	PKG-0155			
REV.	02			This drawing is dual dimensioned. Dimensions in brackets are in millimeters.	
DATE	9/2/2014	www.we-online.com/midcom			SPECIFICATION SHEET 1 OF 1

ECA PICTURES

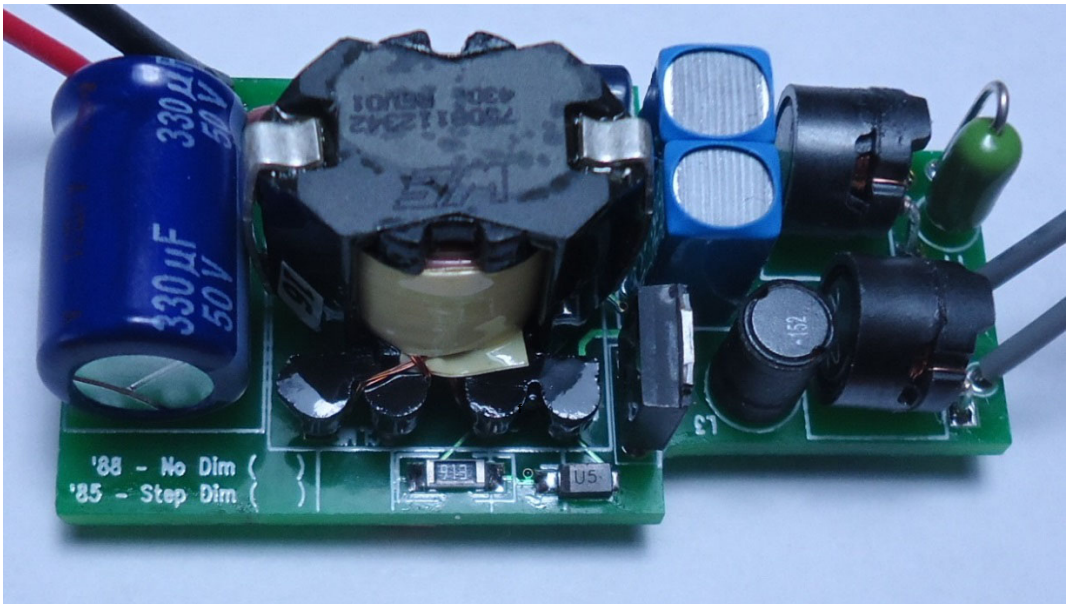


Figure 8. Top View

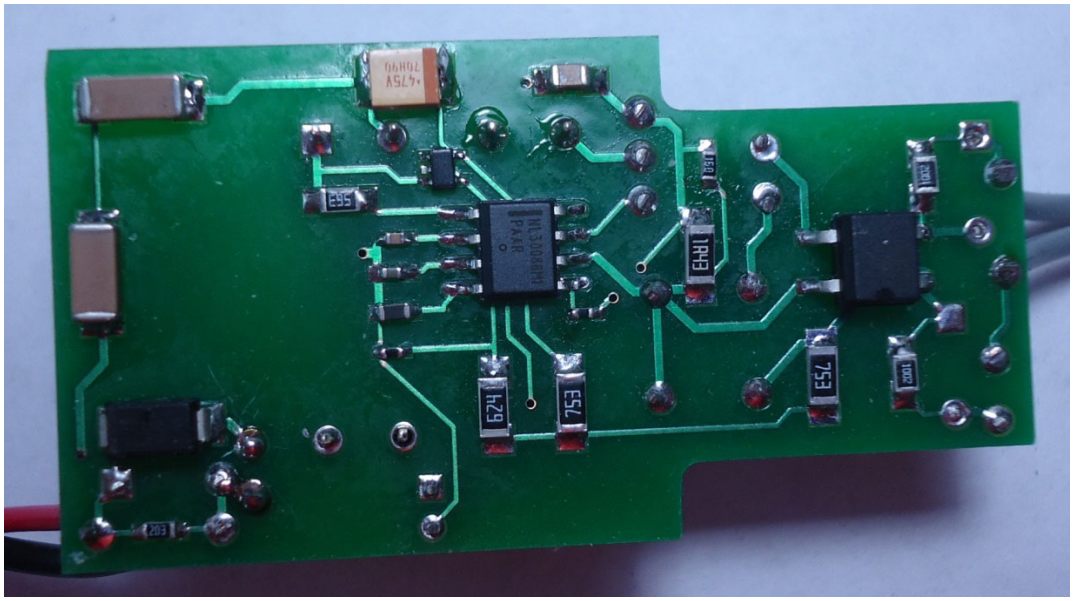


Figure 9. Bottom View

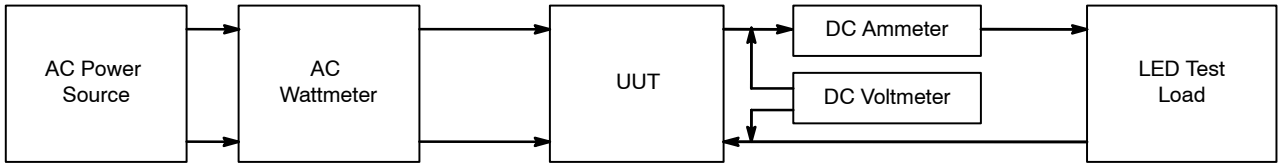
TEST PROCEDURE

Equipment Needed

- AC Source – 90 to 305 V ac 50/60 Hz Minimum 500 W capability
- AC Wattmeter – 300 W Minimum, True RMS Input Voltage, Current, Power Factor, and THD 0.2% accuracy or better

Test Connections

1. Connect the LED Load to the red(+) and black(−) leads through the ammeter shown in Figure 10. Caution: Observe the correct polarity or the load may be damaged.
2. Connect the AC power to the input of the AC wattmeter shown in Figure 10. Connect the white leads to the output of the AC wattmeter
3. Connect the DC voltmeter as shown in Figure 10.



NOTE: Unless otherwise specified, all voltage measurements are taken at terminals of the UUT.

Figure 10. Test Set Up

Functional Test Procedure

1. Set the LED Load for 26 V output.
2. Set the input power to 120 V 60 Hz. Caution: Do not touch the ECA once it is energized because there are hazardous voltages present.

LINE AND LOAD REGULATION

Table 2. 120 V/MAX LOAD

	Output Current 350 mA ±14 mA	Output Power	Power Factor	THD < 20%
14 V				
21 V				
28 V				

Table 3. 230 V/MAX LOAD

	Output Current 350 mA ±14 mA	Output Power	Power Factor	THD < 30%
14 V				
21 V				
28 V				

$$\text{Efficiency} = \frac{\text{Vout} \times \text{Iout}}{\text{Pin}} \times 100\% \qquad \text{(eq. 5)}$$

TEST DATA

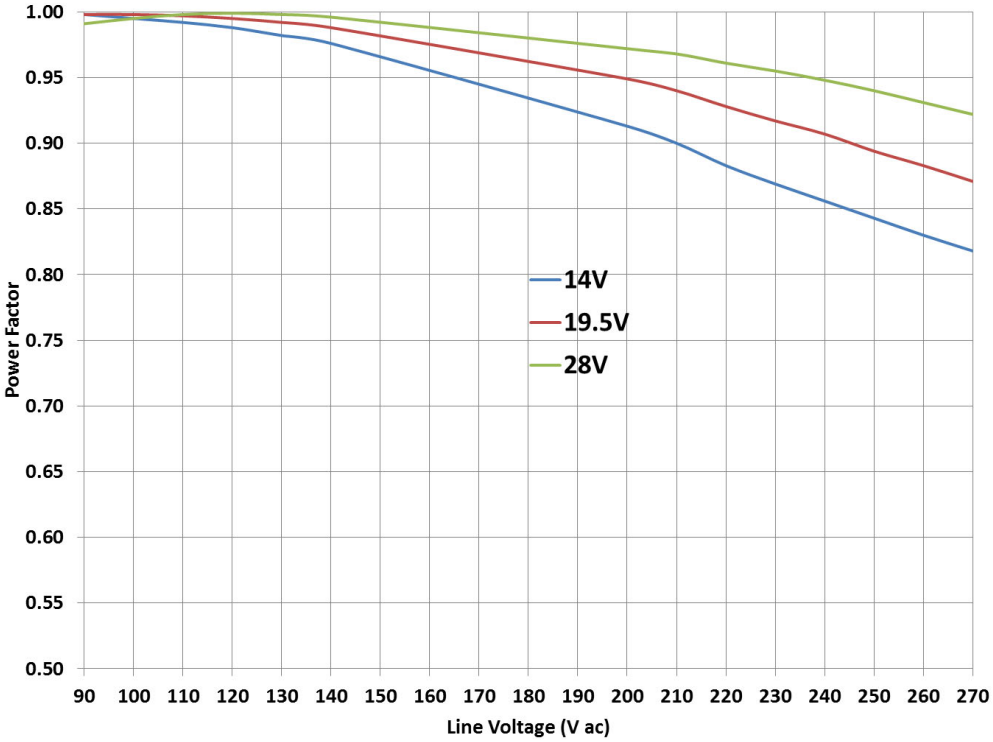


Figure 11. Power Factor over Line and Load

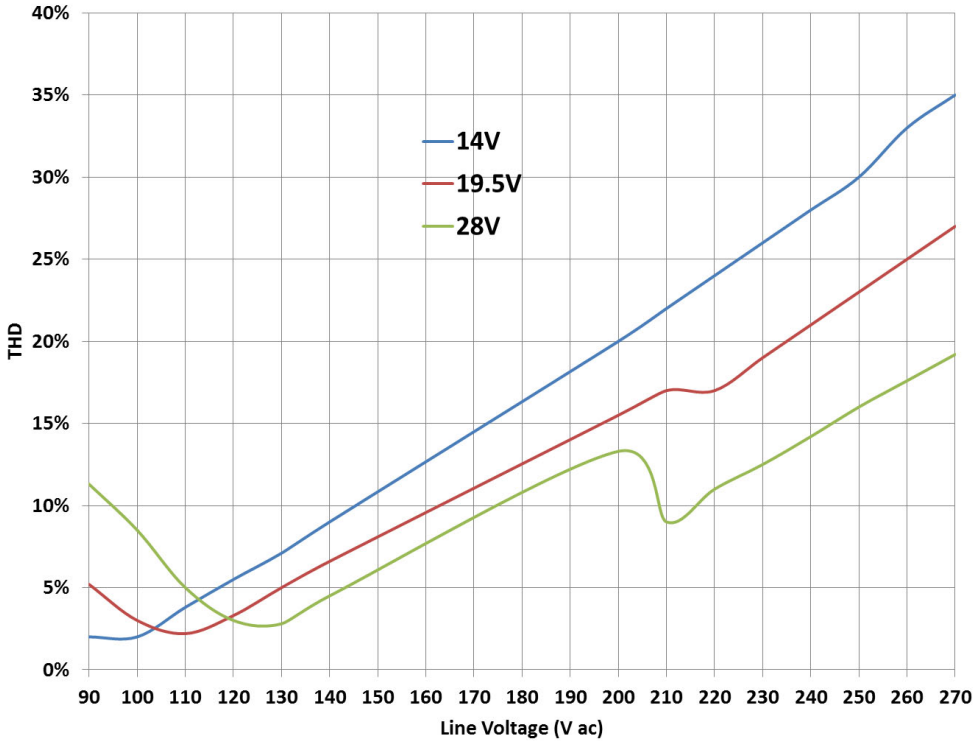


Figure 12. THD over Line and Load

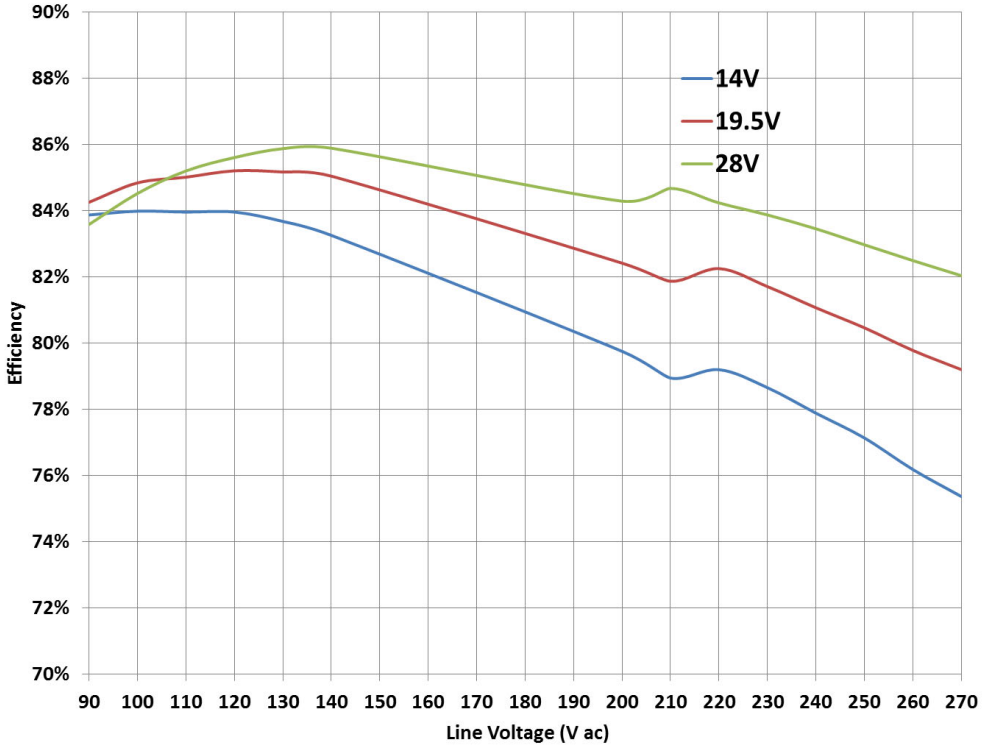


Figure 13. Efficiency over Line and Load @ Maximum Output Current

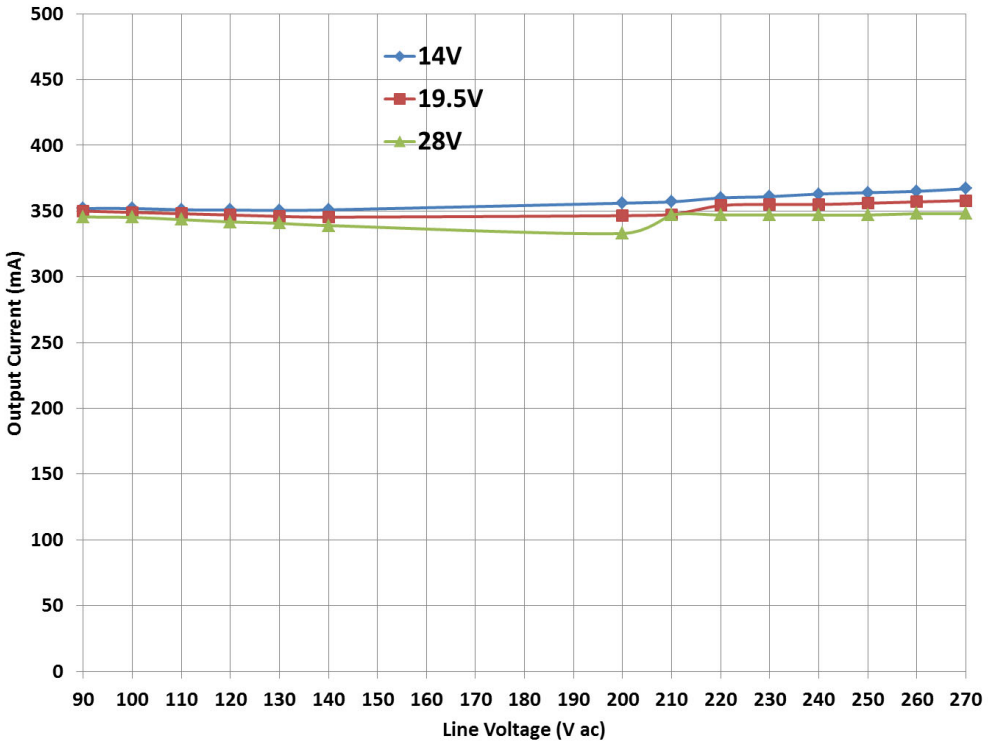


Figure 14. Maximum Current Load Regulation over Line

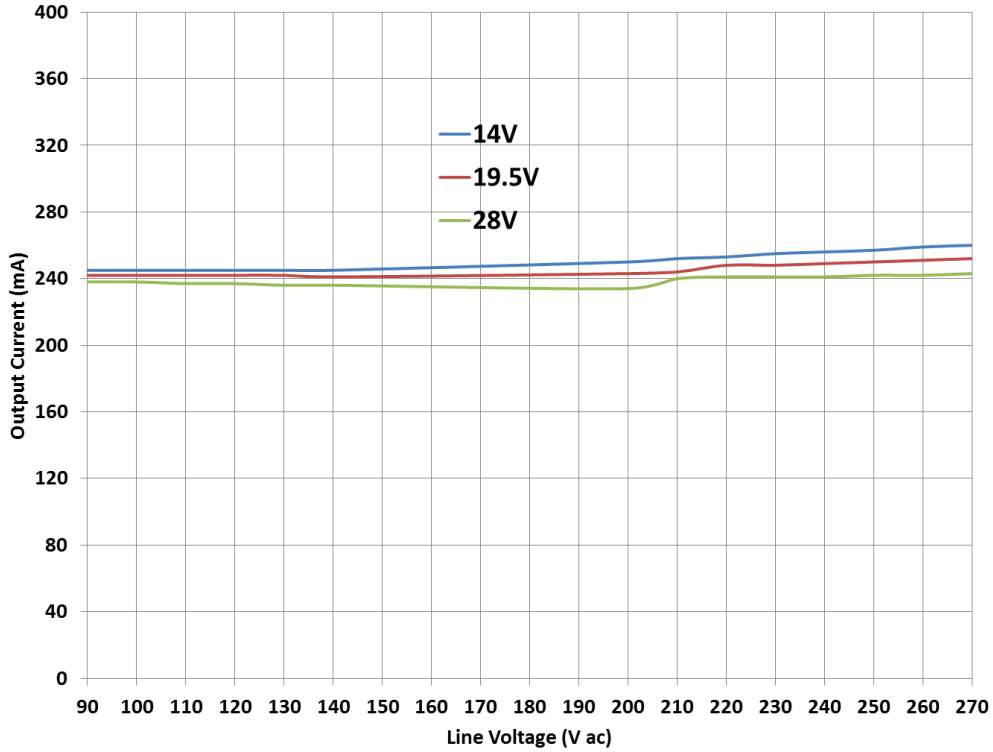


Figure 15. 70% Load Regulation over Line (NCL30185FLYG only)

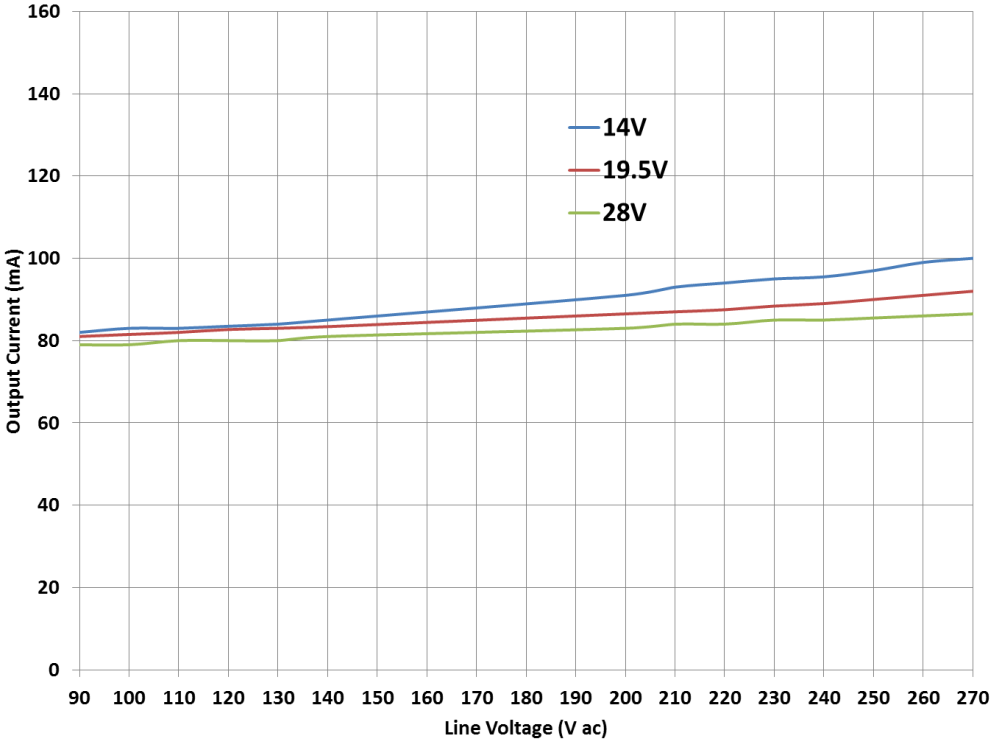


Figure 16. 25% Load Regulation over Line (NCL30185FLYG only)

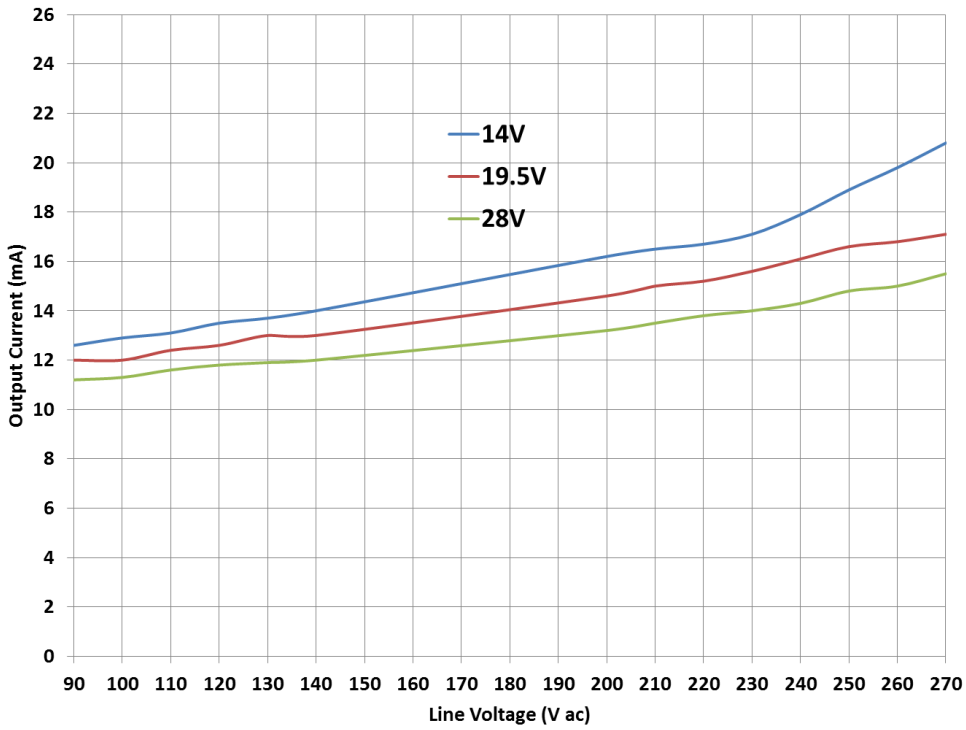


Figure 17. Minimum Load Regulation over Line (NCL30185FLYG only)

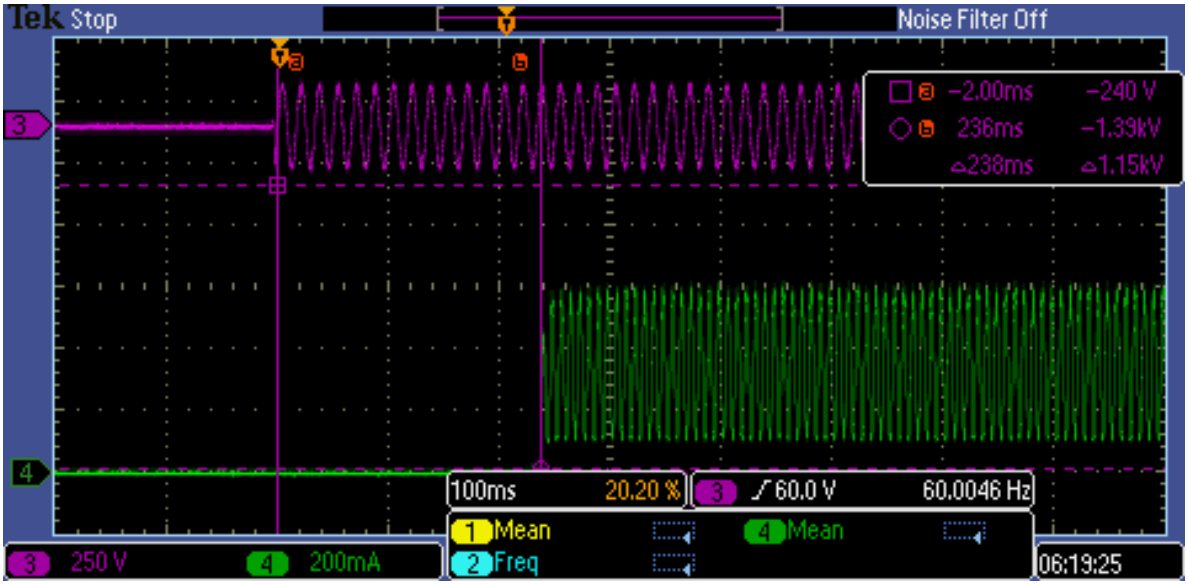


Figure 18. Start Up with AC Applied 120 V Maximum Load

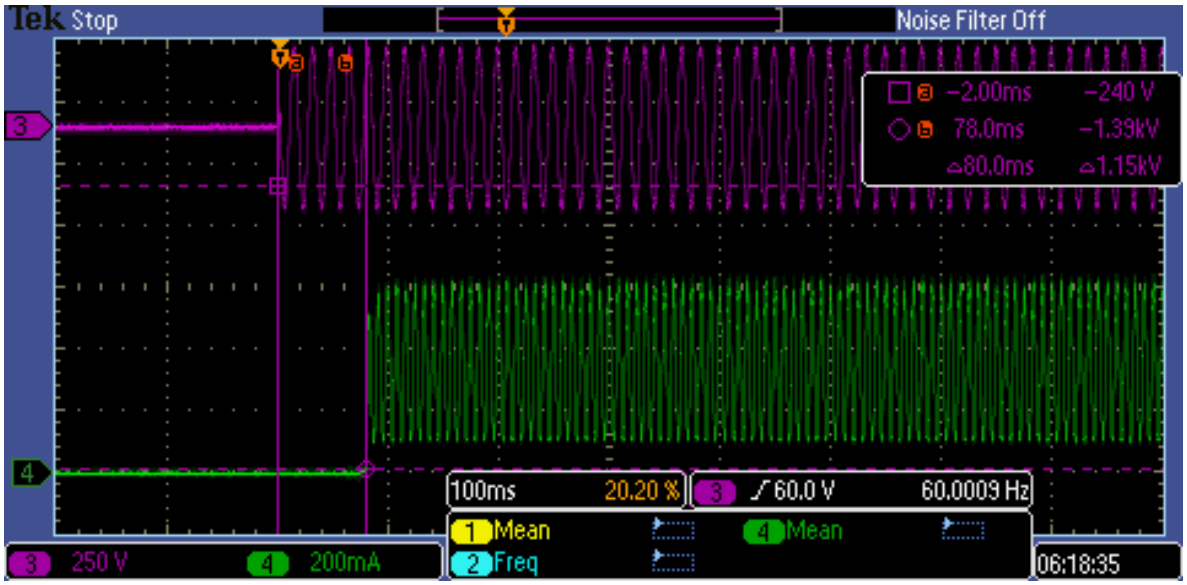


Figure 19. Start Up with AC Applied 230 V Maximum Load

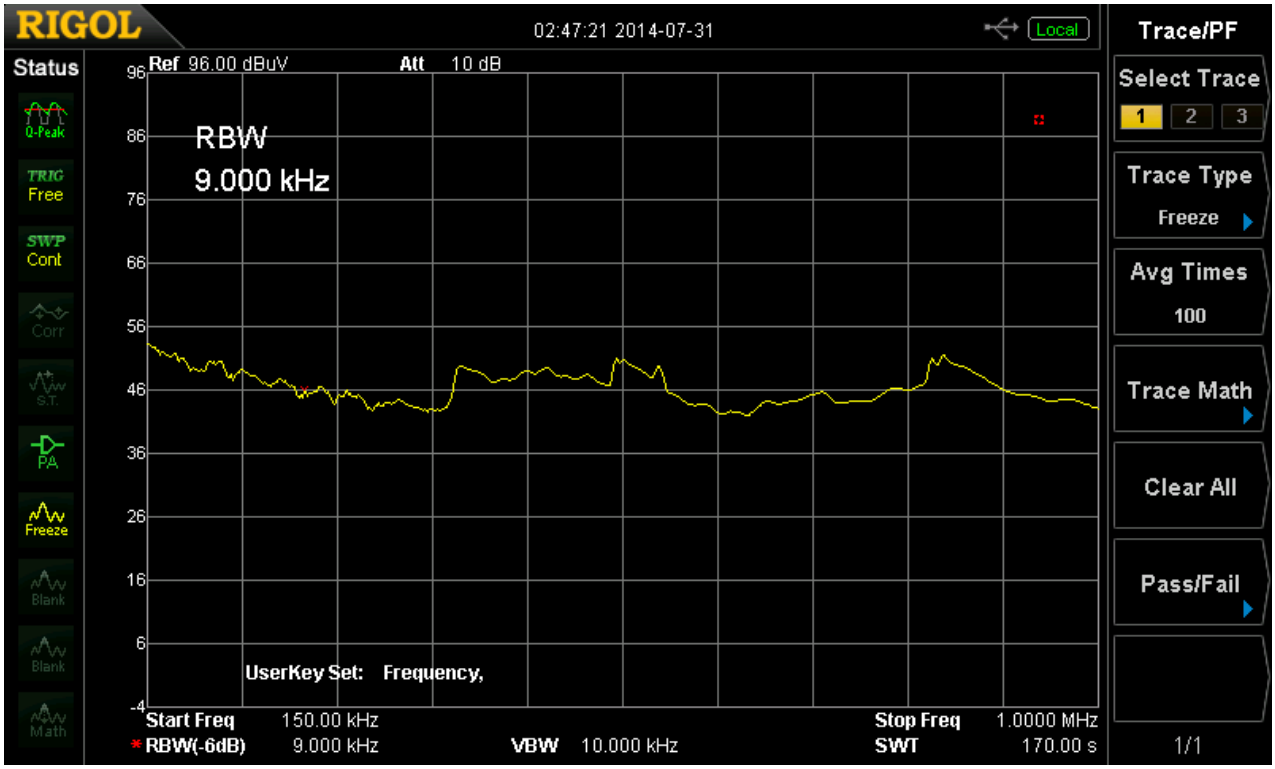


Figure 20. Conducted EMI Pre−compliance QP Data 150 kHz − 1 MHz

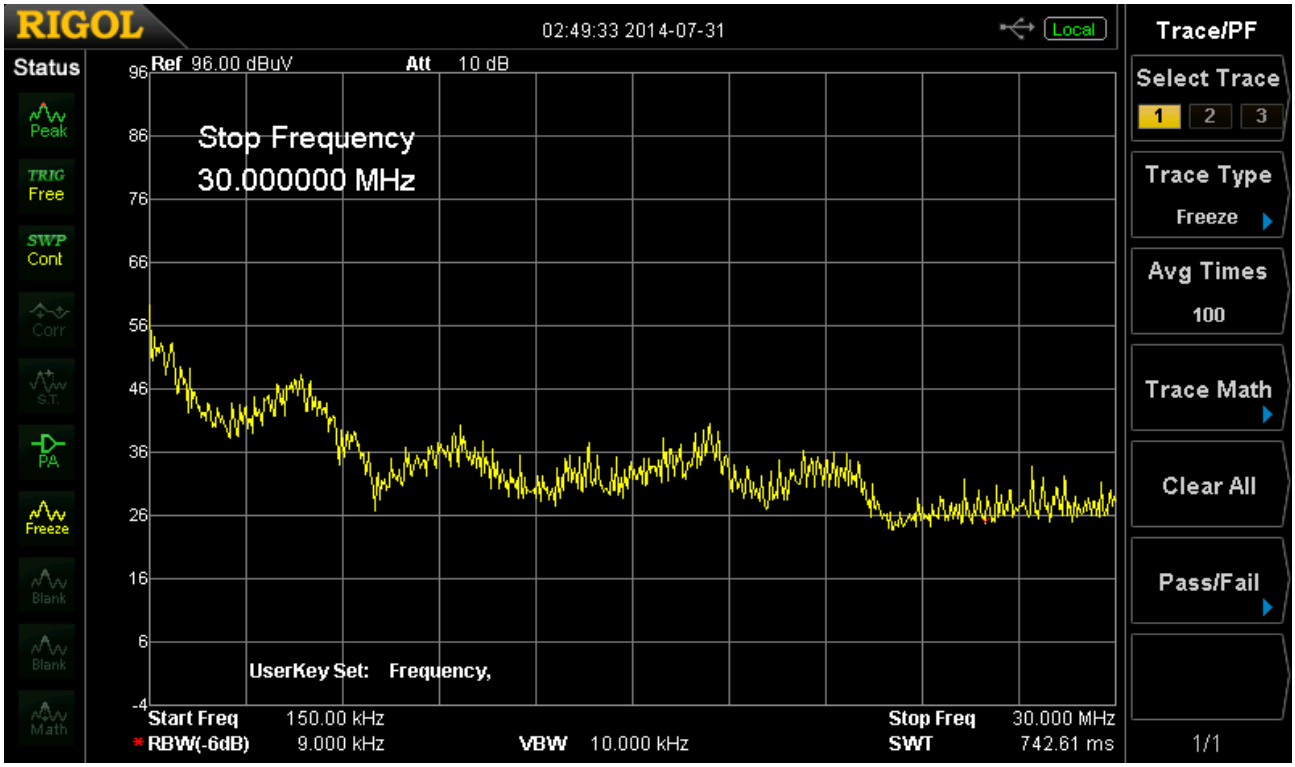


Figure 21. Conducted EMI Pre−compliance Peak Data 150 kHz − 30 MHz

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