# *PRODUCT SPECIFICATION*

**Customer :** _____

**Product Name :** Real Time Clock

**Part NO :** FRTC1338S

**Issue Date :** _____

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| Prepared | Checked | Customer Check |
|---|---|---|
| ChenTT | Zelig | |

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# 1 Features

- RTC Counts Seconds, Minutes, Hours, Date of the Month, Month, Day of the Week, and Year with Leap-Year Compensation Valid Up to 2100
- Support 3.3V operation
- 56-Byte Battery-Backed NV RAM for Data Storage
- I²C Serial Interface
- Programmable Square-Wave Output Signal
- Automatic Power-Fail Detect and Switch Circuitry
- Operating Temperature: -40 ~ 85° C

# 2 Applications

- Handhelds (GPS, POS Terminal)
- Consumer Electronics (Set-Top Box, Digital Recording, Network Appliance)
- Office Equipment (Fax/Printer, Copier)
- Medical (Glucometer, Medicine Dispenser)
- Telecommunications (Router, Switcher, Server)
- Other (Utility Meter, Vending Machine, Thermostat, Modem)

# 3 Typical application circuit

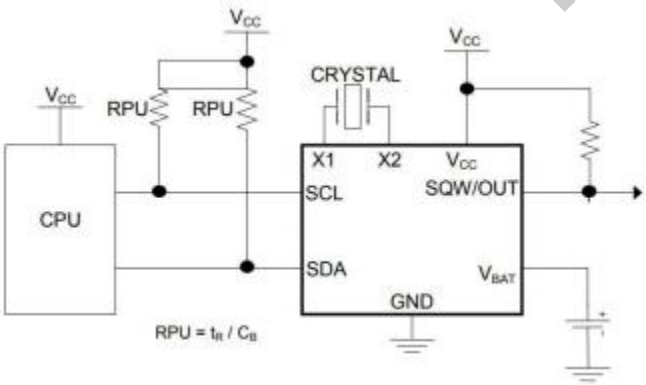



Figure 1 Typical application circuit

# 4 Description

The FRTC1338S is a low-power serial real-time clock (RTC) that integrates a full BCD (Binary-Coded Decimal) clock/calendar along with 56 bytes of non-volatile SRAM. Communication with the device is carried out via an I2C serial interface for address and data transfer.

The clock/calendar subsystem provides comprehensive timekeeping data, including seconds, minutes, hours, day, date, month, and year. The date is automatically adjusted at month-end to accommodate months with fewer than 31 days, with full leap-year correction applied as necessary. The time format is user-selectable, supporting either 24-hour mode or 12-hour mode with an AM/PM indicator.

Additionally, the FRTC1338S incorporates a built-in power-sense circuit that continuously monitors the primary supply voltage. Upon detection of a power failure, the device automatically switches to battery backup to preserve timekeeping and SRAM data.

# 5 Ordering Information:

| Ordering Code | Package | Package Description |
|---|---|---|
| FRTC1338S | | SOP-8 |

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# 6 Pin Configurations

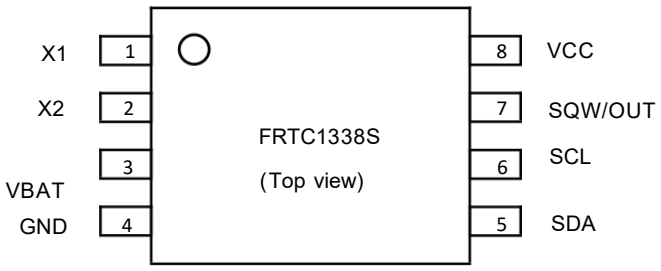



Figure 2 SOP-8 pin configuration (Top view)

| Pin Name | Pin No.<br>SOP-8/MSOP-8 | Description |
|---|---|---|
| X1 | 1 | Pin X1 can optionally be connected to an external 32.768kHz oscillator. Pin X2, is floated if an external oscillator is connected to pin X1. |
| X2 | 2 | |
| VBAT | 3 | +3V Battery Input. |
| GND | 4 | Ground. DC power is provided to the device on these pins. |
| SDA | 5 | Serial Data. Input/output pin for the I2C serial interface. It is open drain and requires an external pullup resistor. |
| SCL | 6 | Serial Clock. Used to synchronize data movement on the serial interface |
| SQW/OUT | 7 | Square-Wave/Output Driver. |
| VCC | 8 | Primary Power Supply. |

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# 7 Absolute Maximum Ratings

| Symbol | Parameter | MIN | TYP | MAX | Unit |
|---|---|---|---|---|---|
| $T_{store}$ | Storage Temperature | -55 | _ | +150 | ° C |
| $T_{op}$ | Operating Temperature Range | -40 | _ | +85 | ° C |
| $V_{IN}$ | Voltage Range on Any Pin Relative to Ground | -0.3 | _ | 6 | V |

**Note:**
Maximum ratings listed in this specification represent stress limits beyond which permanent damage to the device may occur. These values are intended as stress ratings only, and the device is not guaranteed to function under these or any other conditions exceeding those specified in the operational sections of this document. Prolonged exposure to absolute maximum rating conditions may adversely affect device reliability and long-term performance.

# 8 Recommended Operation Conditions

| Symbol | Parameter | CONDITIONS | MIN | TYP | MAX | Unit |
|---|---|---|---|---|---|---|
| VCC | Positive DC Supply Voltage | FRTC1338S | 2.97 | 3.3 | 3.63 | V |
| VIH | SCL/SDA input | | 0.7 x VCC | _ | VCC + 0.3 | V |
| VIL | SCL/SDA input | | -0.3 | _ | +0.3 x VCC | V |
| VPF | Power-Fail Voltage | FRTC1338S | 2.7 | 2.82 | 2.97 | V |
| VBAT | Battery Voltage*2 | | 1.3 | 3.0 | 3.7 | V |

**Note:**
1. Limits at -40° C are guaranteed by design and not production tested.
2. All voltages are referenced to ground

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# 9 Product Features

## 9.1 DC Electrical Characteristics

Unless otherwise specified, -40 ° C≤$T_A$≤ 85 ° C , ($V_{CC(MIN)}$ ≤$V_{CC}$≤ $V_{CC(MAX)}$ )*1

| Symbol | Parameter | Test Conditions*1 | | MIN | TYP | MAX | Unit |
|---|---|---|---|---|---|---|---|
| $V_{BAT}$ | Battery Voltage*2 | | | 1.3 | | 3.7 | V |
| $I_{LI}$ | Input Leakage | SCL only | | _ | _ | 1 | μA |
| $I_{LO}$ | I/O Leakage | SDA and SQW/OUT | | | _ | 1 | μA |
| $I_{OLSDA}$ | SDA Logic 0 Output | $V_{CC}$ > 2V; $V_{OL}$ = 0.4V | | _ | _ | 3 | mA |
| | | $V_{CC}$ < 2V; $V_{OL}$ = 0.2 $V_{CC}$ | | _ | _ | 3 | mA |
| $I_{OLSQW}$ | SQW/OUT Logic 0 Output | $V_{CC}$ > 2V; $V_{OL}$ = 0.4V | | _ | _ | 3 | mA |
| | | 1.71V < $V_{CC}$ < 2V; $V_{OL}$ = 0.2 $V_{CC}$ | | _ | _ | 3 | |
| | | 1.3V < $V_{CC}$ < 1.71V; $V_{OL}$ = 0.2 $V_{CC}$ | | _ | _ | 250 | mA |
| $I_{CCA}$ | Active Supply Current Supply Current | SCL clocking at max frequency = 400kHz | FRTC1338S | _ | 120 | 200 | μA |
| $I_{CCS}$ | Standby Current | Specified with the I2C bus inactive | FRTC1338S | _ | 85 | 125 | μA |
| $I_{BATLKG}$ | $V_{BAT}$ Leakage Current ($V_{CC}$ Active) | | | | 25 | 100 | nA |
| $I_{BATOSC1}$ | $V_{BAT}$ Current ($O_{SC}$ ON) | $V_{BAT}$ = 3.7V , SQW/OUT OFF*3 | | | 400 | 1200 | nA |
| $I_{BATOSC2}$ | $V_{BAT}$ Current ($O_{SC}$ ON) | $V_{BAT}$ = 3.7V , SQW/OUT ON (32kHz) *3 | | | 570 | 1400 | nA |
| $I_{BATDAT}$ | $V_{BAT}$ Data-Retention Current ($O_{SC}$ Off) | $V_{BAT}$ = 3.7V*2 | | | 10 | 100 | nA |

Note:
1. Limits at -40° C are guaranteed by design and not production tested.
2. All voltages are referenced to ground
3. A fast-mode device can be used in a standard-mode system, but the requirement tSU:DAT ≥ to 250ns must then be met.

This condition is automatically satisfied when the device does not stretch the low period of the SCL signal. In cases where the device does implement SCL low-period stretching, it must ensure that the next data bit is output to the SDA line at least tR MAX + tSU:DAT = 1000 + 250 = 1250 ns before the SCL line is released.

## 9.2 Crystal Specifications

| Symbol | Parameter | MIN | TYP | MAX | Units |
|---|---|---|---|---|---|
| $f_O$ | Nominal Frequency | | 32.768 | | kHZ |
| ESR | Series Resistance | | | 45 | kΩ |
| $C_L$ | Load Capacitance | | 12.5 | | pF |

Note:
1. The crystal, traces, and crystal input pins should be isolated from RF generating signals.

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# 9.3 AC Electrical characteristics

(TA = -40 ° C to +85 ° C) *1

| Symbol | Parameter | Test Conditions*1 | MIN | TYP | MAX | Unit |
|---|---|---|---|---|---|---|
| $f_{SCL}$ | SCL Clock Frequency | Fast mode | 100 | | 400 | kHz |
| | | Standard mode | | | 100 | kHz |
| $t_{BUF}$ | Bus Free Time Between STOP and START Condition | Fast mode | 1.3 | | | μs |
| | | Standard mode | 4.7 | | | |
| $t_{HD:STA}$ | Hold Time (Repeated) START Condition*2 | Fast mode | 0.6 | | | μs |
| | | Standard mode | 4.0 | | | |
| $t_{LOW}$ | LOW Period of SCL Clock | Fast mode | 1.3 | | | μs |
| | | Standard mode | 4.7 | | | |
| $t_{HIGH}$ | HIGH Period of SCL Clock | Fast mode | 0.6 | | | μs |
| | | Standard mode | 4.0 | | | |
| $t_{SU:STA}$ | Setup Time for Repeated START Condition | Fast mode | 0.6 | | | μs |
| | | Standard mode | 4.7 | | | |
| $t_{HD:DAT}$ | Data Hold Time*3/4 | Fast mode | 0 | | 0.9 | μs |
| | | Standard mode | 0 | | | |
| $t_{SU:DAT}$ | Data Setup Time*5 | Fast mode | 100 | | | ns |
| | | Standard mode | 250 | | | |
| $t_R$ | Rise Time of Both SDA and SCL Signals *6 | Fast mode | 20 + 0.1CB | | 300 | ns |
| | | Standard mode | 20 + 0.1CB | | 1000 | |
| $t_F$ | Fall Time of Both SDA and SCL Signals *6 | Fast mode | 20 + 0.1CB | | 300 | ns |
| | | Standard mode | 20 + 0.1CB | | 300 | |
| $t_{SU:STO}$ | Setup Time for STOP Condition | Fast mode | 0.6 | | | μs |
| | | Standard mode | 4.0 | | | |
| $C_B$ | Capacitive Load for Each Bus Line*6 | | | | 400 | pF |
| $C_{I/O}$ | I/O Capacitance (SDA, SCL) *7 | | | | 10 | pF |
| $t_{OSF}$ | Oscillator Stop Flag (OSF) Delay*8 | | | 100 | | ms |

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Note:

1. Temperature Limits: Specifications at -40° C are guaranteed by design and are not subject to production testing.
2. Clock Generation: The first clock pulse is generated after the specified period has elapsed.
3. SDA Hold Time Requirement: The device must internally provide a minimum hold time of 300 ns for the SDA signal, referenced to the VIHMIN of the SCL signal, in order to bridge the undefined region during the falling edge of SCL.
4. tHD:DAT Maximum Condition: The maximum tHD:DAT specification only needs to be satisfied when the device does not stretch the low period (tLOW) of the SCL signal.
5. Fast-Mode Device in Standard-Mode System: A fast-mode device may be used in a standard-mode system, provided that the tSU:DAT requirement of ≥ 250 ns is met. This condition is automatically satisfied if the device does not stretch the SCL low period. If SCL stretching is employed, the next data bit must be output to the SDA line at least tR MAX + tSU:DAT = 1000 + 250 = 1250 ns before the SCL line is released.
6. Bus Capacitance: CB represents the total capacitance of one bus line, measured in picofarads (pF).
7. Design Guarantee: Any specifications noted as "guaranteed by design" are verified through characterization and are not covered by production testing.
8. The parameter $t_{OSF}$ is the time period the oscillator must be stopped for the OSF flag to be set over the voltage range of

   $0.0V \leqslant V_{CC} \leqslant V_{CC\ MAX}$ and $1.3V \leqslant V_{BAT} \leqslant 3.7V$

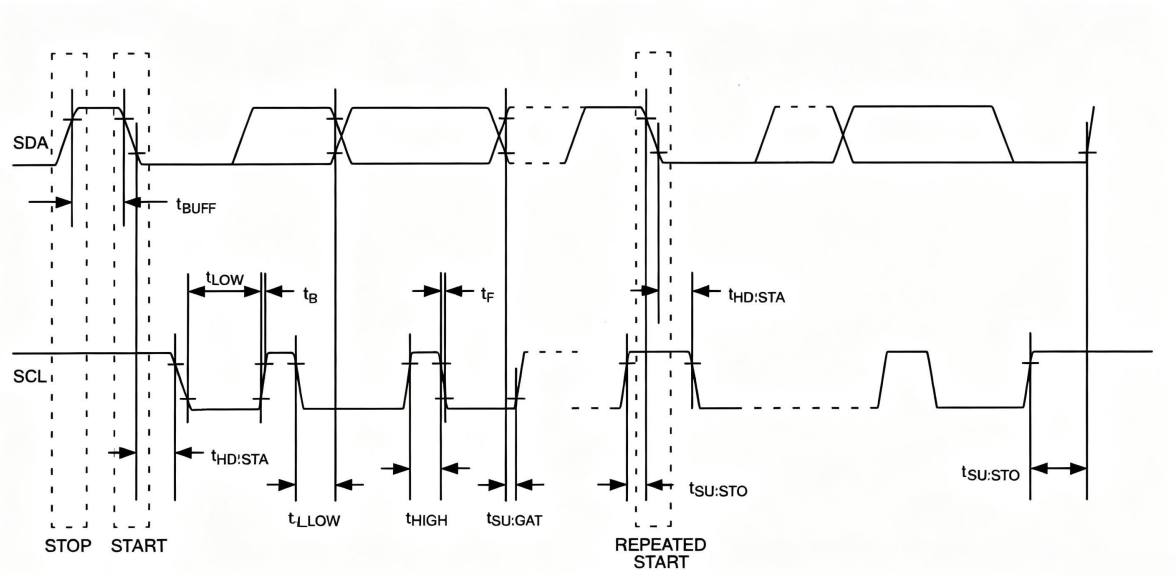



Figure 3 Timing Diagram

## 9.4 Power-Up/Power-Down Characteristics

(TA = -40 ° C to +85 ° C) *1

| Symbol | Parameter | Test Conditions*1 | MIN | TYP | MAX | Unit |
|---|---|---|---|---|---|---|
| $t_{REC}$ | Recovery at Power-Up*2 | | | | 2 | ms |
| $t_{VCCF}$ | $V_{CC}$ Fall Time | $V_{PF}$(MAX) to $V_{PF}$(MIN) | 300 | | | μs |
| $t_{VCCR}$ | $V_{CC}$ Rise Tim | $V_{PF}$(MIN) to $V_{PF}$(MAX) | 0 | | | μs |

Note:
1. Limits at -40° C are guaranteed by design and not production tested.
2. This delay applies only if the oscillator is enabled and running. If the oscillator is disabled or stopped, no power-up delay occurs.

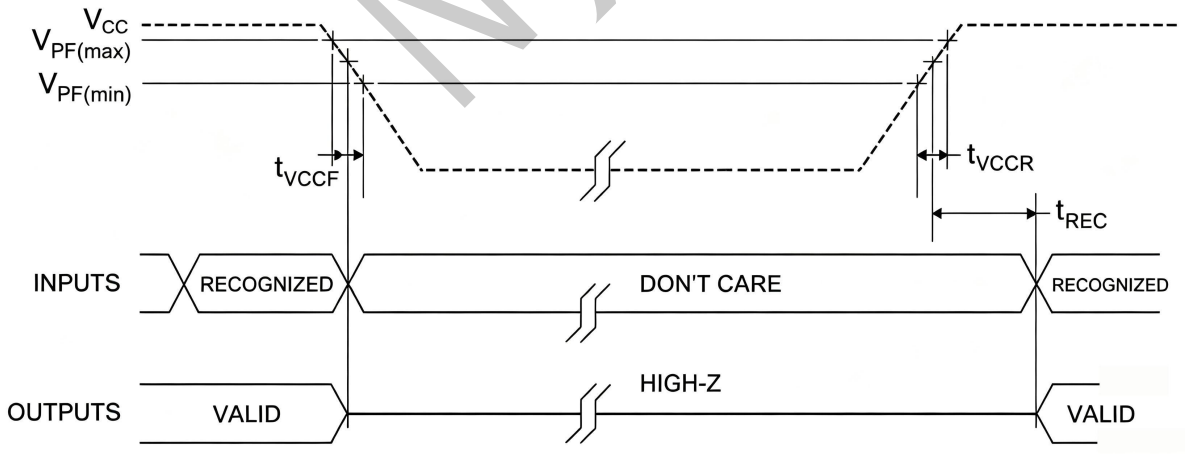



**Figure 4 Power-Up/Power-Down Timing**

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## 9.5 Functional Description

The FRTC1338S is a low-power serial real-time clock (RTC) that integrates a full BCD clock/calendar with 56 bytes of non-volatile SRAM. Communication with the host is carried out via an I²C serial interface for all address and data transfers. The clock/calendar subsystem provides comprehensive timekeeping information, including seconds, minutes, hours, day, date, month, and year. The date is automatically adjusted at month-end to accommodate months with fewer than 31 days, with full leap-year correction applied as necessary. The time format is user-selectable, supporting either 24-hour mode or 12-hour mode with an AM/PM indicator.

The device incorporates a built-in power-sense circuit that continuously monitors the primary supply voltage and automatically switches to battery backup upon detection of a power failure. The internal oscillator circuitry is optimized for operation with a crystal featuring a specified load capacitance (CL) of 12.5 pF. Pin X1 serves as the oscillator input and may optionally be driven by an external 32.768 kHz oscillator. When an external oscillator is connected to X1, the X2 pin (internal oscillator output) is left floating.

The FRTC1338S is equipped with a backup supply input (VBAT) designed for use with any standard 3V lithium cell or other suitable energy source. The VBAT voltage must be maintained within the specified minimum and maximum limits to ensure proper device operation. If a backup supply is not required, the VBAT pin must be connected to ground. When the primary supply (VCC) is within normal operating limits, the device is fully accessible for read and write operations. However, when a backup supply is connected and VCC drops below the power-fail threshold (VPF), read and write access is inhibited; nevertheless, the timekeeping function continues uninterrupted.

The SQW/OUT pin, when enabled via the SQWE bit set to logic 1, outputs one of four selectable square-wave frequencies: 1 Hz, 4 kHz, 8 kHz, or 32 kHz. This pin features an open-drain output stage and therefore requires an external pull-up resistor. The square-wave output function operates with either VCC or VBAT applied.

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# 10 Application Information

The FRTC1338S functions as a slave device on the serial bus. Bus access is initiated by issuing a START condition, followed by the device identification code and the appropriate data. Once access is established, subsequent registers may be accessed sequentially until a STOP condition is issued.

The device is fully accessible for both read and write operations when VCC is above the power-fail threshold (VPF). However, when VCC drops below VPF, the internal clock registers are blocked from any access. The power-switching logic operates as follows: if VPF is lower than VBAT, the device switches from VCC to VBAT when VCC falls below VPF. Conversely, if VPF is higher than VBAT, the switch occurs when VCC drops below VBAT. The registers are maintained from the VBAT supply until VCC is restored to normal operating levels. A block diagram illustrating the main functional elements of the FRTC1338S is provided for reference.

The oscillator is controlled by an enable bit located in the seconds register. Oscillator startup times are highly dependent on crystal characteristics, PC board leakage, and layout design. High equivalent series resistance (ESR) and excessive capacitive loads are the primary contributors to extended startup durations. With a crystal meeting the recommended specifications and proper PCB layout, the oscillator typically starts within 1 second.

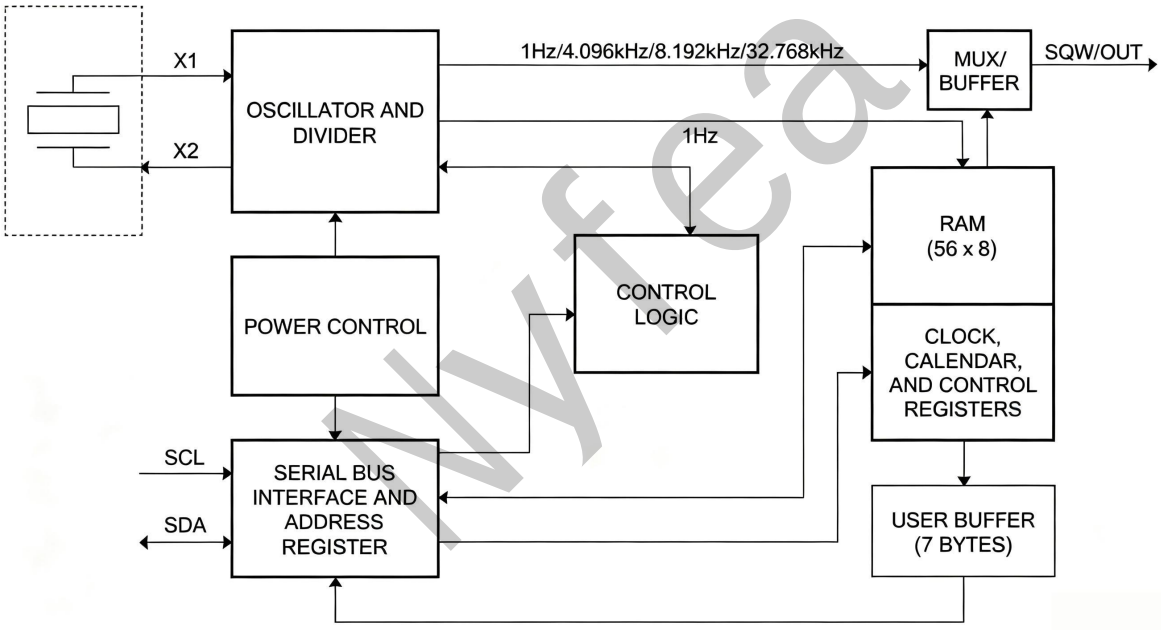



Figure 5 Block Diagram

## 10.1 Oscillator Circuit

The FRTC1338S is designed to operate with an external 32.768 kHz quartz crystal. The internal oscillator circuit is self-contained and does not require any external resistors or capacitors for proper operation. A functional schematic of the oscillator circuit, including the internal bias network, is illustrated in the accompanying figure.

When a crystal with the specified characteristics is used, the oscillator typically achieves stable operation within less than 1 second after power-up.

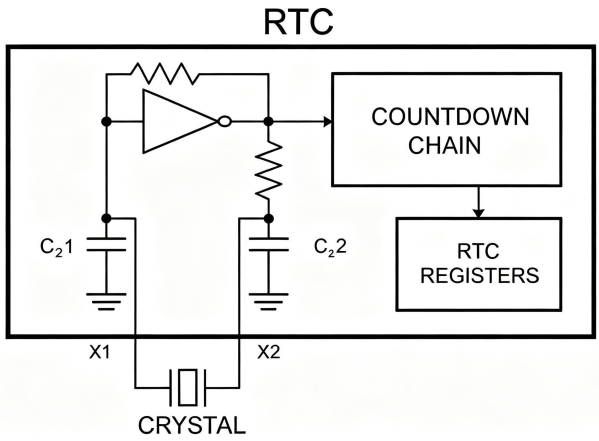



Figure 6 Oscillator Circuit Showing Internal Bias Network

## 10.2 Clock Accuracy

The overall timekeeping accuracy of the clock is influenced by several factors. Primary among these are the precision of the external crystal itself and the degree to which the capacitive load presented by the oscillator circuit matches the load capacitance for which the crystal was trimmed. Any mismatch between these capacitances will introduce frequency deviation and degrade accuracy. Additionally, temperature-induced frequency drift of the crystal contributes further error. External circuit noise coupled into the oscillator circuitry may also cause the clock to run fast.

## 10.3 RTCAnd RAM Address Map

The RTC registers and the control register are mapped to address locations 00h through 07h, while the RAM registers occupy address locations 08h through 3Fh. During a multibyte access, when the register pointer reaches 3Fh (the end of the RAM address space), it wraps around to location 00h (the beginning of the clock register space).

Upon any of the following events—an I²C START condition, a STOP condition, or the register pointer incrementing to address 00h—the current time and date values are transferred from the main registers to a secondary set of registers. The time and date information read during a multibyte data transfer is sourced from these secondary registers, allowing the main clock to continue running uninterrupted. This double-buffering mechanism eliminates the need to re-read the registers in the event of an update to the main registers occurring during a read operation.

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## 10.4 Clock And Calendar

The time and calendar information is obtained by reading the appropriate register bytes, as illustrated in the RTC and RAM Address Map figure. Similarly, the time and calendar are set or initialized by writing to the corresponding register bytes. All time and calendar register contents are stored in BCD format.

Bit 7 of Register 0 is the Clock Halt (CH) bit. When this bit is set to logic 1, the oscillator is disabled; when cleared to logic 0, the oscillator is enabled. The clock may be halted whenever timekeeping functions are not required, which reduces VBAT current consumption.

The day-of-week register increments at midnight. The values assigned to each day of the week are user-defined but must follow a sequential order—for example, if 1 represents Sunday, then 2 must represent Monday, and so forth. Illogical or non-sequential time and date entries may result in undefined operation.

To prevent errors during internal register updates, secondary (user) buffers are employed when reading or writing the time and date registers. When reading, these user buffers are synchronized to the internal registers upon any START or STOP condition, as well as when the register pointer rolls over to 00h. The countdown chain is reset whenever the seconds register is written; write transfers occur on the acknowledge from the FRTC1338S. Once the countdown chain is reset, the remaining time and date registers must be written within 1 second to avoid rollover issues.

The 1 Hz square-wave output, if enabled, transitions high 500 ms after the seconds data transfer, provided the oscillator is already running.

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**Note that the initial power-on state of all registers, unless otherwise specified, is not defined. Therefore, it is important to enable the oscillator (CH = 0) during initial configuration.**

The FRTC1338S supports both 12-hour and 24-hour timekeeping formats. Bit 6 of the hours register serves as the mode-select bit: when set to logic 1, the 12-hour mode is selected; when cleared to logic 0, the 24-hour mode is active. In 12-hour mode, bit 5 functions as the AM/PM indicator, with logic 1 representing PM and logic 0 representing AM. In 24-hour mode, bit 5 acts as the second 10-hour bit, extending the range to 20－23 hours. Whenever the 12/24-hour mode selection is changed, the hours register must be re-initialized to the new format to ensure proper timekeeping.

On an I²C START condition, the current time is transferred from the main registers to a secondary set of registers. All time information read during a transaction is sourced from these secondary registers, while the main clock continues to run independently. This double-buffering scheme eliminates the need to re-read the registers in the event that the main registers update during a read operation.

## 10.4.1 RTC and RAM Address Map

| Address | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Function | Range |
|---|---|---|---|---|---|---|---|---|---|---|
| 00H | CH | 10 Seconds | | | Seconds | | | | Seconds | 00-59 |
| 01H | 0 | 10 Minutes | | | Minutes | | | | Minutes | 00-59 |
| 02H | 0 | 12/24 | AM/ PM<br>10 Hour | 10 Hour | Hour | | | | Hour | 1-12<br>+AM/ PM<br>00-23 |
| 03H | 0 | 0 | 0 | 0 | 0 | Day | | | Day | 1-7 |
| 04H | 0 | 0 | 10 Date | | Date | | | | Date | 01-31 |
| 05H | 0 | 0 | 0 | 10 Month | Month | | | | Month | 01-12 |
| 06H | 10 Year | | | | Year | | | | Year | 00-99 |
| 07H | OUT | 0 | OSF | SQWE | 0 | 0 | RS1 | RS0 | Control | |
| 08H-3FH | | | | | | | | | RAM 56 x 8 | 00H-FFH |

**Note**: Bits listed as “0” always read as a 0

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## 10.4.2 Control Register (07h)

The control register controls the operation of the SQW/OUT pin and provides oscillator status.

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| OUT | 0 | OSF | SQWE | 0 | 0 | RS1 | RS0 |

**Bit 7: Output Control (OUT).** Controls the output level of the SQW/OUT pin when the square-wave output is disabled. If SQWE = 0, the logic level on the SQW/OUT pin is 1 if OUT = 1; it is 0 if OUT = 0.

**Bit 5: Oscillator Stop Flag (OSF)** A logic 1 in this bit indicates that the oscillator has either stopped or experienced a stoppage at some point in the past, and may be used as an indicator for assessing the validity of clock and calendar data. This bit is edge-triggered and is set to logic 1 when the internal circuitry detects that the oscillator has transitioned from a normal running state to a stopped condition. Conditions that may cause the OSF bit to be set include, but are not limited to, the following:

1) The first time power is applied.
2) The voltage present on $V_{CC}$ and $V_{BAT}$ are insufficient to support oscillation.
3) The CH bit is set to 1, disabling the oscillator.
4) External influences on the crystal (i.e., noise, leakage, etc.).

This bit remains at logic 1 until written to logic 0. This bit can only be written to logic 0. Attempting to write OSF to logic 1 leaves the value unchanged.

**Bit 4: Square-Wave Enable (SQWE).** When this bit is set to logic 1, the square-wave output is enabled and operates with either VCC or VBAT applied. The output frequency is determined by the settings of the RS0 and RS1 bits.

**Bits 1 and 0: Rate Select (RS1 and RS0).** These bits control the output frequency of the square-wave signal when the square-wave output is enabled. The selectable frequencies are listed in the table below, as determined by the RS0 and RS1 bit settings.

**Square-Wave Output Frequency**

| RS1 | RS0 | SQW Output Frequency |
|---|---|---|
| 0 | 0 | 1HZ |
| 0 | 1 | 4.096kHz |
| 1 | 0 | 8.192kHz |
| 1 | 1 | 32.768kHz |

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# 11 I2C Serial Data Bus

The FRTC1338S supports the I²C serial communication protocol. On the I²C bus, any device that transmits data onto the bus is defined as a transmitter, while any device that receives data is defined as a receiver. The device that initiates and controls the message transaction is referred to as the master; the devices that respond to the master's commands are referred to as slaves.

The bus must be controlled by a master device, which is responsible for generating the serial clock (SCL), managing bus access, and generating both START and STOP conditions. The FRTC1338S operates exclusively as a slave device on the I²C bus.

The I²C bus specification defines two speed modes: standard mode (100 kHz clock cycle rate) and fast mode (400 kHz clock cycle rate). The FRTC1338S is fully compatible with both operating modes. All bus connections are made through the open-drain SDA and SCL I/O lines.

The following bus protocol has been defined (Figure: Data Transfer on I2C Serial Bus).

1) Data transfer can be initiated only when the bus is not busy.

During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH are interpreted as control signals.

Accordingly , the following bus conditions have been defined:

**Bus not busy**: Both data and clock lines remain HIGH.

**Start data transfer**: A change in the state of the data line, from HIGH to LOW, while the clock is HIGH, defines a START condition .

**Stop data transfer**: A change in the state of the data line, from LOW to HIGH, while the clock line is HIGH, defines the STOP condition.

**Data valid:** Following a START condition, the state of the SDA line is considered valid data when it remains stable throughout the HIGH period of the SCL clock signal. Any changes to the data line must occur while the clock signal is LOW. Each data bit corresponds to one clock pulse.

Every data transfer is initiated by a START condition and terminated by a STOP condition. The number of data bytes transmitted between START and STOP is not fixed and is determined by the master device. Data is transferred on a byte-wide basis, with each byte followed by a ninth acknowledge bit generated by the receiver.

**Acknowledge:** Each receiving device , when addressed, is obliged to generate an acknowledge after the reception of each byte . The master device must generate an extra clock pulse that is associated with this acknowledge bit.

A device that acknowledges must pull the SDA line low during the acknowledge clock pulse, ensuring that SDA remains stable at a logic-low level throughout the entire high period of the acknowledge-related clock pulse. Proper setup and hold times must be observed to guarantee reliable ACK detection.

To signal the end of a data transfer, the master must not generate an acknowledge bit (i.e., it must issue a NACK) on the last byte clocked out from the slave. In this case, the slave must release the SDA line and leave it high, enabling the master to generate a STOP condition and terminate the transaction.

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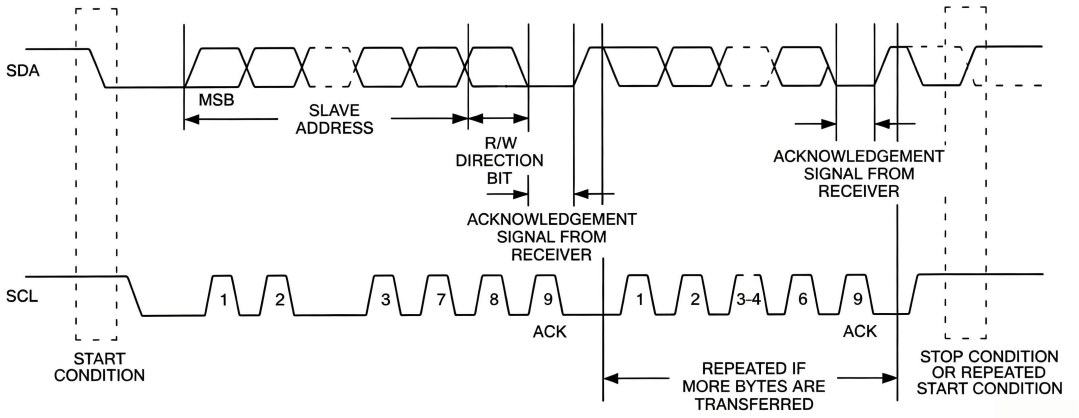



Figure 7 Data Transfer on I2C Serial Bus

Depending upon the state of the R/W bit, two types of data transfer are possible:

1) **Data transfer from a master transmitter to a slave receiver.** The master initiates the transfer by transmitting the first byte, which contains the slave address. This is followed by a sequence of data bytes. The slave returns an acknowledge bit after each byte it receives. Data is transmitted with the most significant bit (MSB) first.

2) **Data transfer from a slave transmitter to a master receiver.** The master initiates the transfer by transmitting the first byte, which contains the slave address. The slave then returns an acknowledge bit, after which it begins transmitting a number of data bytes. The master returns an acknowledge bit after every received byte except the last one; upon receiving the final byte, the master issues a not-acknowledge (NACK) to signal the end of the data transfer.

The master device is responsible for generating all serial clock pulses, as well as the START and STOP conditions. A transfer may be terminated either with a STOP condition or with a repeated START condition. Since a repeated START condition also serves as the beginning of the next serial transfer, the bus is not released between transactions. All data is transferred with the most significant bit (MSB) first.

The FRTC1338S can operate in the following two modes:

1) **Slave receiver mode (write mode):** Serial data and clock are received through the SDA and SCL lines, respectively. An acknowledge bit is transmitted by the receiver after each byte is received. START and STOP conditions are recognized as the beginning and end of a serial transfer.

Address recognition is performed by the hardware after the reception of the slave address and the direction bit (R/W), as illustrated in Figure: Data Write. The slave address byte is the first byte received after the master generates a START condition. This byte contains the 7-bit FRTC1338S address—1101000—followed by the direction bit (R/W), which is set to 0 for a write operation.

After receiving and decoding the slave address byte, the FRTC1338S outputs an acknowledge on the SDA line. Once the slave acknowledges the address and write bit, the master transmits a register address to the FRTC1338S, which sets the internal register pointer. The FRTC1338S acknowledges this transfer as well.

The master may then transmit zero or more bytes of data, with the FRTC1338S acknowledging each byte received. The register pointer increments automatically after each data byte is transferred. The master generates a STOP condition to terminate the data write operation..

2) **Slave transmitter mode (read mode):** The first byte is received and handled in the same manner as in the slave receiver mode. However, in this mode, the direction bit (R/W) indicates that the transfer direction is reversed. The FRTC1338S transmits serial data on SDA while the serial clock is input on SCL.

START and STOP conditions are recognized as the beginning and end of a serial transfer, as illustrated in Figure: Data Read. The slave address byte is the first byte received after the master generates the START condition.

The slave address byte contains the 7-bit FRTC1338S address—1101000—followed by the direction bit (R/W), which is set to 1 for a read operation. After receiving and decoding the slave address byte.,

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the slave outputs an acknowledge on the SDA line. The FRTC1338S then starts transmitting data using the register address pointed to by the register pointer. If the register pointer is not set before the initiation of a read mode, the first address that is read is the last one stored in the register pointer. The register pointer is incremented after each byte is transferred. The FRTC1338S must receive a “not acknowledge ” to end a read.

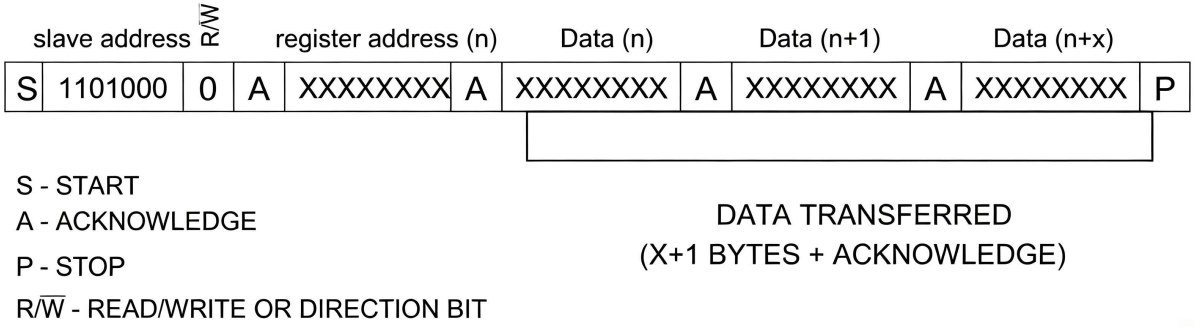



Figure: Data Write—Slave Receiver Mode

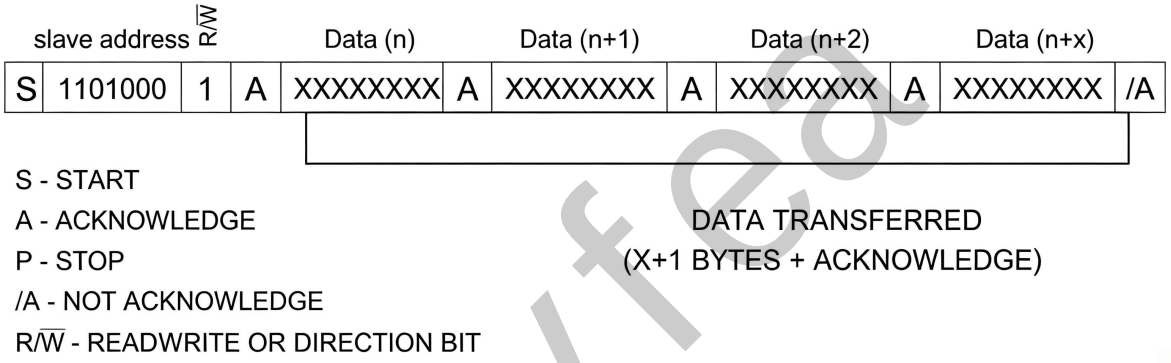



Figure: Data Read—Slave Transmitter Mode

# 12 Handling, PC Board Layout, And Assembly

The FRTC1338S package incorporates a quartz tuning-fork crystal. While pick-and-place equipment may be used for assembly, precautions must be taken to avoid excessive mechanical shocks that could damage the crystal. Ultrasonic cleaning should be avoided to prevent potential crystal damage.

For PCB layout, it is recommended to avoid routing signal traces directly under the package unless a ground plane is placed between the package and the signal lines. All No Connect (N.C.) pins must be connected to ground.

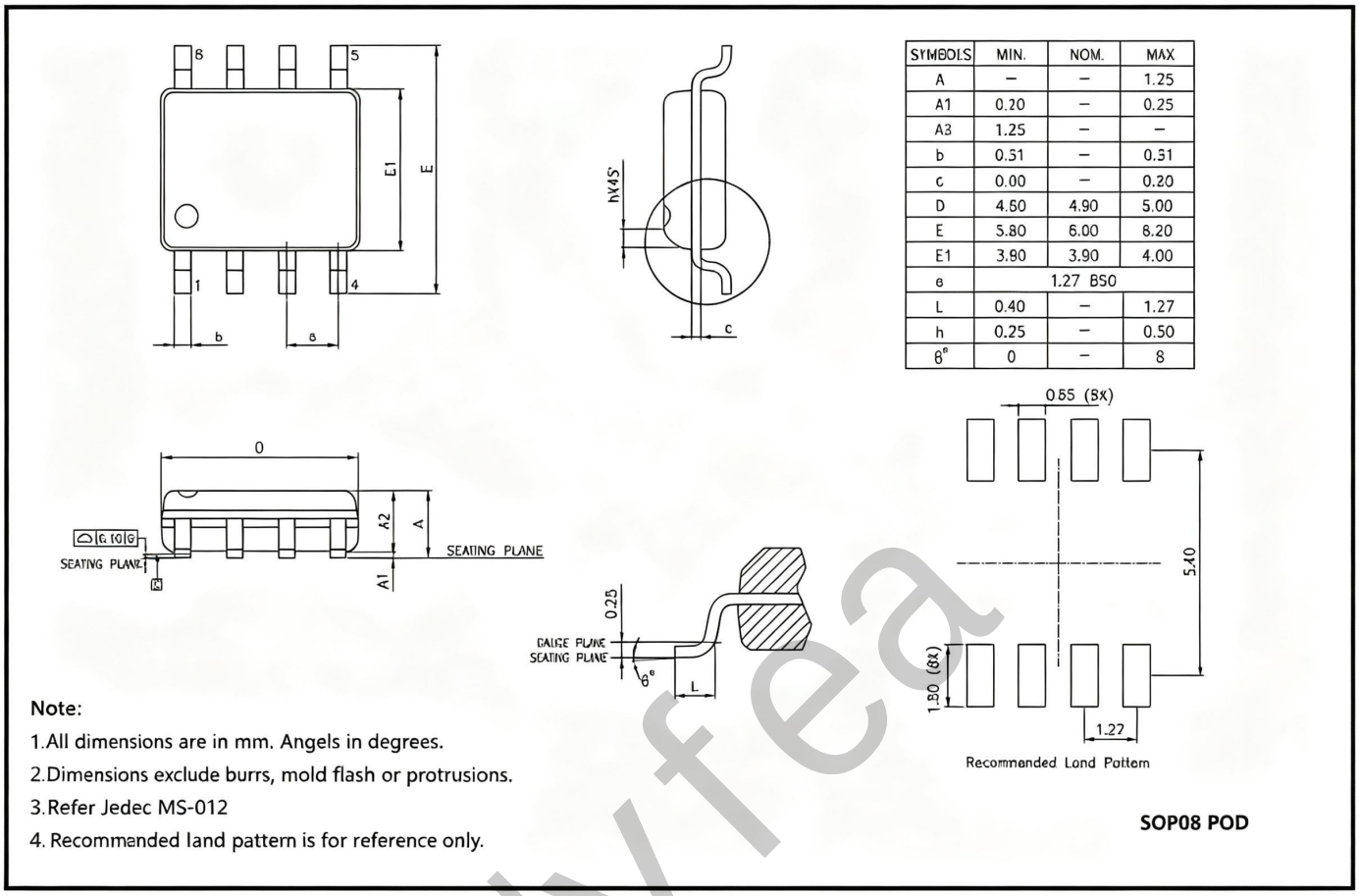
The SO package may be reflowed provided that the peak temperature does not exceed 240° C. The duration at peak reflow temperature (≥230° C) should not exceed 10 seconds, and the total time above 200° C should be limited to 40 seconds maximum (30 seconds nominal). Exposure to reflow is restricted to a maximum of two cycles.

Moisture-sensitive packages are shipped from the factory in dry-packed condition. The handling instructions printed on the package label must be followed to prevent damage during the reflow process. For moisture-sensitive device (MSD) classification and handling requirements, refer to the IPC/JEDEC J-STD-020B standard.

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# 13 Package Information

FRTC1338S SOP-8 Package




| SYMBOLS | MIN. | NOM. | MAX |
|---|---|---|---|
| A | – | – | 1.25 |
| A1 | 0.20 | – | 0.25 |
| A3 | 1.25 | – | – |
| b | 0.31 | – | 0.31 |
| c | 0.00 | – | 0.20 |
| D | 4.50 | 4.90 | 5.00 |
| E | 5.80 | 6.00 | 6.20 |
| E1 | 3.90 | 3.90 | 4.00 |
| e | 1.27 BSC | | |
| L | 0.40 | – | 1.27 |
| h | 0.25 | – | 0.50 |
| θ° | 0 | – | 8 |

**Note:**

1.All dimensions are in mm. Angels in degrees.

2.Dimensions exclude burrs, mold flash or protrusions.

3.Refer Jedec MS-012

4. Recommanded land pattern is for reference only.

**SOP08 POD**

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