钍地半导体
Tudi Semiconductor

Product Specification

TUDI-ADM488/489

Full-Duplex, Low Power, Slew Rate Limited, EIA RS-485 Transceivers

网址 www.sztdbdt.com

用芯智造·卓越品质

semiconductor device manufacturer

- Design
- research and development
- production
- and sales

Features

- Meets EIA RS-485 and RS-422 standards
- 250 kbps data rate
- Single 5 V ± 10% supply
- 7 V to +12 V bus common-mode range
- 12 kΩ input impedance
- 2 kV EFT protection meets IEC1000-4-4
- High EM immunity meets IEC1000-4-3
- Reduced slew rate for low EM interference
- Short-circuit protection
- Excellent noise immunity

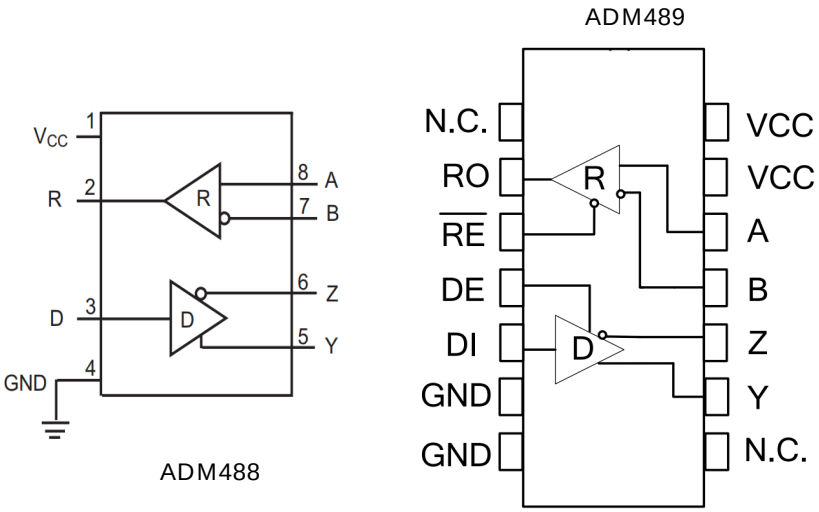


Figure 1 Pin diagram

Description

The ADM488 and ADM489 are low power differential line transceivers for multipoint bus transmission line communications. They used for balanced data transmission and are compliant with the Electronic Industries Association (EIA) RS-485 and RS-422 standards. Both products contain a differential line and a differential line receiver, making them suitable for full-duplex data transmission. The ADM489 includes an additional receiver and driver enable control. The input impedance is12 kΩ, allowing up to 32 transceivers to be connected to the bus. The ADM488/ADM489 are powered from single 5 V ±10% supply. Excessive power dissipation caused by bus contention or output short circuit is prevented by thermal shutdown circuitry. This feature, in the of a fault condition, detects a temperature rise in the internal driver circuitry and forces the driver outputs into a high -impedance state. The receiver contains a fault-safe that drives the output to a logic high if the input is not connected (floating). The ADM488/ADM489 are fully specified over the temperature range and are available in PDIP, SOIC packages.

Applications

- Low power RS-485 and RS-422 systems
- DTE-DCE interface
- Packet switching
- Local area networks
- Data concentration
- Data multiplexers
- Integrated services digital network (ISDN)

ADM489 Pin description

Pin number	Pin name	Pin function
1	NC	No internal connections required
2	RO	Receiver output.When RE is low,the RO output is high if A-B is ≥-10mV,and low if A-B is≤-200mV.
3	/RE	Receiver output enable control.When/RE is low,the receiver output is enabled and RO is active;when/REis high,the receiver output is disabled and RO is in high-impedance state.When RE is at a high level and DE is at a low level,the device enters low-power shutdown mode
4	DE	The driver output enables the control.When DE is at high level, the driver outputs effectively;when DE is low,it outputs high-impedance state.When/RE is high and DE is low,the device enters low-power shutdown mode.
5	DI	DI driver input.When DE is high,the low level on DI makes the in-phase output A of the driver low and the in-phase output B high;the high levelon DI makes the in-phase output high and the in-phase output Blow.
6	GND	Landing
7	GND	Landing
8	NC	No internal connections required
9	Y	Driver in-phase output terminal
10	Z	Driver inverting output
11	B	Receiver inverting input
12	A	Receiver in phase input
13	VCC	This pin can be connected to power or left unconnec-ted
14	VCC	Power connection

ADM488Pin description

Pin number	Pin name	Pin function
1	VCC	Power supply:4.5V≤VCC≤5.5V
2	R	Receiver output.
3	D	Driver Input
4	GND	Landing
5	Y	Driver in-phase output terminal
6	Z	Driver inverting output
7	B	Receiver inverting input
8	A	Receiver in-phase input

Additional description

Introduction
The 488/489 is a full-duplex high-speed transceiver for RS-485/RS-42 communication,containing a driver and a receiver.It has fail-safe,overvoltage protection,and overcurrent protection.The 488/489 achieves error-free transmission up to 250Kbps.
fail-safe
The 488/489 guarantees a logic high receiver output if the receiver input is short-circuited or open-circuited,or drivers connected to the terminated transmission line are disabled (idle).This is achieved by setting the receiver input thresholds to -10mV and -20mV, respectively.RO is logic high if the differential receiver input voltage(A-B)≥-10mV,and RO is logic low the voltage(A-B)≤-200mV.Logic high with a minimum noise margin of 50mV can be realized depending the receiver thresholds.The-10mV to -200mV threshold voltage is in accordance with the EIA/TIA-485 of±200mV.
32 transceivers on the bus
The input impedance of the standard RS485 receiver is 12kΩ(1 unit load),and the standard driver can drive to 32 unit loads.The receiver of the 488/489 transceiver has an input impedance of 1/8 unit load (96kΩ,allowing up to 32 transceivers to be connected in parallel on the samecommunication bus.These devices can be combined arbitrarily,or combined with other485 transceivers,as long as the total load does not exceed 32 unit loads,they can be connected to the same bus.
Drive output protection
Protection against excessive output current and dissipation by fault or bus contention is provided by overcurrent and overvoltage protection mechanisms,with fast short-circuit throughout the common-mode voltage range(see Typical Operating Characteristics).

Extreme parameter

Parameter	Symbol	Unit	size
Continuous power consumption	SOP	mW	600
	DIP	mW	700
Power supply voltage	VCC	V	+7
working temperature range		℃	-40~85
Storage temperature range		℃	-60~150
Welding temperature range		℃	300
Control port voltage	DI	V	-0.3~VCC+0.3
Bus side input voltage	A、B	V	-8~13
Receiver output voltage	RO	V	-0.3~VCC+0.3

The maximum limit parameters are values beyond which the device can be damaged in an irreversible manner. Operation of the device under these conditions is not intended to be normal and may affect the reliability of the device if operated continuously at the maximum rated limit. All voltages are referenced to ground.

ESD Protect						
Parameter	symbol	Test condition	Minimum	Typical case	Maximum	Unit
A、B、Y、Z		Human bodymodel		±15		KV
Other ports		Human bodymodel		±6		KV

Receiver Switching Characteris-tics						
Parameter	symbol	Test condition	Minimum	Typical case	Maximum	Unit
Acceptor	tRPLH	See Figure 7 and Figure 8	20	60	90	ns
Input to output propag-ation delay from low to high		V≥2.0V;risingand falling edgetime ViD≤15ns				
The propagation delay from receiverinput to output is from high to low	tRPHL		20	60	90	ns
|tRPLH-tRPHLl	tsKEW2			7	10	ns
Enable low time out	tRPZL	CL=15pF SeeFigures 7 and 8		20	50	ns
Enable to output high time	tRPZH	CL=15pF SeeFigures 7 and 8		20	50	ns
Time from output low to disable	tpRLZ	CL=15pF SeeFigures 7 and 8		20	45	ns
Time from output high to disable	tpRHZ	CL=15pF SeeFigures 7 and 8		20	45	ns
Off stateEnable to output high time	tRPSH	CL=15pF SeeFigures 7 and 8		200	1400	ns
Off stateEnable low time out	tRPSL	CL=15pF SeeFigures 7 and 8		200	1400	ns
Time to turn off	tsHDN	NOTE2	80		300	ns

(If not otherwise, VCC=3V~5.5V, Temp = TMIN ~ TMAX, typical value at Temp = 25) NOTE 1:? VO D and? VOC is the change in VOD and VOC amplitude caused when the DI state of the input signal changes, respectively.

DC electrical characteristics of thedriver						
Parameter	symbol	Test condition	Minimum	Typical case	Maximum	Unit
Driver differential output (non-loaded)	VoD_1			4.5	VCC	V
Drive differential output	VoD_2	graph 2,RL=27Ω	1.5	2.3	VCC	V
		graph 2,RL=50Ω	2	2.8	VCC	
Variation in the amplitude of the output voltage (NOTE1)	△VoD	graph 2,RL=27Ω			0.2	V
Output common mode voltage	Voc	graph 2,RL=27Ω			3	V
Amplitude Variation of Common Mode Output Voltage(NOTE1)	△Voc	graph 2,RL=27Ω			0.2	V
High-level input	VH	DI	2.0			V
Low level input	Vπ	DI			0.8	V
Logic input current	IN1	DI	-2		2	uA
Output the current during ashort circuit,with high short-circuit	$IosD_1$	Short circuit to OV~12V	35		250	mA
Output the current during ashort circuit,down to low	$IosD_2$	Short circuit to-7V~0V	-250		-35	mA

(If not otherwise, VCC=3V~5.5V, Temp = TMIN ~ TMAX, typical value at Temp = 25) NOTE 1:? VO D and? VOC is the change in VOD and VOC amplitude caused when the DI state of the input signal changes, respectively.

drive switch characteristics						
Parameter	symbol	Test condition	Minimum	Typical case	Maximum	Unit
Input to output propag-ation delay (low to high)	tDPLH	RDIFF=54 Ω,CL_1 =CL_2=100pF(see Figure 3 and Figure 4)		12	35	ns
Input to output propag-ation delay (high to low)	tDPHL			12	35	ns
|tDPLH-tDPHL|	tsKEW1			6	10	ns
Rise time /fall time	tDR,tDF			9	25	ns
Enable to high output	tpZH	R=110Ω (see Figure 5 and 6)		20	90	ns
Enable to output low	tpZL			20	90	ns
Input low to disable	tpLZ	R=110Ω (see Figure 5 and 6)		20	80	ns
Enable high input	tpHZ			20	80	ns
Enable high outputunder off condition	tDSH	R=110Ω (see Figure 5 and 6)		500	900	ns
Enable low outputunder shutdown conditions	tDSL	RL=110Ω (see Figure 5 and 6)		500	900	ns

Supply Current						
Parameter	symbol	Test condition	Minimum	Typicel case	Maximum	Unit
Supply current	Iccl	/RE=0V,DE=0V		220	400	uA
	Icc2	/RE=VCC, DE=VCC		240	400	uA
Turn-off current	IsHDN	/RE=VCC,DE=0V		0.5	10	uA

DC Electrical Characteristics of the Receiver						
Parameter	symbol	Test condition	Minimum	Typical case	Maximum	Unit
Input current(A,B)	IN2	VCC=0 or 3.3V VIn=12V			125	uA
		VCC=0 or 3.3V VIn=-7V	-100			uA
Forward input threshold voltage	VIT+	-7V≤Vcm≤12V			-10/-50	mV
Reverse input threshold voltage	VIT-	-7V≤Vcm≤12V	-200			mV
Input hysteresis voltage	Vhys	-7V≤Vcm≤12V	10	30		mV
High level output voltage	VoH	IoUT=-4mA, VID=+200 mV	VCC-1.5			V
Low level output voltage	VoL	IoUT=+4mA, VID=-200 mV			0.4	V
Three state input leakage cur-rent	IozR	0.4V<Vo<2.4V			±1	uA
Input resistance of receiver	RIN	-7V≤VcM≤12V	96			kΩ
Receiver short circuit curr-ent	IosR	0V≤Vo≤VCC	±7		±95	mA

Drive switch characteristics						
Parameter	symbol	Test condition	Minimum	Typical case	Maximum	Unit
Input to output propag-ation delay (low to high)	tDPLH	RDIF=54 Q,CL1=CL2=100pF(see Fi-gure 10 and Figure 11)		12	35	ns
Input to output propag-ation delay(high to low)	tDPHL			12	35	ns
tDPLH-tDPHLI	tsKEW1			7	10	ns
Rise time/fall time	tDR,tDF			10	25	ns
Receiver switch characteristic						
Parameter	symbol	Test condition	Minimum	Typical case	Maximum	Unit
Propagationdelayfrom receiver input to	tRPLH	See Figure 12and Figure 13VD≥2.0V; rising and fal-ling edge timeVm≤15ns	20	60	90	ns
The propagation de-lay from receiver	tRPHL		20	60	90	ns
tRPLH-tRPHL	tsKEW2			7	10	ns

ADM489 Test circuit

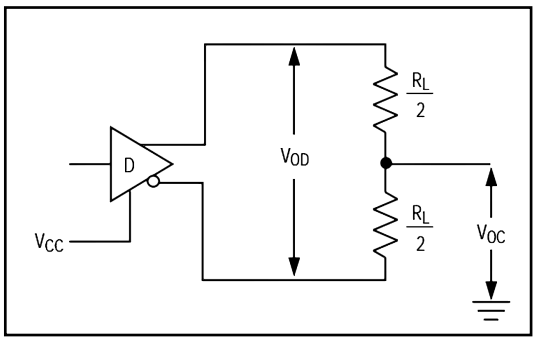


Figure 2: DC test load for the drive

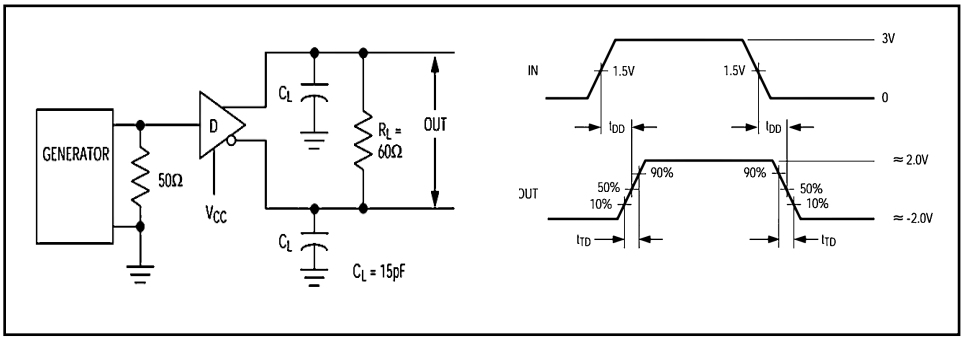


Figure 3 Drive-line Differential Delay and Transit Time

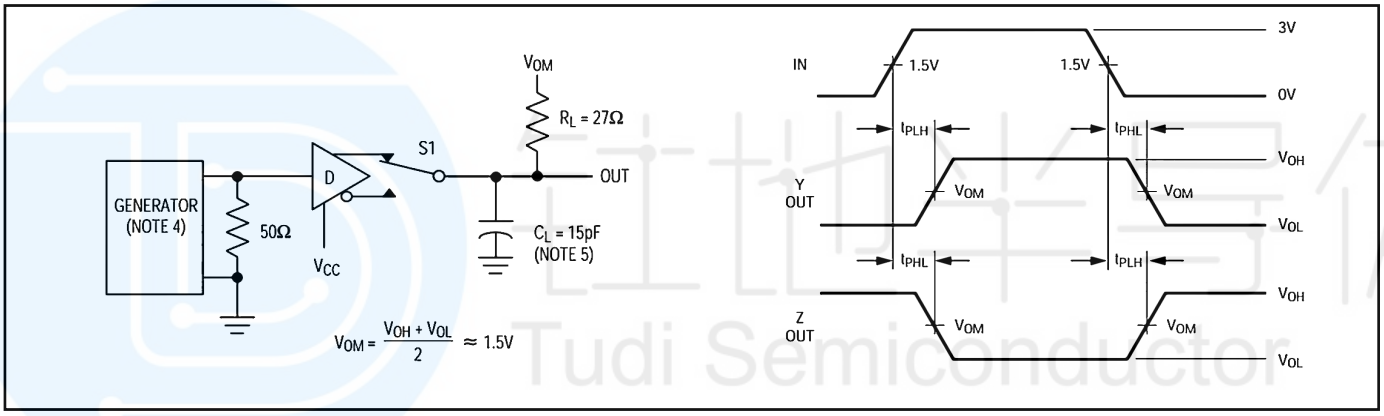


Figure 4 Drive propagation delay

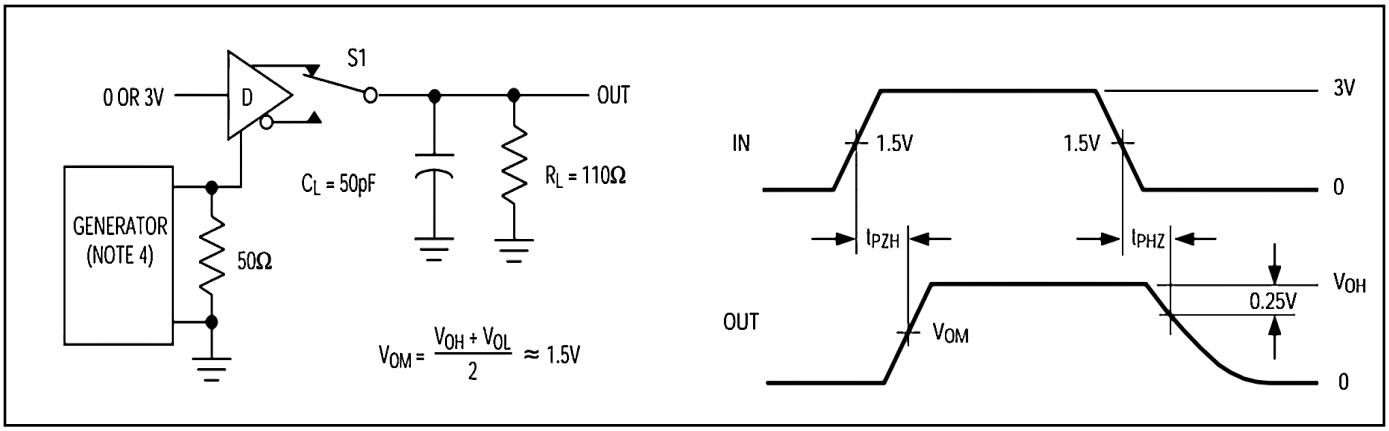


Figure 5 Drive enable and disable time

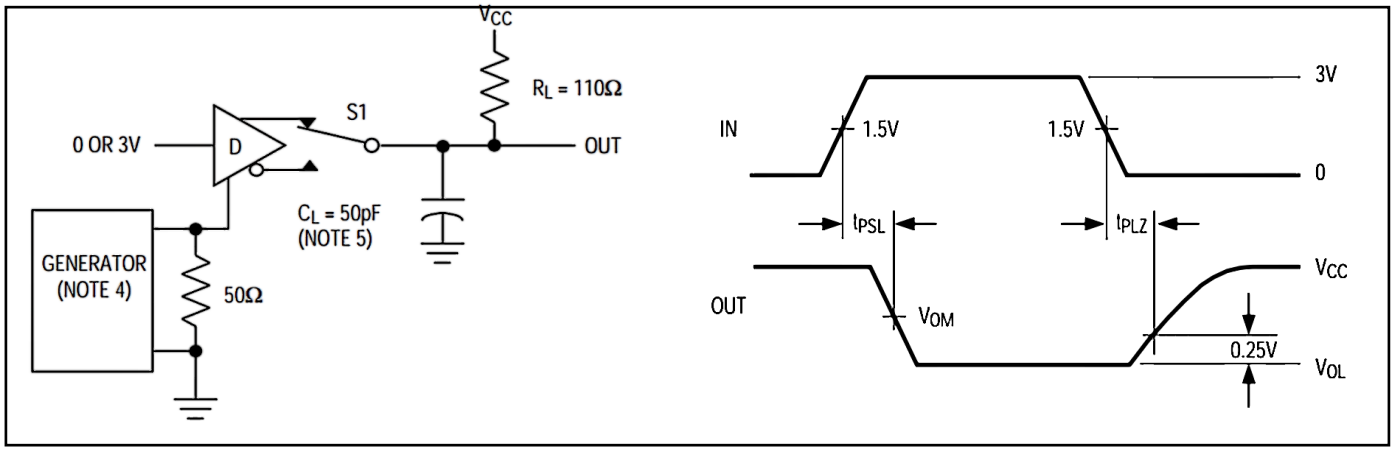


Figure 6 Drive enable and disable time

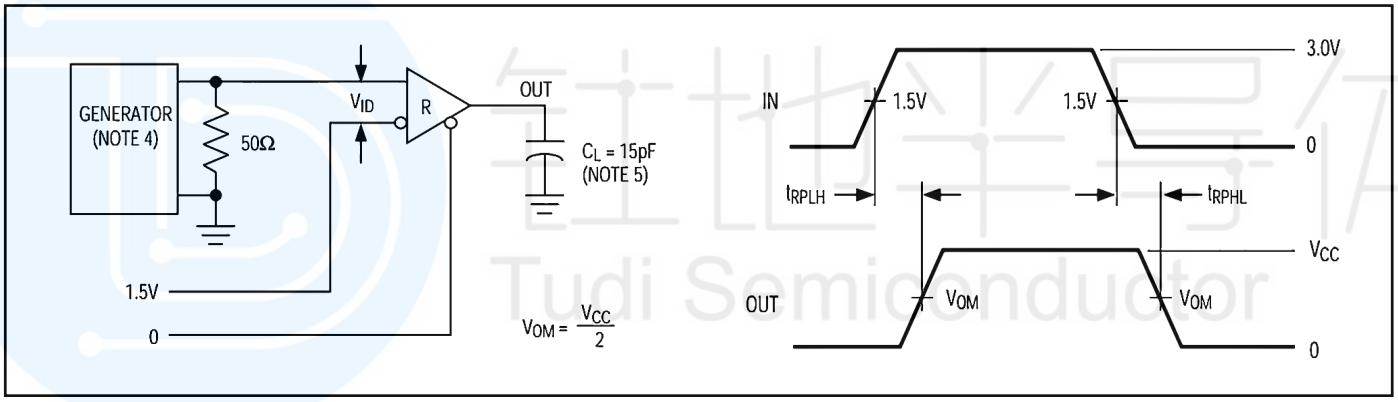
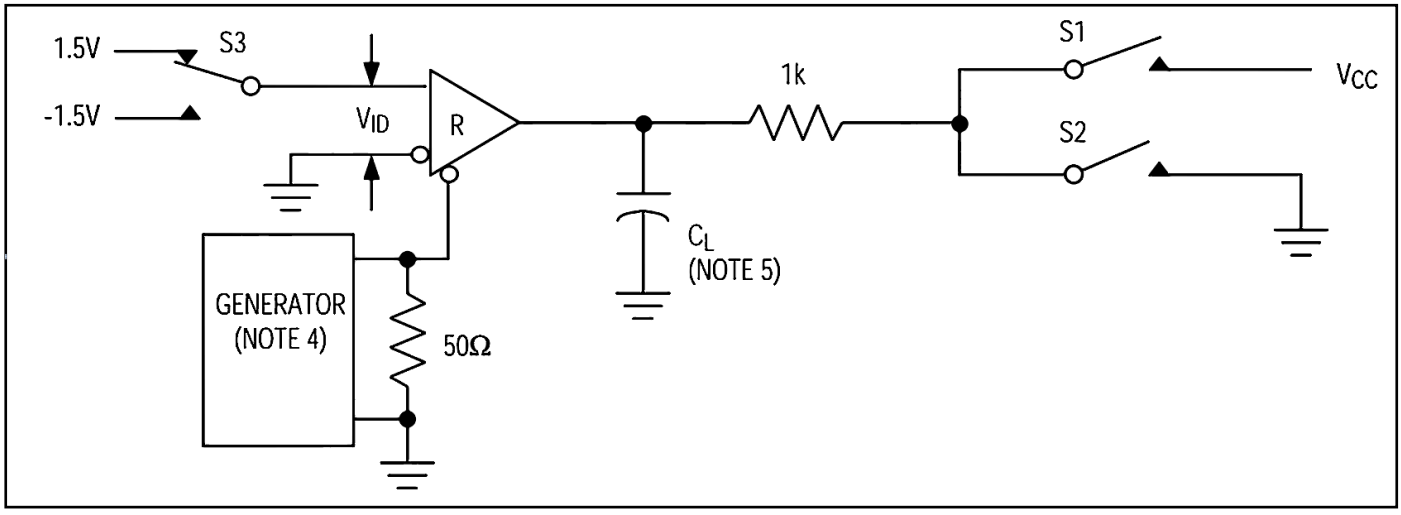


Figure 7: Receiver Propagation Delay Test Circuit



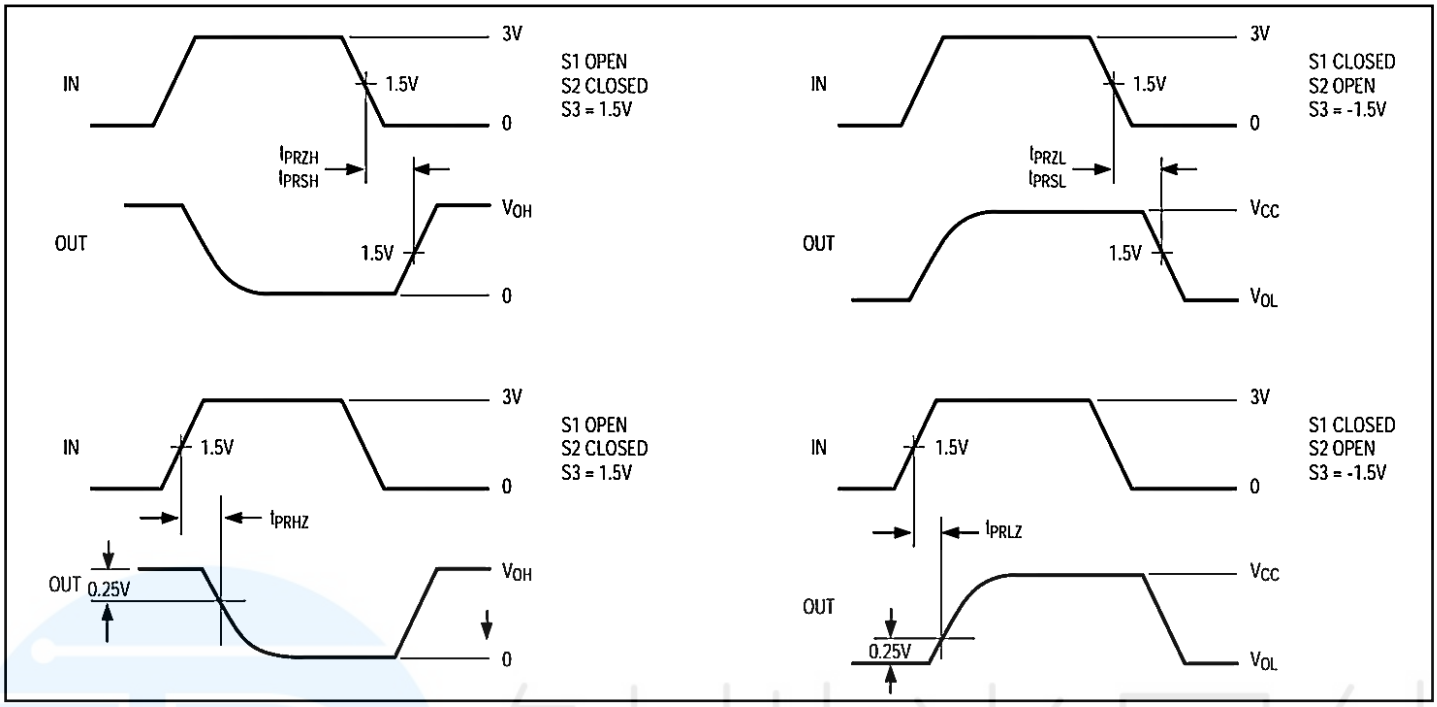


Figure 8 Receive enable and disable time

Order information

Order Number	Package	Package Quantity	Marking On The park	Temperature
ADM489ABRZ-REEL-TUDI	SOP14	Tape,Reel,2500	489ABRZ	- 40°C to 85°C
ADM489ABNZ-TUDI	DIP14	Tube,25,A box of 1000	489ABNZ	
ADM488ABRZ-REEL-TUDI	SOP8	Tape,Reel,2500	ADM488ABRZ	
ADM488ABRMZ-REEL-TUDI	MSOP8	Tape,Reel,2500	488ABRMZ	
ADM488ABNZ-TUDI	DIP8	Tube,50,A box of 2000	ADM488ABNZ	

SP490 Test circuit

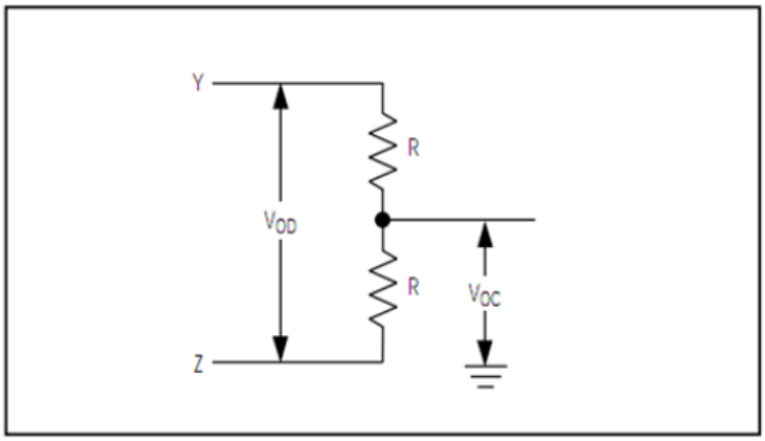


Figure9 DCTestLoadoftheDriver

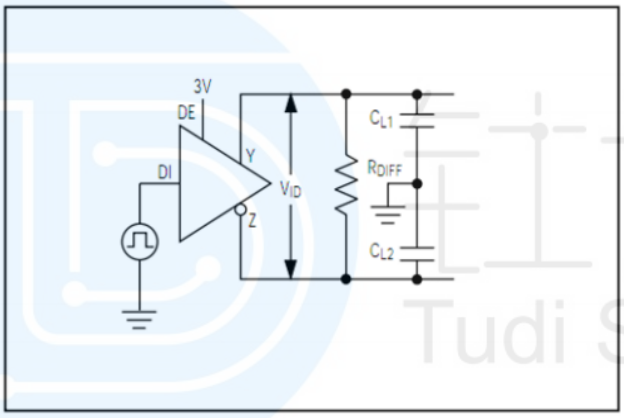


Figure10 DriverTimingTestCircuit

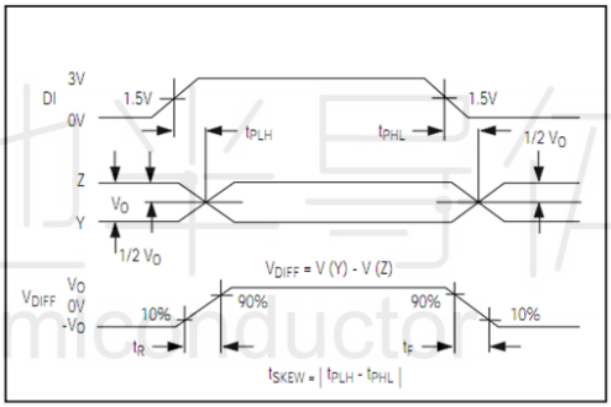


Figure11 PropagationDelayofDriver

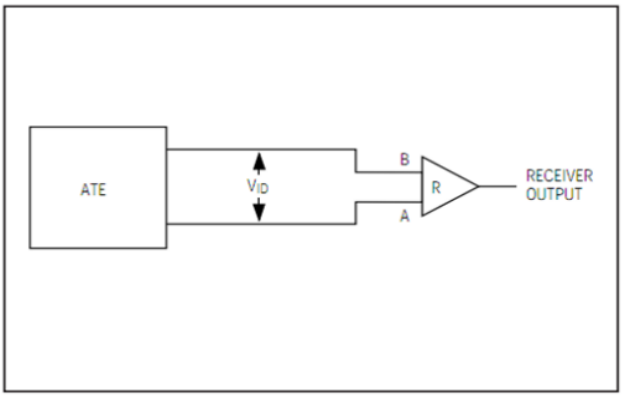


Figure12 ReceiverPropagationDelayTestCircuit

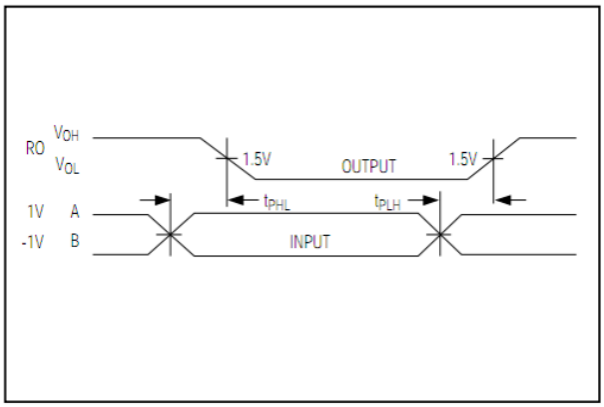
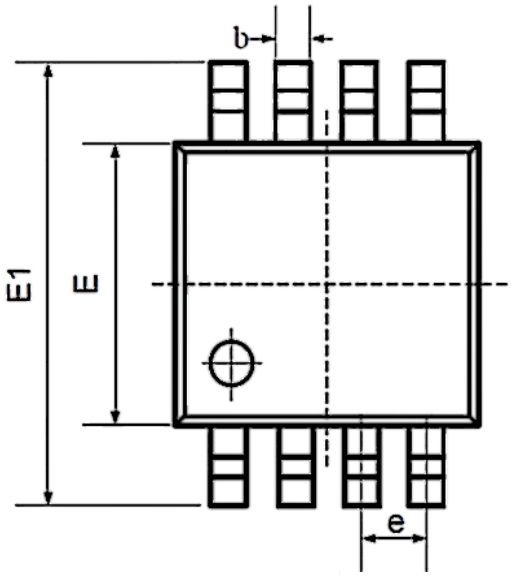
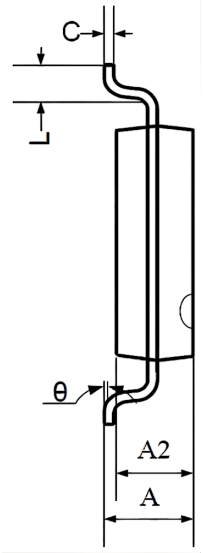
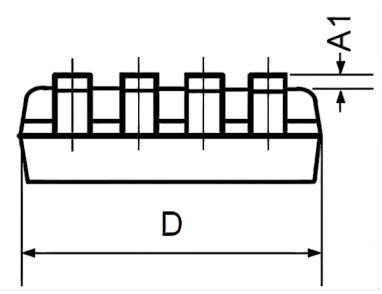


Figure13 ReceiverPropagationDelaySequence

Package MSOP8

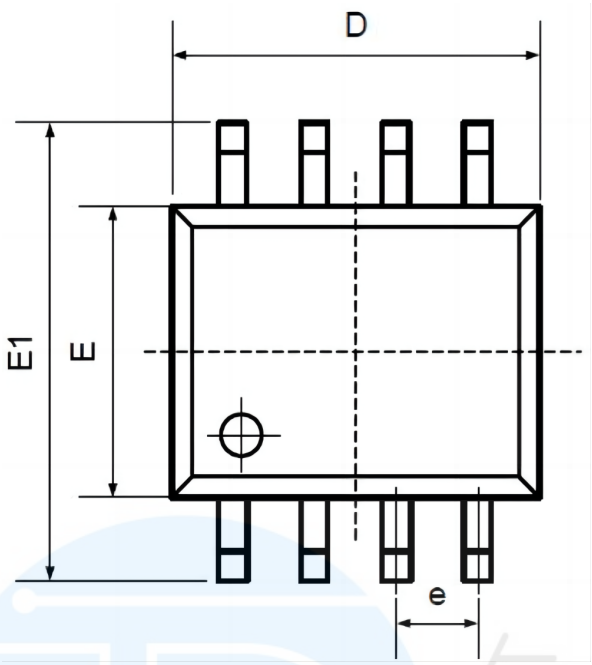


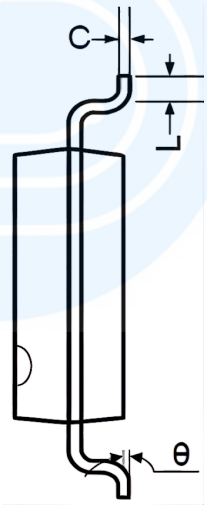


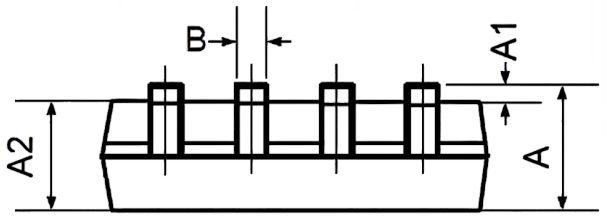


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.800	1.200	0.031	0.047
A1	0.000	0.200	0.000	0.008
A2	0.760	0.970	0.030	0.038
b	0.30 TYP		0.012 TYP	
C	0.15 TYP		0.006 TYP	
D	2.900	3.100	0.114	0.122
e	0.65 TYP		0.026 TYP	
E	2.900	3.100	0.114	0.122
E1	4.700	5.100	0.185	0.201
L	0.410	0.650	0.016	0.026
θ	0°	6°	0°	6°

Package SOP8

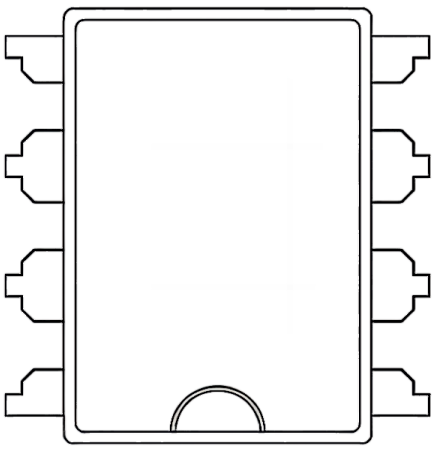


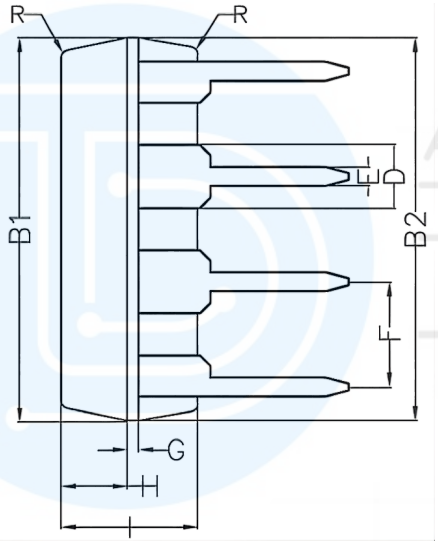


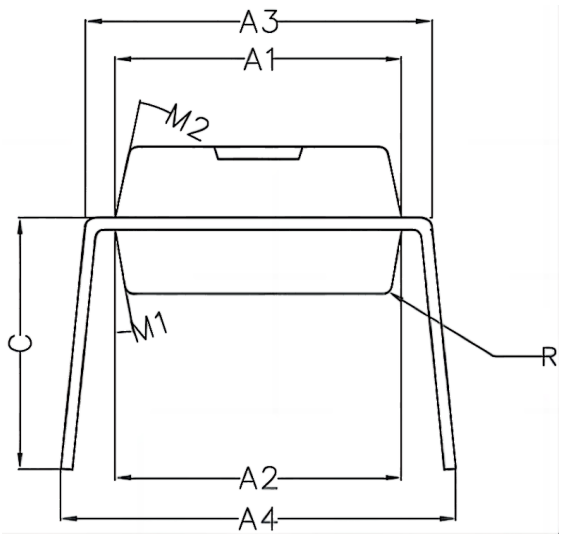


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
B	0.330	0.510	0.013	0.020
C	0.190	0.250	0.007	0.010
D	4.780	5.000	0.188	0.197
E	3.800	4.000	0.150	0.157
E1	5.800	6.300	0.228	0.248
e	1.270TYP		0.050TYP	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Package DIP8

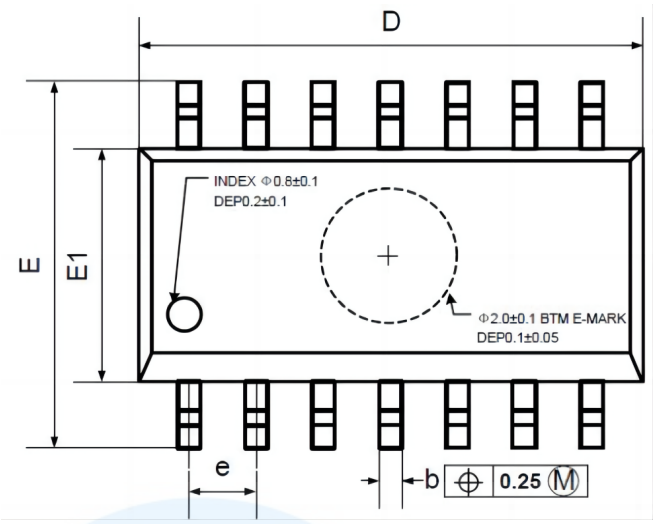


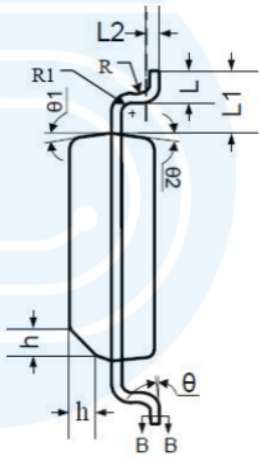


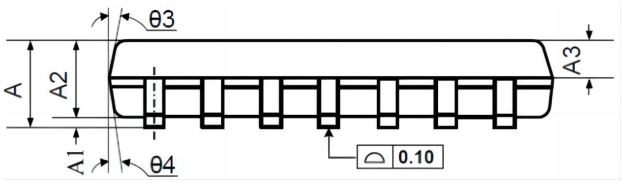


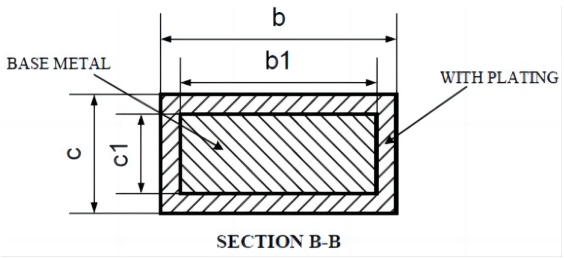
Symbol	Min	Non	Max
A1	6.28	6.33	6.38
A2	6.33	6.38	6.43
A3	7.52	7.62	7.72
A4	7.80	8.40	9.00
B1	9.15	9.20	9.25
B2	9.20	9.25	9.30
C		5.57	
D		1.52	
E	0.43	0.45	0.47
F		2.54	
G		0.25	
H	1.54	1.59	1.64
工	3.22	3.27	3.32
R		0.20	
M1	9°	10°	11°
M2	11°	12°	13°

Package SOP14



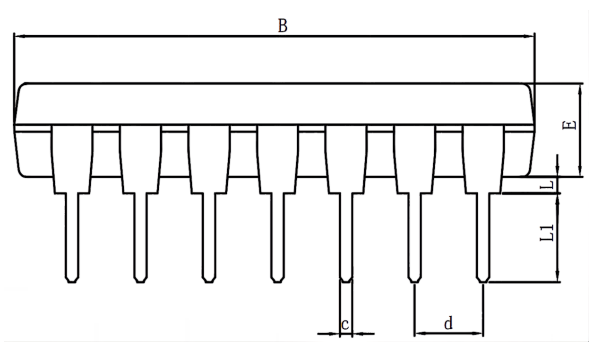


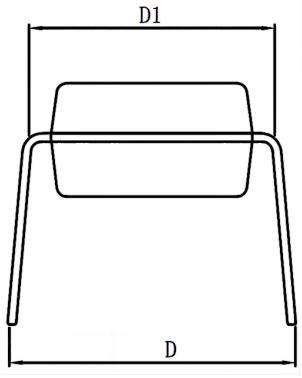


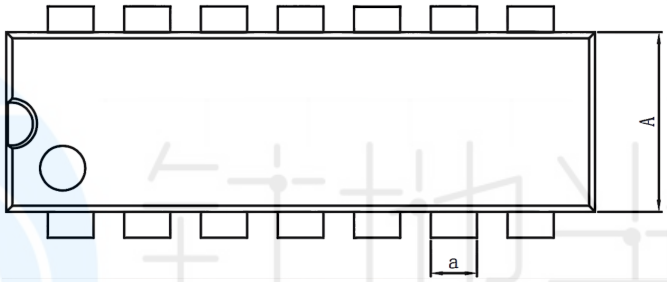


Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	1.35	1.60	1.75
A1	0.10	0.15	0.25
A2	1.25	1.45	1.65
A3	0.55	0.65	0.75
b	0.36		0.49
b1	0.35	0.40	0.45
C	0.16		0.25
c1	0.15	0.20	0.25
D	8.53	8.63	8.73
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27 BSC		
L	0.45	0.60	0.80
L1	1.04 REF		
L2	0.25 BSC		
R	0.07		
R1	0.07		
h	0.30	0.40	0.50
θ	0°		8°
θ1	6°	8°	10°
θ2	6°	8°	10°
θ3	5°	7°	9°
θ4	5°	7°	9°

Package DIP14







DIM.	MIN	TYP	MAX	DIM.	MIN	TYP	MAX
A	6.100	6.300	6.680	a	1.504	1.524	1.544
B	18.940	19.200	19.560	C	0.437	0.457	0.477
D	8.200	8.700	9.200	d	2.530	2.540	2.550
D1	7.42	7.62	7.82	L	0.500	—	0.800
E	3.100	3.300	3.550	L1	3.000	3.200	3.600

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