UMW TLP759

1.Description

TLP759 devices each consist of an infrared emitting diode, optically coupled to a high speed photo detector transistor. A separate connection for the photodiode bias and output-transistor collector increase the speed by several orders of magnitude over conventional phototransistor couplers by reducing the base-collector capacitance of the input transistor. The devices are packaged in an 8-pin DIP package and available in wide-lead spacing and SMD option.

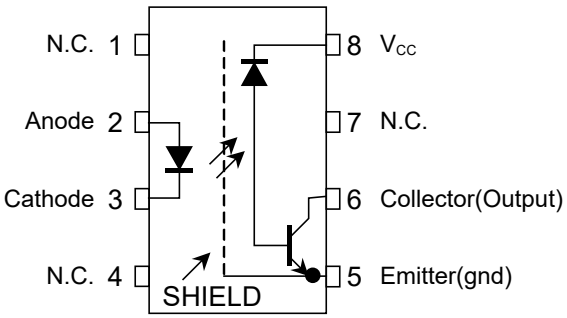
2.Features

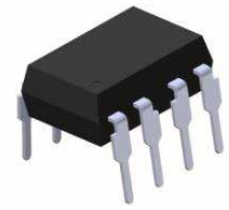
- High speed 1Mbit/s
- High isolation voltage between input and output (Viso=5000 Vrms)
- Guaranteed performance from 0°C to 70°C
- Wide operating temperature range of -55°C to 100°C
- Pb free and RoHS compliant

3.Applications

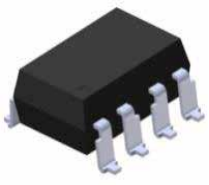
- Line receivers
- Telecommunication equipments
- Power transistor isolation in motor drives
- Replacement for low speed phototransistor photo couplers
- Feedback loop in switch-mode power supplies
- Home appliances
- High speed logic ground isolation

4.Pinning Information





DIP-8



SOP- 8

5.Absolute Maximum Ratings T_A= 25°C

Parameter		Symbol	Value	Units
Input	Forward current	I_F	25	mA
	Peak forward current (50% duty, 1ms P.W) (1)	I_{FP}	50	mA
	Peak transient current (≤1μs P.W,300pps)	I_{Ftrans}	1	A
	Reverse voltage	V_R	5	V
	Power dissipation	P_{IN}	45	mW
Output	Power dissipation	P_O	100	mW
	Average Output current	$I_{O(AVG)}$	8	mA
	Peak Output current	$I_{IO(PK)}$	16	mA
	Output voltage	V_O	-0.5 to 20	V
	Supply voltage	V_{CC}	-0.5 to 30	V
Total Power Dissipation		P_{TOT}	145	mW
Isolation Voltage (2)		V_{ISO}	5000	V_{rms}
Operating Temperature		T_{OPR}	-55 to 100	°C
Storage Temperature		T_{STG}	-55 to 125	°C
Soldering Temperature (3)		T_{SOL}	260	°C

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings. Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/Derating Concept and Methods) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

(Note 1) 50 % duty cycle, 1 ms pulse width. Derate 1.6 mA / °C above 70 °C.

(Note 2) AC for 1 minute, R.H.=40 ~ 60% R.H. In this test, pins 1,2,3 & 4 are shorted together,and pins 5,6,7 & 8 are shorted together.

(Note 3) For 10 seconds.

6.Electrical Characteristics (T_A=0 to 70°C unless specified otherwise)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input						
Forward Voltage	V_F	I_F=16mA		1.45	1.7	V
Reverse Voltage	B_{VR}	I_R=10μA	5	20		V
Temperature coefficient of forward voltage	$\Delta V_F/\Delta T_A$	I_F=16mA		-1.6		mV/°C
Output						
Logic High Supply Current	I_{CCH}	V_{CC}=15V, I_F=0mA, V_O=Open			1	μA
		T_A=0~70°C			2	μA
Transfer						
Logic High Output Current	I_{OH}	I_F=0mA, V_O=V_{CC}=15V		0.005	1	μA
		T_A=0~70°C, V_O=V_{CC}=15V			50	μA
Logic Low Output Voltage	VOL	I_F=16mA, V_{CC}=4.5V,I_O=2.4mA		0.1	0.4	V
Current Transfer Ratio	CTR	I_F=16mA, V_{CC}=4.5V, I_O=0.4V	26	40	60	%
Isolation Voltage	V_{ISO}	RH<50%, T_A=25°C, I_{I-O}≤50μA	5000			V_{RMS}

7.Switching Characteristics

(T_A=0 to 70°C unless specified otherwise, I_F=16mA, V_{CC}=5V)

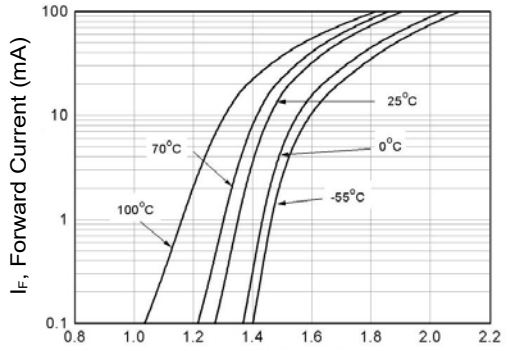
Parameter	Symbol	Conditions		Typ	Max	Units
Propagation Delay Time to Logic Low	T_{PLH}	I_F=16mA, R_L=4.1kΩ		1300	1500	ns
		I_F=16mA, R_L=1.9kΩ		600	800	ns
Propagation Delay Time to Logic	T_{PHL}	I_F=16mA, R_L=4.1kΩ		200	1500	ns
		I_F=16mA, R_L=1.9kΩ		200	800	ns
Common Mode Transient Immunity at Logic High (1)	$\|CM_H\|$	R_L=4.1KΩ	T_A=25°C, I_F=0mA, C_L=15pF	10000		V/μs
		R_L=1.9KΩ	|VCM|=10V(Peak)			
Common Mode Transient Immunity at Logic Low (1)	$\|CM_L\|$	R_L=4.1KΩ	T_A=25°C, I_F=16mA	10000		V/μs
		R_L=1.9KΩ	C_L=15pF			

(Note 1)

CM_L is the maximum rate of fall of the common mode voltage that can be sustained with the output voltage in the logic low state (V_O < 0.8 V).

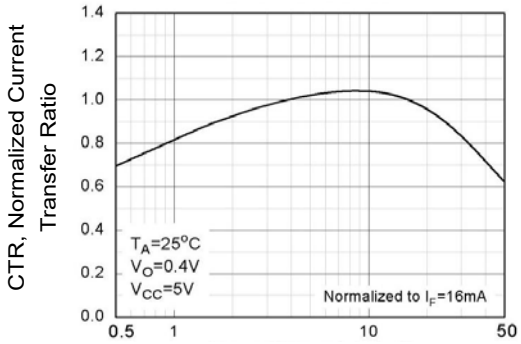
CM_H is the maximum rate of rise of the common mode voltage that can be sustained with the output voltage in the logic high state (V_O > 2.0 V).

8.Typical Characteristic



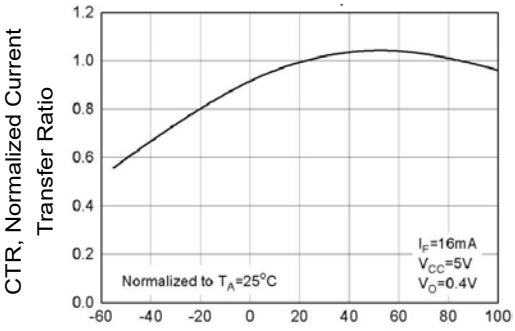
V_F, Forward Voltage (V)

Figure 1: Forward Current vs. Forward Voltage



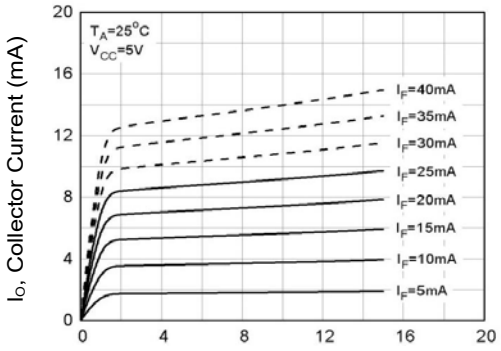
I_F, Forward Current (mA)

Figure 2: Normalized Current Transfer Ratio vs. Forward Current



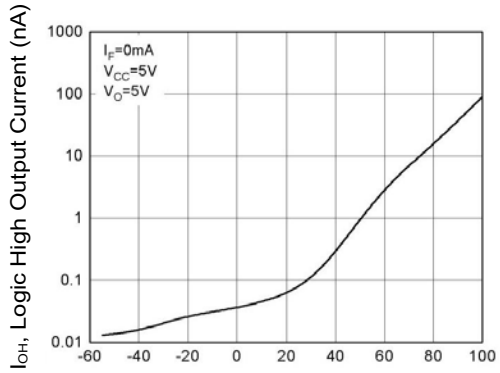
T_A, Ambient Temperature (°C)

Figure 3: Normalized Current Transfer Ratio vs. Ambient Temperature



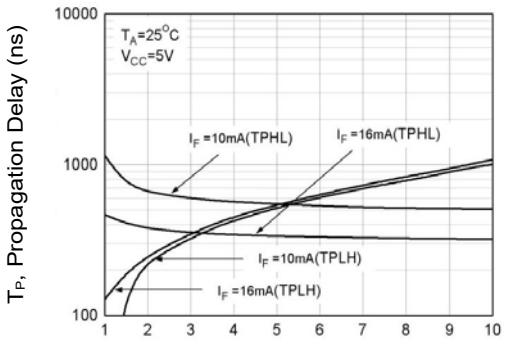
V_O, Collector-Emitter Voltage (V)

Figure 4: Output Current vs Output Voltage



T_A, Temperature (°C)

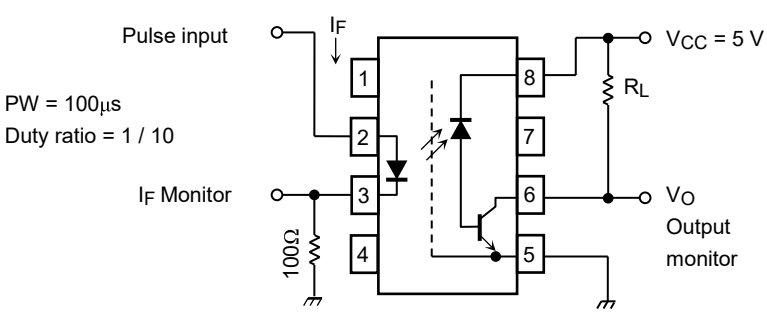
Figure 5: Logic High Output Current vs. Temperature

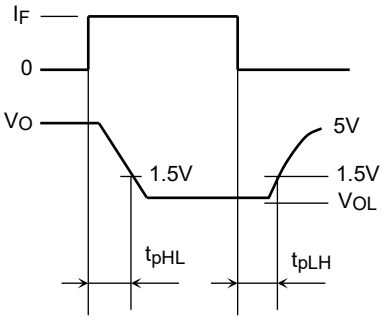


R_L, Load Resistance (kΩ)

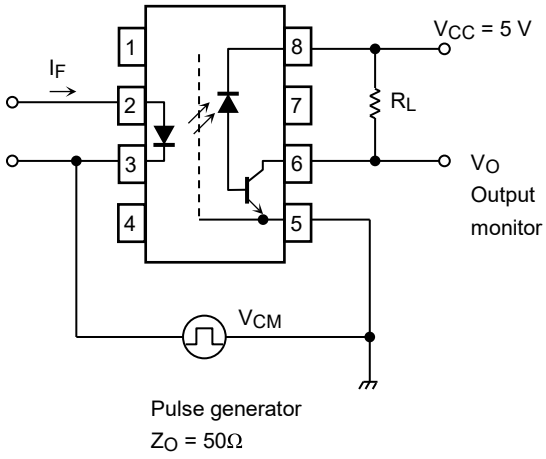
Figure 6: Propagation Delay vs. Load Resistance

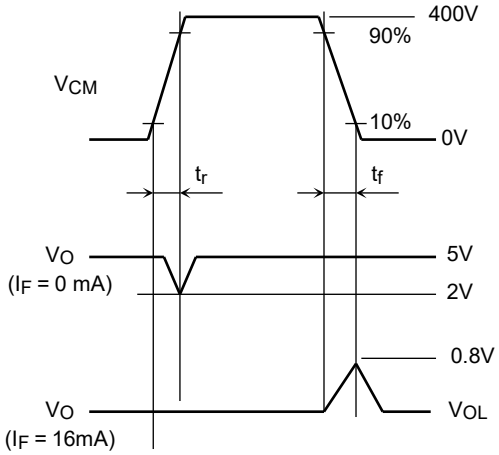
9.Switching Time Test Circuit





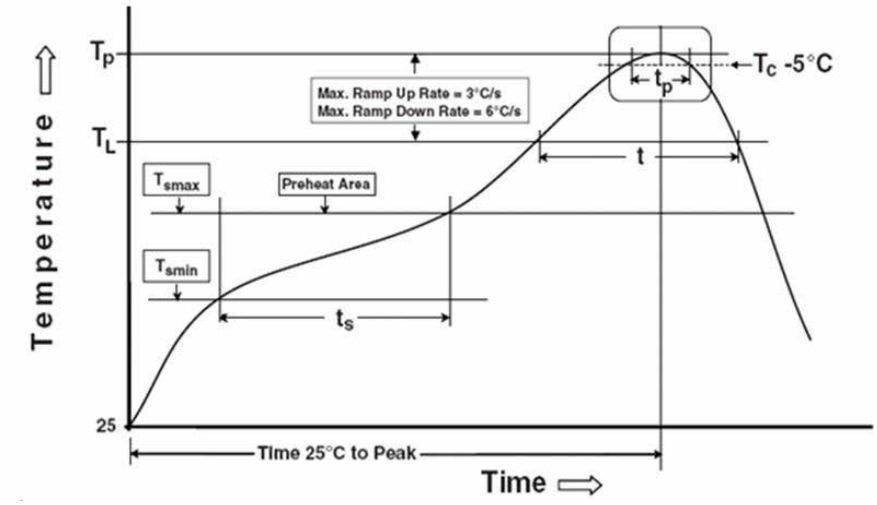
10.Common Mode Noise Immunity Test Circuit





$$CM_H = \frac{320\,(V)}{t_r\,(\mu s)} \quad CM_L = \frac{320\,(V)}{t_f\,(\mu s)}$$

11.Precautions for Use

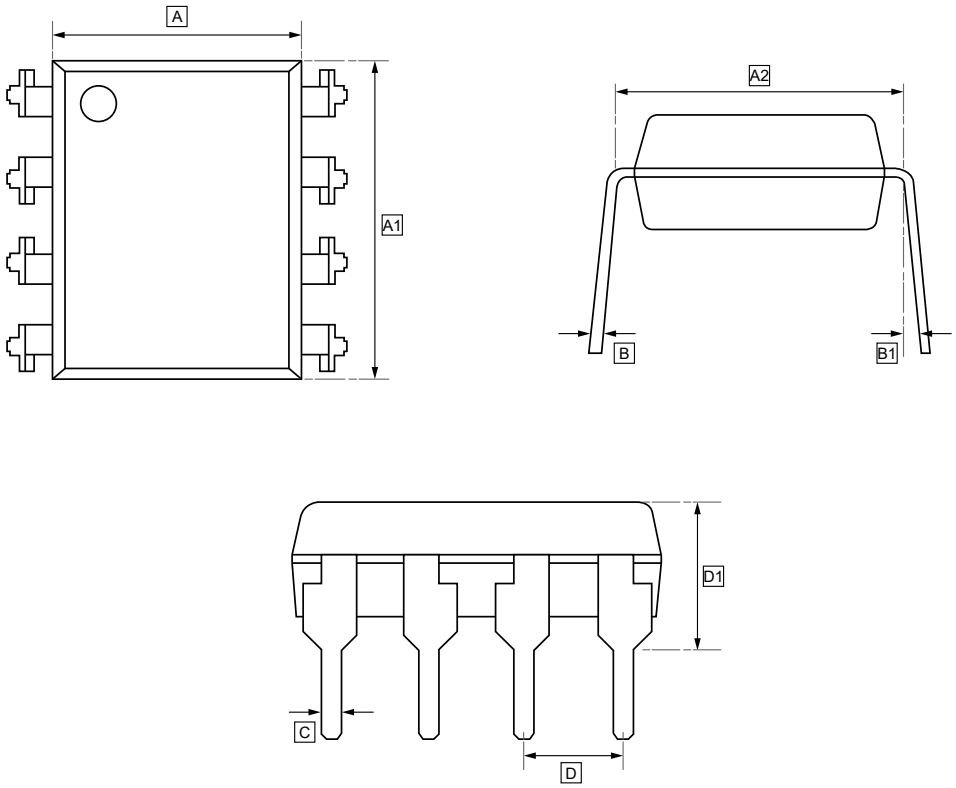


1. Soldering Condition

1.1 (A) Maximum Body Case Temperature Profile for evaluation of Reflow Profile

Preheat	
Temperature min (T_{smin})	150°C
Temperature max (T_{smax})	200°C
Time (T_{smin} to T_{smax}) (t_s)	60-120 seconds
Average ramp-up rate (T_{smax} to T_p)	3°C/second max
Other	
Liquidus Temperature (T_L)	216°C
Time above Liquidus Temperature (t_L)	60-100 sec
Peak Temperature (T_p)	260°C
Time within 5°C of Actual Peak Temperature: T_p - 5°C	30s
Ramp- Down Rate from Peak Temperature	6°C /second max
Time 25°C to peak temperature	8 minutes max
Reflow times	3 times

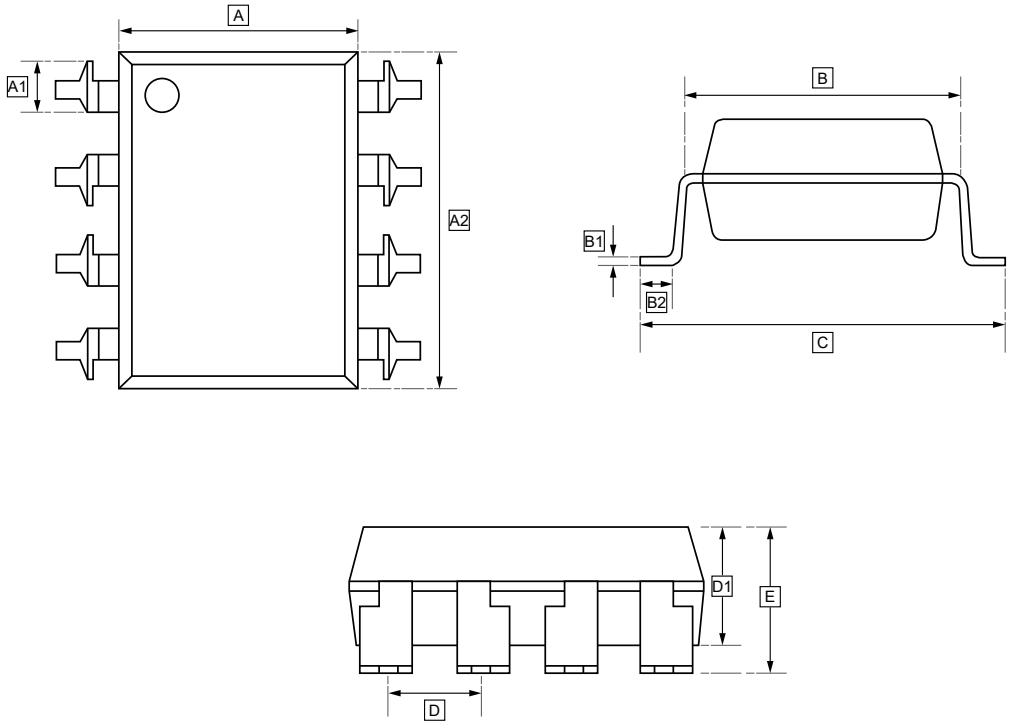
12.1 DIP-8 Package Outline Dimensions



DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A2	B	B1	C	D	D1
Min	6.30	9.46	7.62	0.25	5°	0.40	2.54	4.20
Max	6.90	10.06	TYP.		15°	0.60	TYP.	4.80

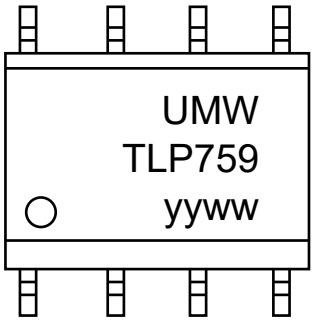
12.2 SOP-8 Package Outline Dimensions



DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A2	B	B1	B2	C	D	D1	E
Min	6.30	1.45	9.46	7.62	0.25	0.6	-	2.54	3.20	4.00
Max	6.90		10.06	TYP		-	10.3	TYP	3.80	4.60

13.Ordering Information



yy: Year Code
ww: Week Code

Order Code	Package	Base QTY	Delivery Mode
UMW TLP759	SOP-8	1000	Tape and reel

14.Disclaimer

UMW reserves the right to make changes to all products, specifications. Customers should obtain the latest version of product documentation and verify the completeness and currency of the information before placing an order.

When applying our products, please do not exceed the maximum rated values, as this may affect the reliability of the entire system. Under certain conditions, any semiconductor product may experience faults or failures. Buyers are responsible for adhering to safety standards and implementing safety measures during system design, prototyping, and manufacturing when using our products to prevent potential failure risks that could lead to personal injury or property damage.

Unless explicitly stated in writing, UMW products are not intended for use in medical, life-saving, or life-sustaining applications, nor for any other applications where product failure could result in personal injury or death. If customers use or sell the product for such applications without explicit authorization, they assume all associated risks.

When reselling, applying, or exporting, please comply with export control laws and regulations of China, the United States, the United Kingdom, the European Union, and other relevant countries, regions, and international organizations.

This document and any actions by UMW do not grant any intellectual property rights, whether express or implied, by estoppel or otherwise. The product names and marks mentioned herein may be trademarks of their respective owners.