

CSNP64GCR01-BOW

Version: V1.1

July 10, 2026



Revision History

Version	Date	Description
V1.0	07/06/2024	Origin Draft
V1.1	10/07/2026	Expanded the temperature range



Contents

REVISION HISTORY	I
1. INTRODUCTION	1
1.1 OVERVIEW	1
1.2 FEATURES	1
1.3 BLOCK DIAGRAM	1
2. PRODUCT SPECIFICATIONS	2
2.1 PIN ASSIGNMENTS (TOP VIEW)	2
2.2 PACKAGE DIMENSIONS	2
3. PERFORMANCE	4
4. DC CHARACTERISTICS	5
5. AC CHARACTERISTICS	6
5.1 BUS TIMING (DEFAULT MODE)	6
5.2 BUS TIMING (HIGH-SPEED MODE)	6
6. REFERENCE DESIGN	8



1.1 Overview

CSNP64GCR01-BOW is LGA-8 package. The size is 8.5mm x 7mm x0.9mm.

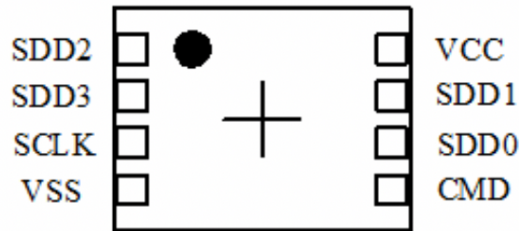
- Interface: Standard SD Specification Version 2.0 with 1-I/O and 4-I/O.
- Power supply: Vcc = 2.7V - 3.6V
- Default mode: Variable clock rate 0 - 25 MHz, up to 12.5 MB/sec interface speed (using 4 parallel data lines)
- High-Speed mode: Variable clock rate 0 - 50 MHz, up to 25 MB/sec interface speed (using 4 parallel data lines)
- Operating Temperature: -25°C to +85°C
- Storage Temperature: -40°C to +125°C
- Standby Current: < 100uA

[illegible]



2. Product Specifications

2.1 Pin Assignments (Top View)

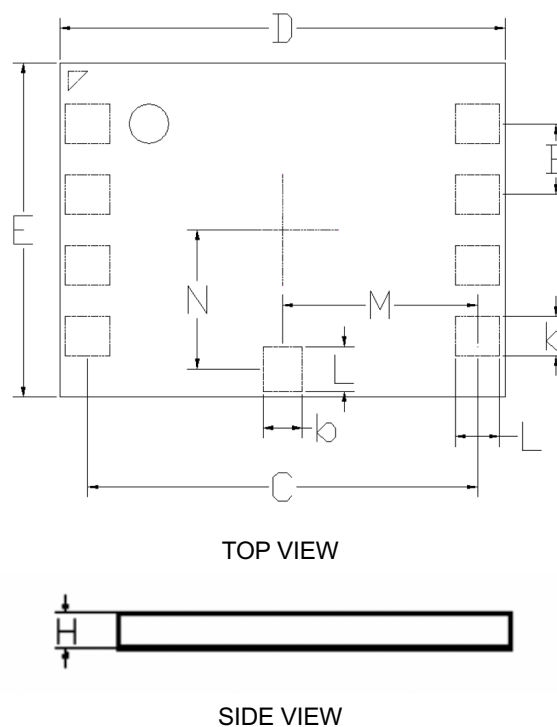


PIN#	SD MODE			SPI MODE		
	NAME	TYPE ¹	DESCRIPTION	NAME	TYPE	DESCRIPTION
1	SDD2	I/O/PP	Data Line [Bit2]	RSV		Reserved
2	CD/SDD3 ²	I/O/PP ³	SDNAND Detect/ Data Line [Bit3]	CS	I ³	Chip Select (Neg True)
3	SCLK	I	Clock	SCLK	I	Clock
4	VSS	S	Supply Voltage Ground	VSS	S	Supply Voltage Ground
5	CMD	PP	Command/Response	DI	I	Data In
6	SDD0	I/O/PP	Data Line [Bit0]	DO	O/PP	Data Out
7	SDD1	I/O/PP	Data Line [Bit1]	RSV		Reserved
8	VCC	S	Supply Voltage	VCC	S	Supply Voltage

1) S: power supply; I: input; O: output using push-pull drivers; PP: I/O using push-pull drivers;

2) The extended SDD lines (SDD1-SDD3) are input on power up. They start to operate as SDD lines after SET_BUS_WIDTH command. The Host shall keep its own SDD1-SDD3 lines in input mode, as well, while they are not used. It is defined so, in order to keep compatibility to SDNAND.

2.2 Package Dimensions





	Common Dimensions			
Symbol	Min	Nom	Max	Note
b	0.7	0.75	0.8	
L	0.78	0.83	0.88	
B	-	1.27(Typ)	-	
C	7.44	7.49	7.54	
D	8.40	8.50	8.60	
E	6.90	7.00	7.10	
H	0.87	0.90	0.93	
M	-	3.75(Typ)	-	
N	-	2.96(Typ)	-	

SDNAND Package Dimensions (unit: mm)

**3. Performance**

Parameter	Range	
Temperature	Work Model	-25° ~ 85°C
	Storage Model	- 40° ~ 125°C
Humidity	Work Model	8% to 95%, Non-condensing
	Storage Model	8% to 95%, Non-condensing



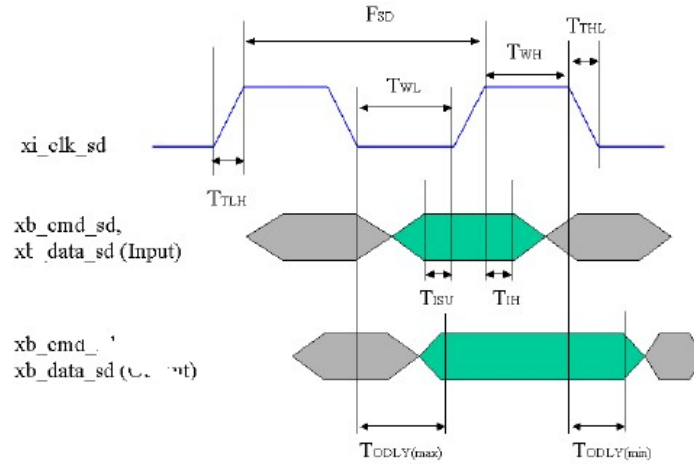
4. DC Characteristics

Symbol	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V _{IL}	Input low voltage		V _{SS} -0.3		0.25V _{CC}	V
V _{IH}	Input high voltage		0.625V _{CC}		V _{CC} +0.3	V
V _{OL}	Output low voltage	I _{OL} =100μA @V _{CC_min}			0.125V _{CC}	V
V _{OH}	Output high voltage	I _{OH} =100μA @V _{CC_min}	0.75V _{CC}			V
I _{IN}	Input leakage current	V _{IN} =V _{CC} or 0	-10	+/-1	10	μA
I _{OUT}	Tri-state output leakage current		-10	+/-1	10	μA
I _{STBY}	Standby current	3.3V@clock stop		80	100	μA
I _{OP}	Operation current	3.3v@50MHz (Write)		15		mA
		3.3v@50MHz (Read)		15		mA



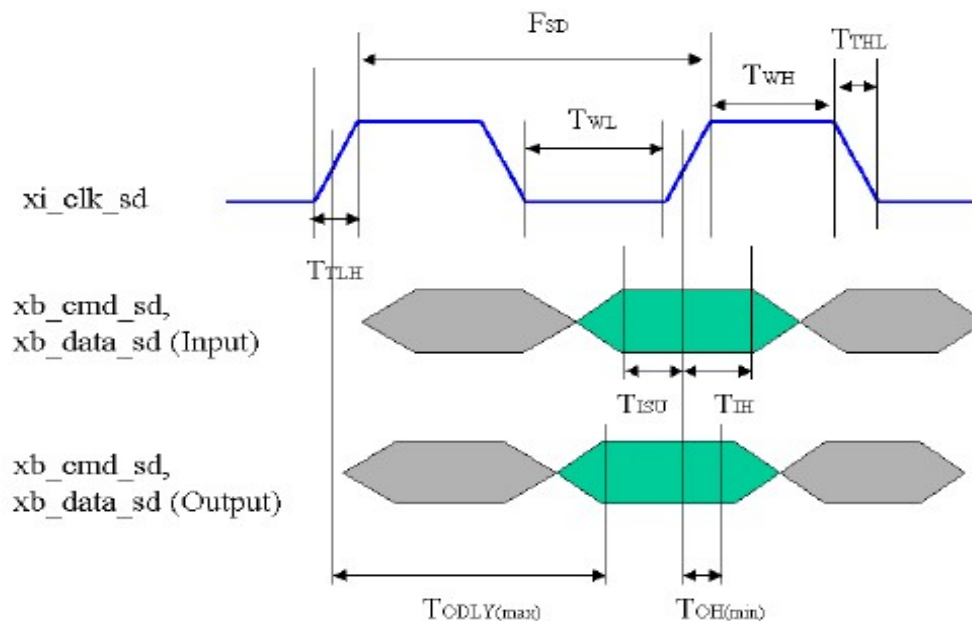
5. AC Characteristics

5.1 Bus Timing (Default Mode)



SYMBOL	PARAMETER	MIN	MAX	UNIT	NOTE
F_{SD}	SD clock frequency	0	25	MHz	
T_{WL}	Clock low time	10		ns	
T_{WH}	Clock high time	10		ns	
T_{TLH}	Clock rise time		10	ns	
T_{THL}	Clock fall time		10	ns	
T_{ISU}	Input setup time	5		ns	
T_{IH}	Input hold time	5		ns	
T_{ODLY}	Output delay time	0	14	ns	

5.2 Bus Timing (High-speed Mode)

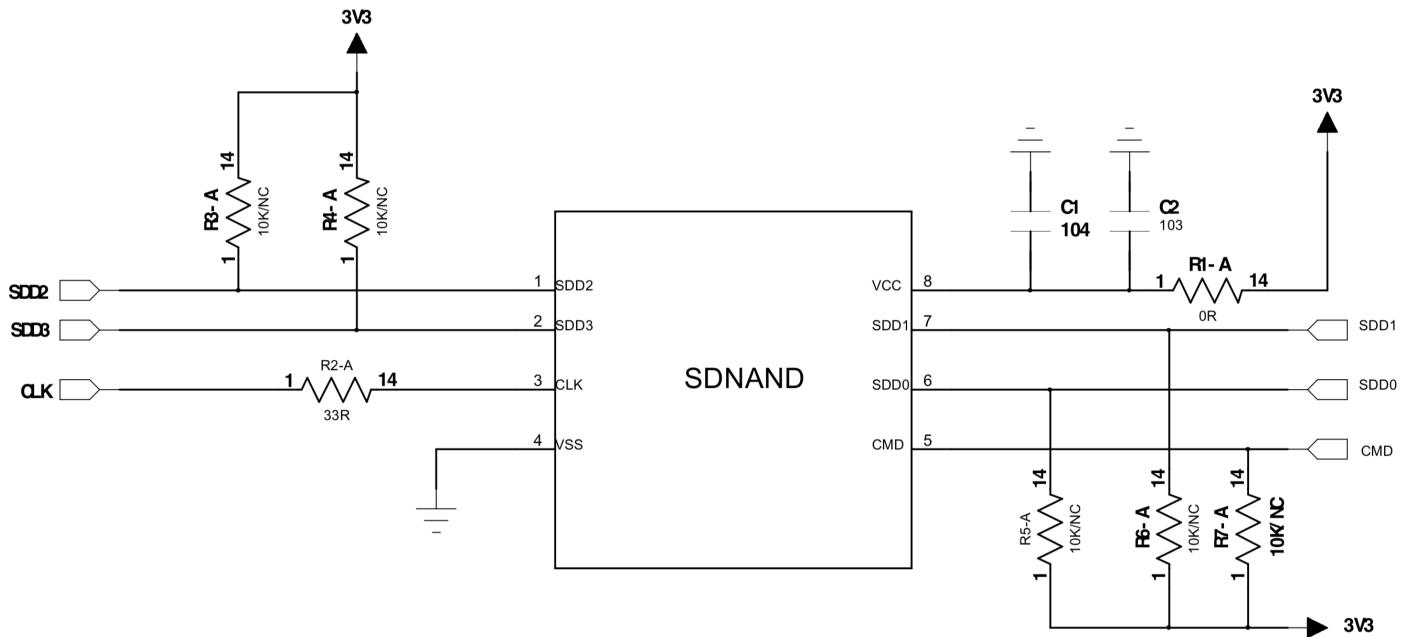




SYMBOL	PARAMETER	MIN	MAX	UNIT	NOTE
F _{SD}	SD clock frequency	0	50	MHz	
T _{WL}	Clock low time	10		ns	
T _{WH}	Clock high time	10		ns	
T _{TLH}	Clock rise time		10	ns	
T _{THL}	Clock fall time		10	ns	
T _{ISU}	Input setup time	5		ns	
T _{IH}	Input hold time	5		ns	
T _{ODLY}	Output delay time	0	14	ns	
T _{OH}	Output hold time	2.5		ns	



6. Reference Design



Note:

R_{DAT} and R_{CMD} (10K~100 k Ω) are pull-up resistors protecting the CMD and the DAT lines against bus floating when SDNAND is in a high-impedance mode.

The host shall pull-up all DAT0-3 lines by R_{DAT} , even if the host uses the SDNAND as 1-bit mode only in SD mode. It is recommended to have 2.2uF capacitance on VCC.

R_{CLK} reference 0~120 Ω .