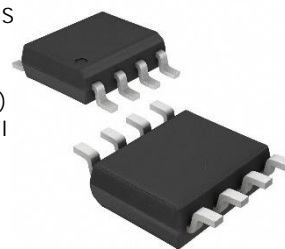


## HX37324-S/HX27324-S Dual channel 2A ultra high speed power switch drive

HX37324-S/HX27324-S is a power switch driver. It has matching rise and fall times for charging and discharging the gate of the power switch. HX37324-S/HX27324-S has high latch resistance under any conditions within the rated power and voltage range. Even if there is a noise spike of up to 5V (of any polarity) on the ground pin, HX37324-S/HX27324-S will not be damaged. It can accept a reverse current of up to 500mA to force its output back without causing damage or logical confusion. In addition, all terminals of HX37324-S/HX27324-S are fully protected by electrostatic discharge (ESD) up to 2.0kV. HX37324-S/HX27324-S is a power switch driver with matching rise and fall times and high latch resistance. It will not be damaged by noise spikes up to 5V and can accept reverse currents up to 500mA. In addition, all terminals of HX37324-S/HX27324-S are protected against electrostatic discharge up to 2.0kV.



SOP-8

Device Information		
Part Number	Encapsulation	Classification
HX37324-S	SOIC8	Consumer category
HX27324-S	SOIC8	Industry

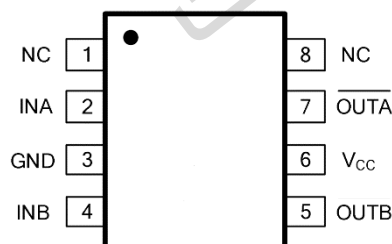
### Pecularity

- Latch protection: can withstand reverse current of 0.5A
- Input logic protection: capable of protecting input signals as low as -10V
- Low output impedance
- Single chip integrated dual driver
- Peak output current: 2A
- Scope of work: 4.5V~25V
- The maximum input voltage is 5V
- High capacitance load driving capability: Under a 1nF load, the switching time is less than 25ns, and the rise/fall time is matched
- Propagation delay: 40ns
- Wide temperature range: -40 °C~125 °C
- Chip on/off delay characteristics: Ton/Off=70ns/70ns
- Compliant with RoSH standards
- Package type: SOIC8/DFN8

### Apply

- Switching power supply, switching converter
- line driver
- Pulse Transformer Drive
- Drive MOSFETs and IGBTs
- motor control
- pulse generator
- power switch
- DC-DC converter
- Class D switching amplifier

Chip Pin Description		
NUMBER	NAME	FUNCTION
1	NC	Empty pin
2	INA	Channel A Input terminal
3	GND	Pin ground
4	INB	Channel B Input terminal
5	OUTB	Channel B output
6	V <sub>CC</sub>	power supply
7	OUTA	Channel A output
8	NC	Empty pin

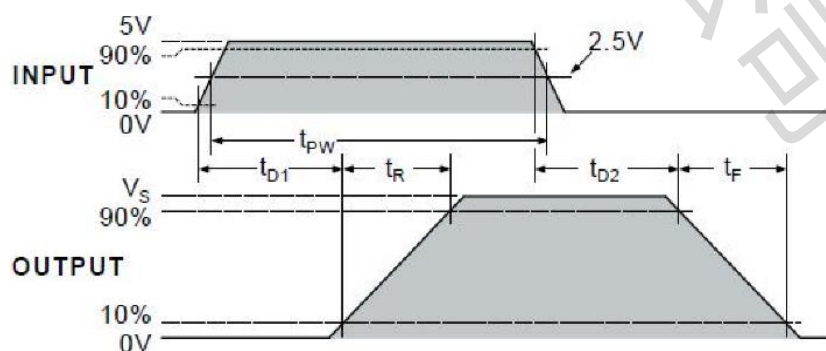


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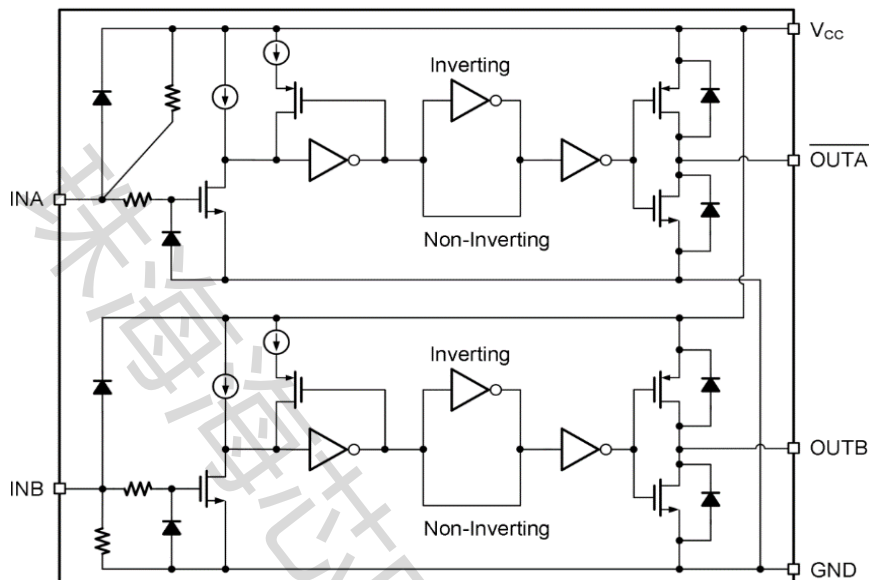
Product Specification				
SYMBOL	DEFINITION	MIN	MAX	UNIT
Limit operating range				
V <sub>CC</sub>	Supply voltage		25	V
V <sub>IN</sub>	Logic input voltage(INA/INB)	-10	V <sub>CC</sub> +0.3	
ESD Rating				
ESD	Human body discharge mode		2000	V
	Machine discharge mode		500	
Rated Power				
P <sub>D</sub>	SOIC Package power (TA ≤ 70°C)		470	mW
Caloric Information				
T <sub>J</sub>	Junction temperature		+150	°C
T <sub>S</sub>	Storage temperature	-45	+150	
Recommended Scope of Work				
V <sub>CC</sub>	Supply voltage	4.5	18.5	°C

Electrical characteristics without special instructions TA= 25°C, 4.5V ≤ V <sub>CC</sub> ≤ 18V					
SYMBOL	DEFINITION	MIN	TYP	MAX	UNIT
V <sub>IH</sub>	Logic High level "1" input voltage	2.4			V
V <sub>IL</sub>	Logic Low "0" input voltage			0.8	V
I <sub>IN</sub>	Input current(0V ≤ V <sub>IN</sub> ≤ V <sub>CC</sub> )			200	μA
V <sub>OH</sub>	High level output voltage drop	V <sub>CC</sub> -0.025			V
V <sub>OL</sub>	Low output voltage drop			0.025	V
R <sub>OH</sub>	High level state, output resistance(V <sub>CC</sub> =18V, I <sub>O</sub> =100mA)		4	8	Ω
R <sub>OL</sub>	Low level state, output resistance(V <sub>CC</sub> =18V, I <sub>O</sub> =100mA)		2	4	Ω
I <sub>PK</sub>	Peak output current		2		A
I <sub>REV</sub>	Latch protection withstands reverse current (Working cycle ≤ 2%, t ≤ 300μs, V <sub>CC</sub> =18V)		>0.5		A
t <sub>R</sub>	Rise time(V <sub>CC</sub> =18V, C <sub>LOAD</sub> =100pF)			30	ns
t <sub>F</sub>	Descent time(V <sub>CC</sub> =18V, C <sub>LOAD</sub> =100pF)			30	ns
t <sub>ON</sub>	Open transmission delay(V <sub>CC</sub> =18V, C <sub>LOAD</sub> =100pF)			70	ns
t <sub>OFF</sub>	Turn off the transmission delay(V <sub>CC</sub> =18V, C <sub>LOAD</sub> =100pF)			70	ns
I <sub>Q1</sub>	Supply current(V <sub>INA</sub> =V <sub>INB</sub> =High logic)			1	mA
I <sub>Q0</sub>	Supply current(V <sub>INA</sub> =V <sub>INB</sub> =Low logic)			1	mA

### Input/output (in-phase) waveform diagram



**Explain  
Functional Block Diagram**



**Chip working logic**

The signal input ports (INA, INB) of HX37324-S/HX27324-S adopt a level triggered mode, which means that when the voltage value meets the logic requirements, the chip will work normally, as shown in the table.

Input-output logic table			
INPUT		OUTPUT	
INA	INB	OUTA/	OUTB
L	L	H	L
H	H	L	H
L	H	H	H
H	L	L	L

Note: H represents high level; L represents low level

**Signal input port**

HX37324-S/HX27324-S has two independent signal input ports for receiving control signals from the main control, and these two ports will not interfere with each other. These input port designs have high reliability, and even if a reverse current of 500mA is forced back to their output, it will not cause damage or logical confusion. The signal input port also has the ability to directly process -10V voltage, even under the influence of large noise waveforms, the chip can still work safely, increasing the stability of the chip. It is not recommended to adjust the output waveform by adjusting the waveform slope or delay of the input port during the design process. If it is necessary to adjust the rise and fall time of the power end, it is recommended to add additional resistance between the output end and the power end. The signal input port of HX37324-S/HX27324-S has a pull-up resistor to GND. Suggest short circuiting this port to GND when not in use.

**Output port**

The output and input of HX37324-S/HX27324-S are reversed and can be used to drive P-type or N-type MOSFETs. Each output port can provide a peak pull-up or pull-down current of 2A, which is suitable for driving MOSFET designs in high-frequency applications due to its high-speed and high current characteristics.

## Application Information

The high-speed, high-current characteristics of the HX37324-S/HX27324-S are suitable for applications such as high-frequency power supplies. Typical applications include using a high-power driver chip to drive the gate voltage of the MOSFET when the PWM output level of the main control IC is not sufficient to drive the power end MOSFET, in order to ensure that the MOSFET is in a stable state.

In the high frequency and high power application environment, it is very important to ensure the stable operation of the chip. Therefore, the following recommendations are made when applying HX37324-S/HX27324-S:

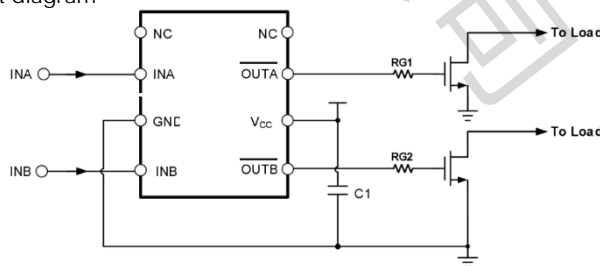
1. During the switching process, HX37324-S/HX27324-S outputs a peak switching current of 2A. As frequency increases, VCC stability may decrease. To stabilize VCC voltage, select a larger electrolytic capacitor during design and use low ESR/ESL capacitors (like ceramic or patch capacitors) in parallel to address high-frequency characteristics. Position the capacitor as close as possible to the VCC and GND pins.
2. The output port is part of the power loop; therefore, to ensure a flat output waveform, place it near the MOSFET on the power grid during design. Additionally, consider adding external resistors at OUT for smoother operating waveforms.

When achieving the best performance from high speed low side door drives, the following points need to be noted:

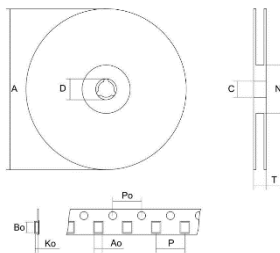
1. Connect the low ESR/ESL capacitor tightly between the VCC and GND pins of the IC to support the peak current drawn from the VDD when the MOSFET is on Time.
2. Grounding considerations:
  - The primary goal of designing grounding connections is to limit the MOSFET gate charging and discharging circuit to the smallest possible loop area, in order to reduce loop inductance and effectively avoid noise issues on the MOSFET gate. Meanwhile, the gate driver chip should be as close as possible to the MOSFET.
  - Star point grounding is a good method to reduce noise coupling between current circuits. Connect the ground point of the driver to other circuit nodes such as the source of the power MOSFET and the ground of the PWM controller. The connection path should be as short as possible to reduce inductance and as wide as possible to reduce resistance.
  - Use ground plane to shield noise. Due to the rapid rise and fall time of OUT, which may disrupt the input signal during the transition period, shielding noise through the ground plane can ensure that the input signal is not disturbed. The ground plane cannot become a conduction path for any current circuit, and the ground plane must establish a ground potential connection with the star point. In addition to shielding noise, the grounding plane can also help dissipate heat.
3. In a noisy environment, to prevent noise from causing output failures, you can connect unused pins to VDD or GND.
4. Separate the power loop from the signal loop, such as output and input signals.

Summary: When using HX37324-S/HX27324-S, it is important to ensure the stable operation of the chip in high-frequency and high-power application environments. It is recommended to adopt appropriate capacitor layout, ground layout, and shielding measures to ensure power stability and output waveform flatness.

Inverting typical application circuit diagram



## Package



Packing Method	Quantity
Tape and Reel	2500PCS/ Disk