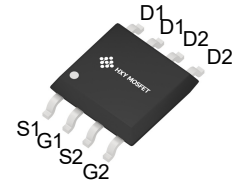




## Description

The IRF7303PBF uses advanced trench technology to provide excellent  $R_{DS(ON)}$ , low gate charge and operation with gate voltages as low as 2.5V. This device is suitable for use as a Battery protection or in other Switching application.



SOP-8

## General Features

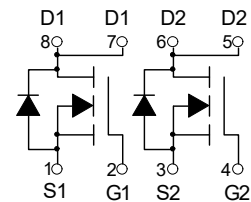
$V_{DS} = 30V$   $I_D = 6A$   
 $R_{DS(ON)} < 30m\Omega$  @  $V_{GS}=10V$   
 $R_{DS(ON)} < 42m\Omega$  @  $V_{GS}=4.5V$

## Application

Battery protection

Load switch

Uninterruptible power supply



Dual N-Channel MOSFET

## Ordering Information

Product ID	Pack	Brand	Qty(PCS)
IRF7303PBF	SOP-8	HXY MOSFET	3000

## Absolute Maximum Ratings@ $T_J=25^\circ C$ (unless otherwise specified)

Symbol	Parameter	Rating	Units
$V_{DS}$	Drain-Source Voltage	30	V
$V_{GS}$	Gate-Source Voltage	$\pm 20$	V
$I_D@T_A=25^\circ C$	Drain Current, $V_{GS}$ @ 4.5V <sup>3</sup>	6	A
$I_D@T_A=70^\circ C$	Drain Current, $V_{GS}$ @ 4.5V <sup>3</sup>	5	A
$I_{DM}$	Pulsed Drain Current <sup>1</sup>	30	A
$P_D@T_A=25^\circ C$	Total Power Dissipation	2	W
$T_{STG}$	Storage Temperature Range	-55 to 150	$^\circ C$
$T_J$	Operating Junction Temperature Range	-55 to 150	$^\circ C$
$R_{thj-a}$	Maximum Thermal Resistance, Junction-ambient <sup>3</sup>	62.5	$^\circ C/W$



**Electrical Characteristics ( $T_J=25^\circ\text{C}$ , unless otherwise noted)**

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>Static Parameters</b>						
$BV_{DSS}$	Drain-Source Breakdown Voltage	$I_D=-250\mu\text{A}$ , $V_{GS}=0\text{V}$	30			V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS}=30\text{V}$ , $V_{GS}=0\text{V}$ $T_J=55^\circ\text{C}$			1	$\mu\text{A}$
					5	
$I_{GSS}$	Gate-Body leakage current	$V_{DS}=0\text{V}$ , $V_{GS}=\pm 20\text{V}$			$\pm 100$	nA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}$ , $I_D=250\mu\text{A}$	1.2	1.8	2.4	V
$I_{D(ON)}$	On state drain current	$V_{GS}=10\text{V}$ , $V_{DS}=5\text{V}$	30			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS}=10\text{V}$ , $I_D=6\text{A}$ $T_J=125^\circ\text{C}$		25	30	m $\Omega$
				40	48	
		$V_{GS}=4.5\text{V}$ , $I_D=5\text{A}$		33	42	m $\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS}=5\text{V}$ , $I_D=6\text{A}$		15		S
$V_{SD}$	Diode Forward Voltage	$I_S=1\text{A}$ , $V_{GS}=0\text{V}$		0.76	1	V
$I_S$	Maximum Body-Diode Continuous Current				2.5	A
<b>Dynamic Parameters</b>						
$C_{iss}$	Input Capacitance	$V_{GS}=0\text{V}$ , $V_{DS}=15\text{V}$ , $f=1\text{MHz}$		255	310	pF
$C_{oss}$	Output Capacitance			45		pF
$C_{rss}$	Reverse Transfer Capacitance			35	50	pF
$R_g$	Gate resistance	$V_{GS}=0\text{V}$ , $V_{DS}=0\text{V}$ , $f=1\text{MHz}$	1.6	3.25	4.9	$\Omega$
<b>Switching Parameters</b>						
$Q_{g(10V)}$	Total Gate Charge	$V_{GS}=10\text{V}$ , $V_{DS}=15\text{V}$ , $I_D=6\text{A}$		5.2	6.3	nC
$Q_{g(4.5V)}$				2.55	3.2	nC
$Q_{gs}$	Gate Source Charge			0.85		nC
$Q_{gd}$	Gate Drain Charge			1.3		nC
$t_{D(on)}$	Turn-On Delay Time			4.5		ns
$t_r$	Turn-On Rise Time	$V_{GS}=10\text{V}$ , $V_{DS}=15\text{V}$ , $R_L=2.5\Omega$ , $R_{GEN}=3\Omega$		2.5		ns
$t_{D(off)}$	Turn-Off Delay Time			14.5		ns
$t_f$	Turn-Off Fall Time			3.5		ns
$t_{rr}$	Body Diode Reverse Recovery Time	$I_F=6\text{A}$ , $dI/dt=100\text{A}/\mu\text{s}$		8.5		ns
$Q_{rr}$	Body Diode Reverse Recovery Charge	$I_F=6\text{A}$ , $dI/dt=100\text{A}/\mu\text{s}$		2.2		nC

A. The value of  $R_{\theta JA}$  is measured with the device mounted on 1in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with  $T_A=25^\circ\text{C}$ . The value in any given application depends on the user's specific board design.

B. The power dissipation  $P_D$  is based on  $T_{J(MAX)}=150^\circ\text{C}$ , using  $\leq 10\text{s}$  junction-to-ambient thermal resistance.

C. Repetitive rating, pulse width limited by junction temperature  $T_{J(MAX)}=150^\circ\text{C}$ . Ratings are based on low frequency and duty cycles to keep initial  $T_J=25^\circ\text{C}$ .

D. The  $R_{\theta JA}$  is the sum of the thermal impedance from junction to lead  $R_{\theta JL}$  and lead to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using  $<300\mu\text{s}$  pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-ambient thermal impedance which is measured with the device mounted on 1in<sup>2</sup> FR-4 board with 2oz. Copper, assuming a maximum junction temperature of  $T_{J(MAX)}=150^\circ\text{C}$ . The SOA curve provides a single pulse rating.



### Typical Electrical And Thermal Characteristics

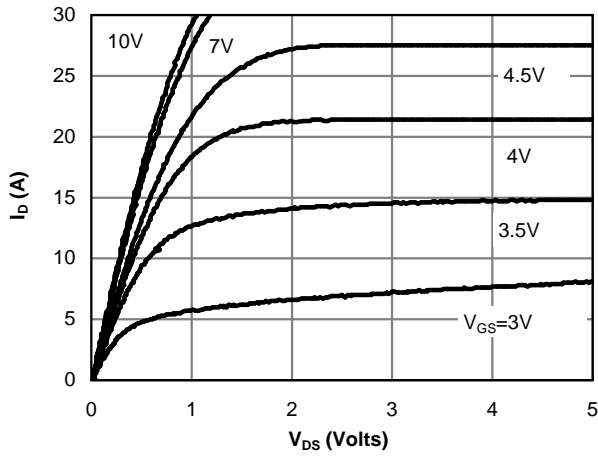


Fig 1: On-Region Characteristics (Note E)

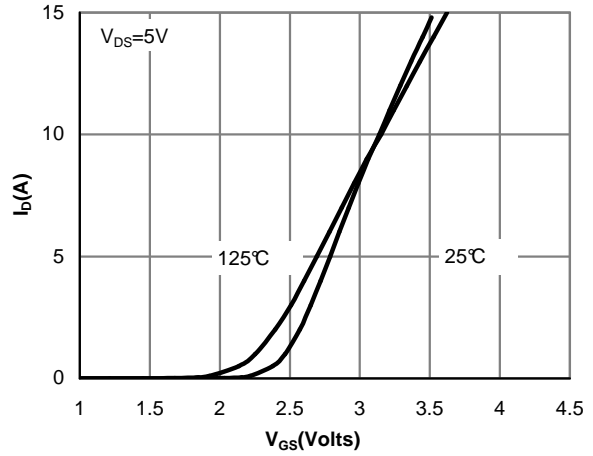


Figure 2: Transfer Characteristics (Note E)

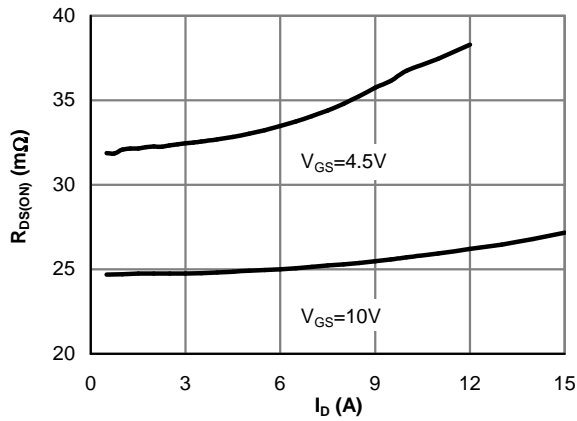


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

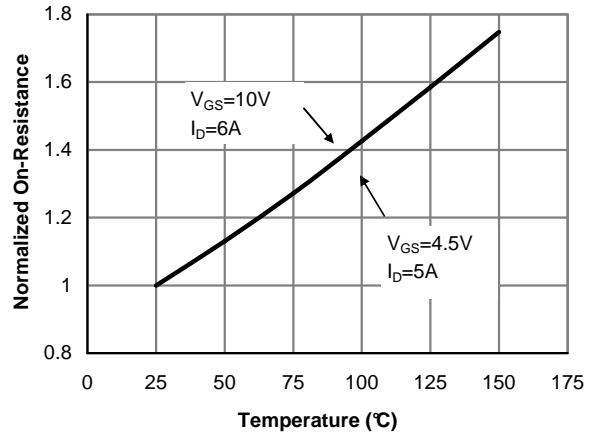


Figure 4: On-Resistance vs. Junction Temperature (Note E)

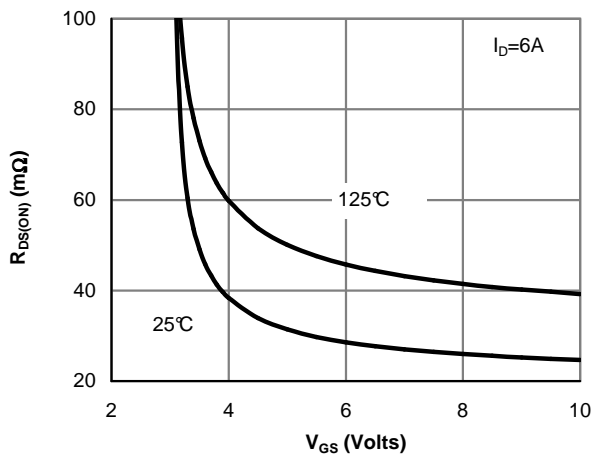


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

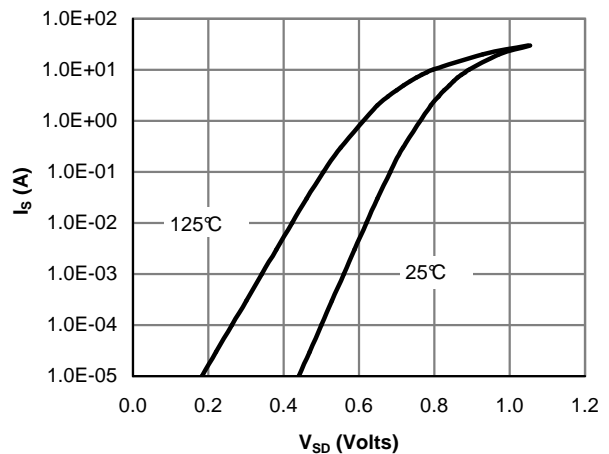


Figure 6: Body-Diode Characteristics (Note E)

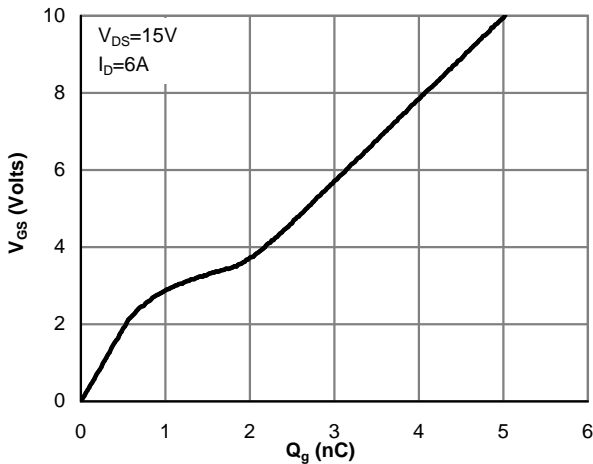


Figure 7: Gate-Charge Characteristics

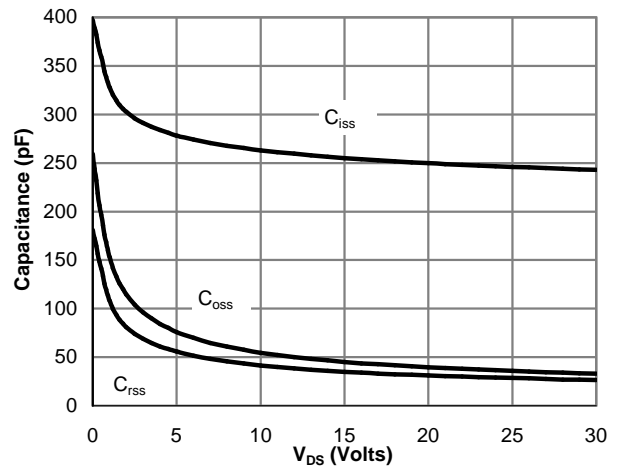


Figure 8: Capacitance Characteristics

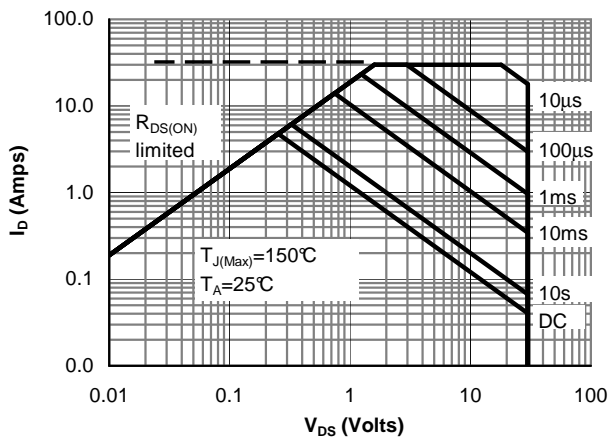


Figure 10: Maximum Forward Biased Safe Operating Area (Note F)

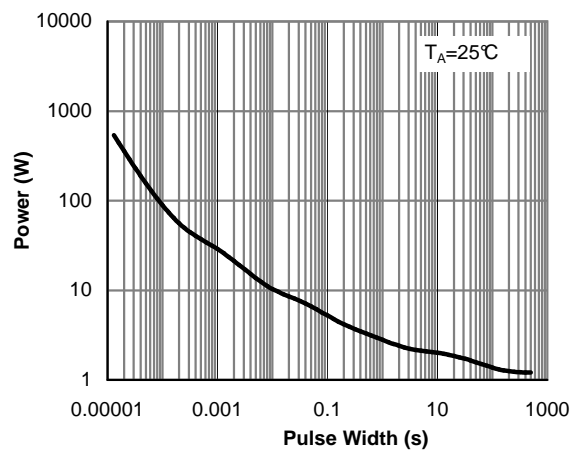


Figure 11: Single Pulse Power Rating Junction-to-Ambient (Note F)

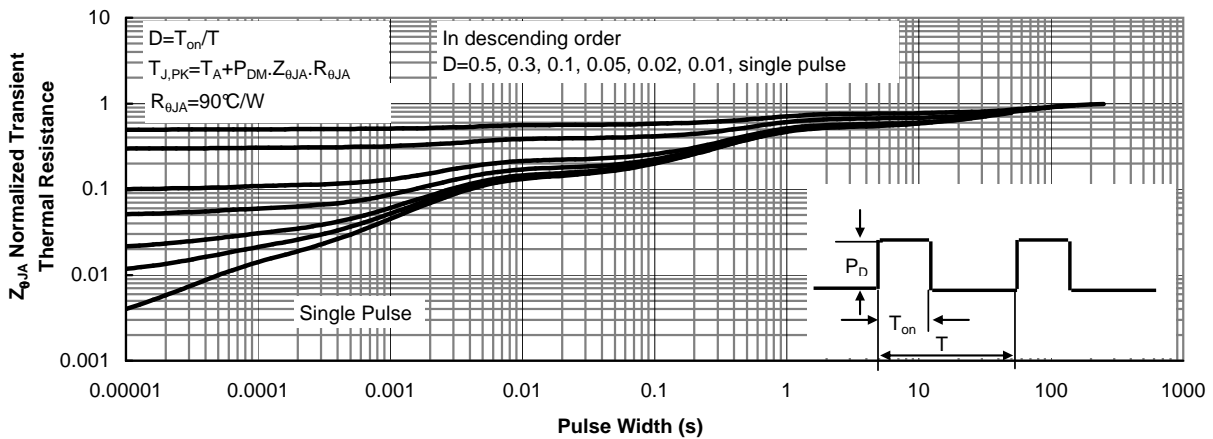
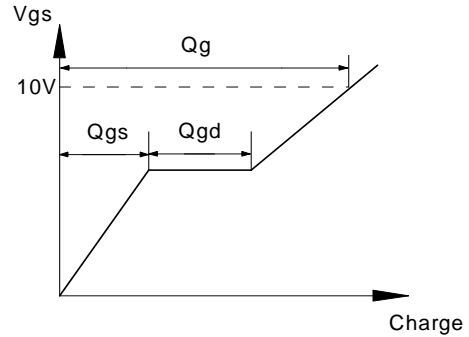
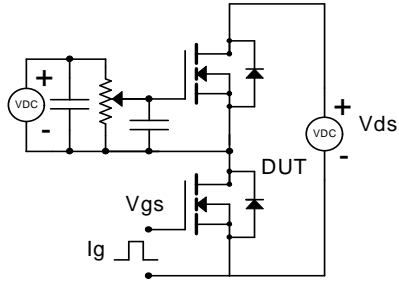


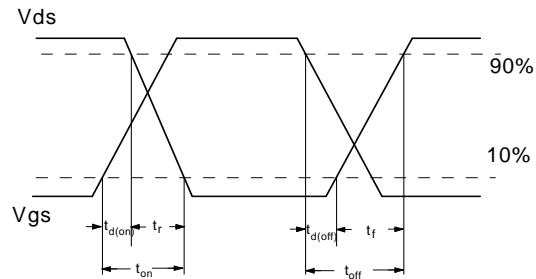
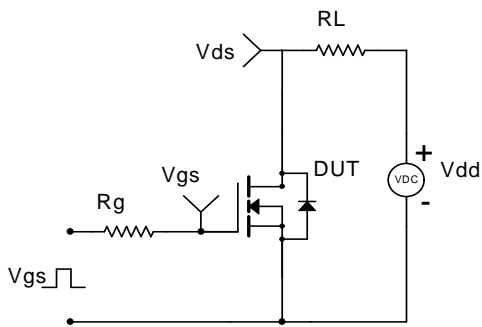
Figure 12: Normalized Maximum Transient Thermal Impedance (Note F)



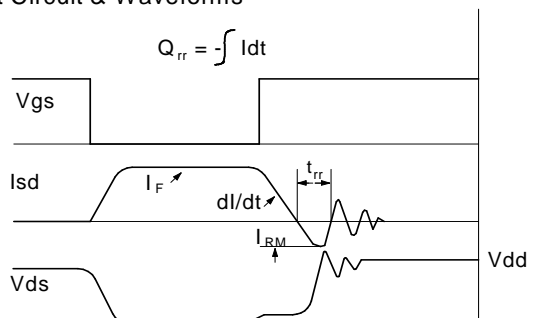
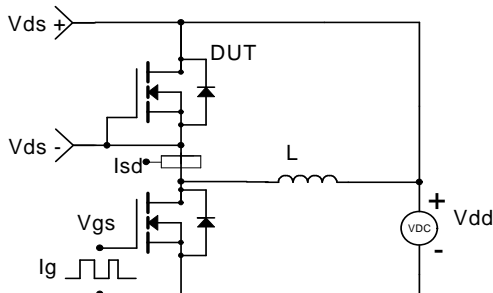
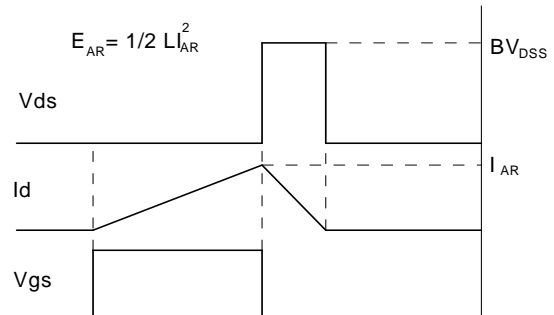
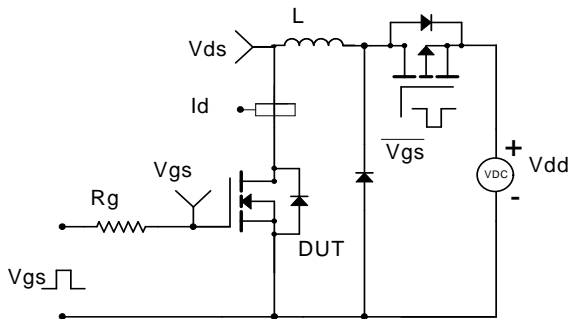
### Gate Charge Test Circuit & Waveform



### Resistive Switching Test Circuit & Waveforms

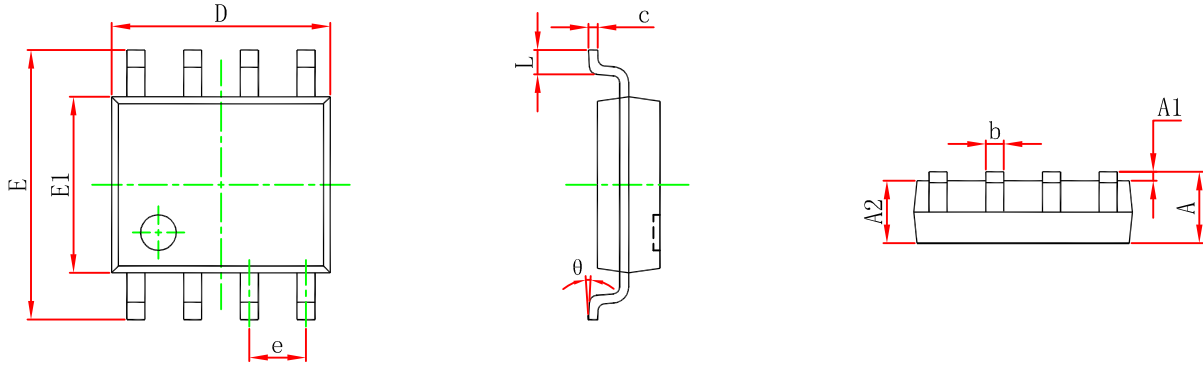


### Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

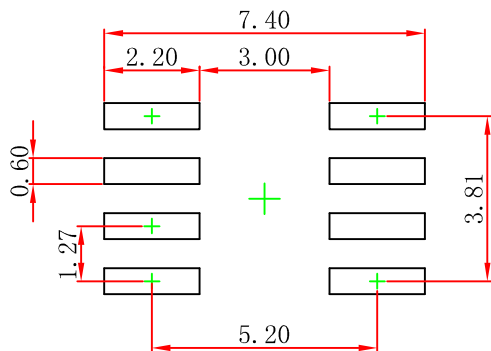




### SOP-8 Package Outline Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.800	5.000	0.189	0.197
e	1.270 (BSC)		0.050 (BSC)	
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°



Note:  
 1. Controlling dimension: in millimeters.  
 2. General tolerance:  $\pm 0.05\text{mm}$ .  
 3. The pad layout is for reference purposes only.



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