## General Description

The JSM2019 series are a group of low-dropout (LDO) voltage regulators offering the benefits of wide input voltage range from 2.3V to 6V, low dropout voltage, low power consumption, and miniaturized packaging.

With fast instantaneous response, it is suitable for product applications that require fast loading speed in an instant. There is an option of shutdown mode by selecting the parts with the EN pin and pulling it low. The shutdown current in this mode goes down to only 100nA (typical).

The JSM2019 series of linear regulators are stable with the ceramic output capacitor over its wide input range from 2.3V to 6V and the entire range of output load current (0mA to 300mA).
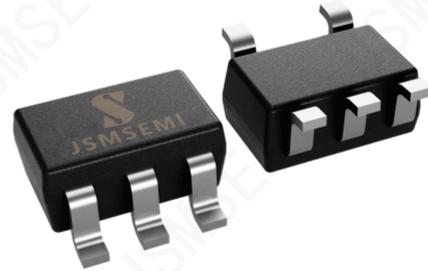
SOT-23-5

Features

- Fast Transient Response
- ±2% Output Accuracy
- 300mA Output Current
- 100nA Disable Current (by option)
- Wide Operating Input Voltage Range: 2.3V to 6V
- Dropout Voltage: 0.06V at 100mA / V_{OUT} 3.3V
- Support Fixed Output Voltage 1.8V, 3.3V
- Stable with Ceramic or Tantalum Capacitor
- Current Limit Protection
- Over-Temperature Protection
- Packages Available

Applications

- Portable, Battery Powered Equipment
- Low Power Microcontrollers
- Laptop, Palmtops and PDAs
- Wireless Communication Equipment
- Audio/Video Equipment
- Car Navigation Systems

Ordering Information

Order number	Package	Operation Temperature Range	MSL Grade	Ship, Quantity	Green
JSM2019-1.8YN5G/TR	SOT-23-5	-40 to 125°C	3	T&R,3000	Rohs
JSM2019-3.3YN5G/TR	SOT-23-5	-40 to 125°C	3	T&R,3000	Rohs
JSM2019-ADJYN5G/TR	SOT-23-5	-40 to 125°C	3	T&R,3000	Rohs

Pin Configurations

SOT-23-5
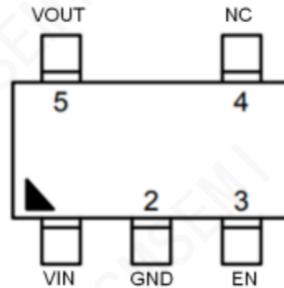
Description of Functional Pins

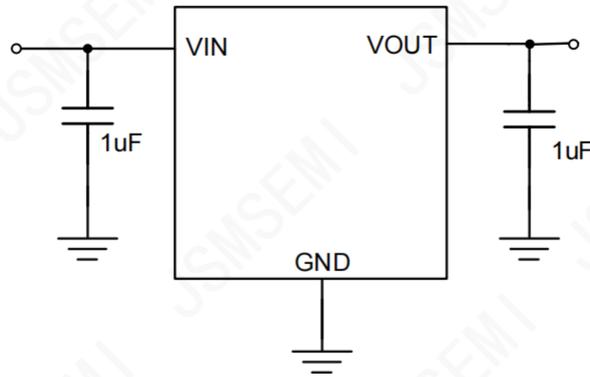| Pin No SOT-23-5	Pin Name	Pin Function
2	GND	Ground
5	VOUT	Output of the Regulator
1	VIN	Input of Supply Voltage.
3	EN	Enable Control Input.
4	NC	No internal connection

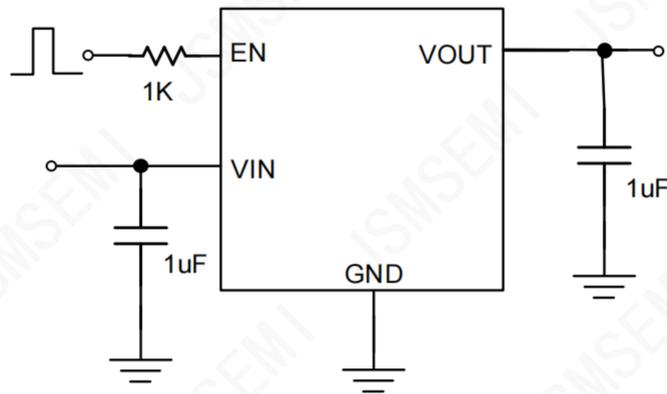## Typical Application Circuit

Figure 1: Application circuit of Fixed V_{OUT} LDO

Figure 2: Application circuit of Fixed V_{OUT} LDO with enable function

Absolute Maximum Ratings (Note 1)

VIN to GND --- -0.3V to 7V

VOUT, EN to GND --- -0.3V to 6V

VOUT to VIN --- -6V to 0.3V

Package Thermal Resistance (Note 2)

SOT-23-5, θ_{JA} --- 220 ºC /W

Lead Temperature (Soldering, 10 sec.) ---------------------------------------260 ºC

Junction Temperature --150 ºC

Storage Temperature Range --- -60 ºC to 150 ºC

ESD Susceptibility

HBM -- 2KV

MM -- 200V

CDM -- 2KV

Recommended Operating Conditions

Input Voltage VIN -- 2.3V to 6V

Junction Temperature Range -- -40 ºC to 125 ºC

Ambient Temperature Range -- -40 ºC to 85 ºC

Function Block Diagram
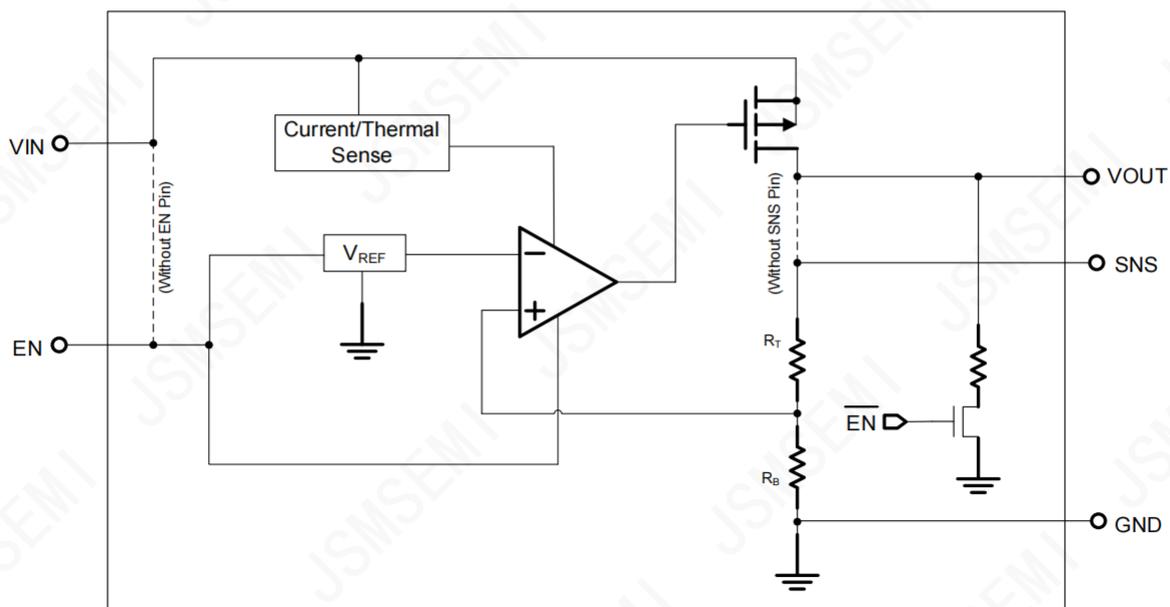
Electrical Characteristics(V_{IN} =5V, V_{EN} = 5V T_A=25°C unless otherwise specified)

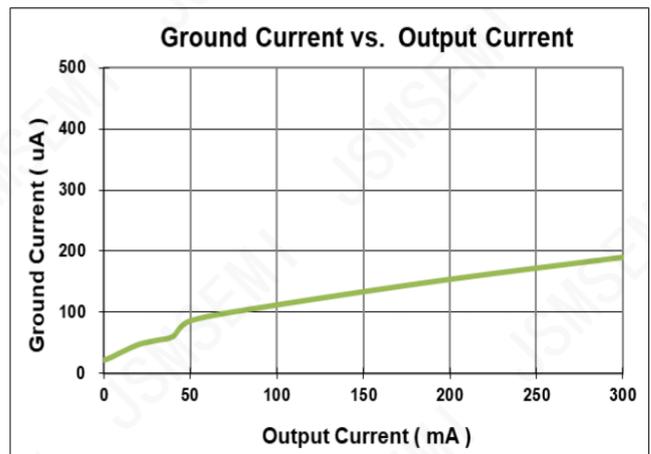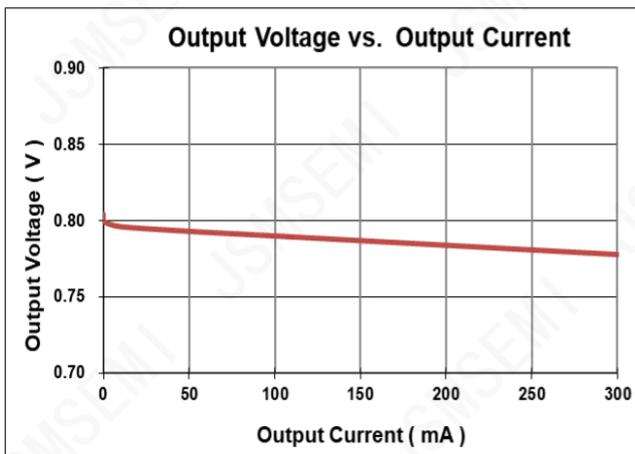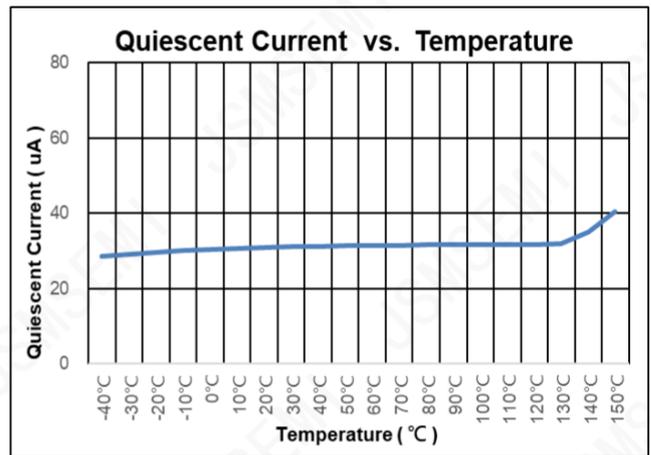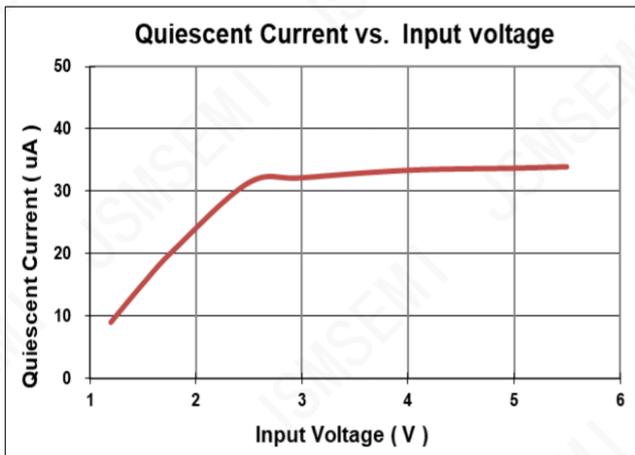| Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Supply Voltage	V_{IN}			2.3	--	6.0	V
DC Output Voltage Accuracy		I_{LOAD} =0.1mA		-2		2	%
Dropout Voltage (I_{LOAD} =100mA) (Note 3)	V_{DROP_3V}	V_{OUT} ≥ 3V			0.06		V
	$V_{DROP\_2.5V}$	V_{OUT} = 2.5V			0.08		
	$V_{DROP\_1.8V}$	V_{OUT} = 1.8V			0.09		
	$V_{DROP\_1.5V}$	V_{OUT} = 1.5V			0.12		
	$V_{DROP\_1.2V}$	V_{OUT} = 1.2V			0.15		
	$V_{DROP\_0.8V}$	V_{OUT} = 0.8V			0.18		
	$V_{DROP\_0.5V}$	V_{OUT} = 0.5V			0.23		
Ground Current	I_Q	I_{LOAD} = 0mA			30		µA
Shutdown Ground Current	I_{SD}	V_{EN} = 0V, V_{OUT} = 0V			0.1	0.5	µA
Enable Threshold Voltage	V_{IH}	EN Rising		1.0			V
	V_{IL}	EN Falling				0.4	
EN Input Current	I_{EN}	V_{EN} = 5V			10	100	nA
Line Regulation	ΔLINE	I_{LOAD} =30mA, 2.5V ≤ V_{IN} ≤ 5.5V or (V_{OUT} + 0.2V) ≤ V_{IN} ≤ 5.5V			0.3		%
Load Line	ΔLOAD	1mA ≤ I_{LOAD} ≤ 300mA			20		mV
Output Current Limit	I_{LIM}	V_{OUT} = 0V		301	550		mA
Power Supply Rejection Ratio (I_{LOAD} =5mA)	PSRR	V_{OUT} =0.8V, V_{IN} = 5V	f = 100Hz	--	55	--	dB
			f = 1kHz	--	60	--	
Output Voltage Noise (BW = 10Hz to 100kHz, C_{OUT} =1µF,)		V_{IN} = 3.5V I_{LOAD} =0.1A	V_{OUT} =0.8V	--	120	--	µV_{RMS}
			V_{OUT} =2.8V	--	180	--	
Thermal Shutdown Temperature	T_{SD}	I_{LOAD} =10mA		--	160	--	°C
Thermal Shutdown Hysteresis	$ΔT_{SD}$			--	20	--	°C
Discharge Resistance	R_{DC}	EN = 0V , V_{OUT} = 0.1V		--	30	--	Ω

Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ$_{JA}$ is measured at T_A = 25°C on a JSMSEMI EVB board.

Note 3. V_{DROP} = V_{IN} − V_{OUT} when the V_{OUT} is 98% of its target value.

Typical Characteristics

Output Voltage vs. Input voltage

Output Voltage vs. Temperature

Quiescent Current vs. Input voltage

Quiescent Current vs. Temperature

Output Voltage vs. Output Current
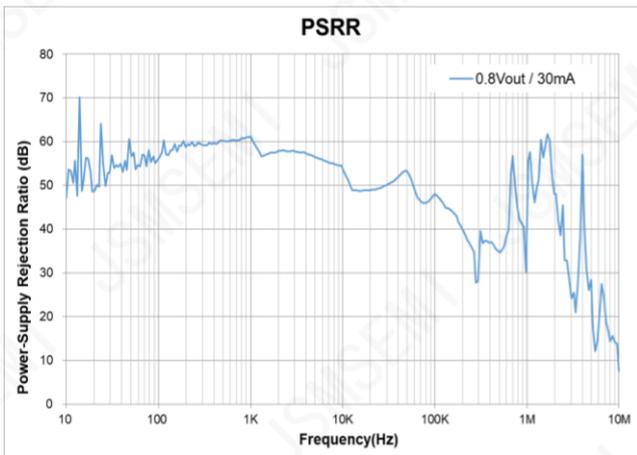

Ground Current vs. Output Current
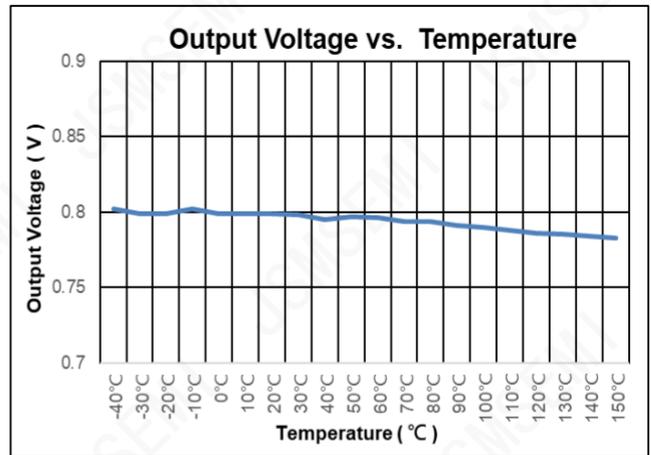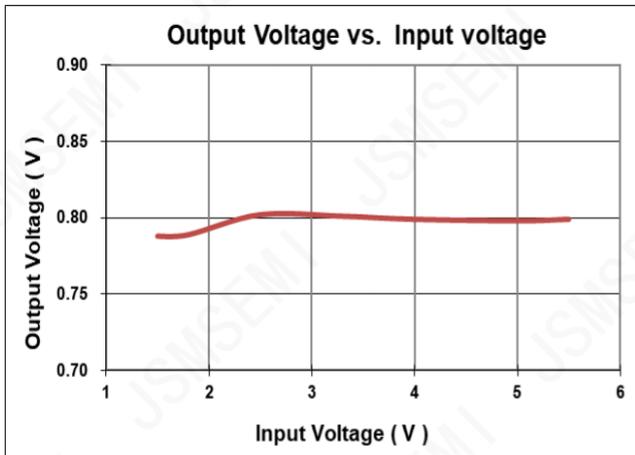
Load Transient Response

Current Limit

PSRR vs. Frequency

Application Guideline

Input and Output Capacitor Requirements

The external input and output capacitors of JSM2019 series must be properly selected for stability and performance. Use a 1μF or larger input capacitor and place it close to the IC's V_{IN} and GND pins. Any output capacitor meeting the minimum 1mΩ ESR (Equivalent Series Resistance) and effective capacitance between 1μF and 22μF requirement may be used. Place the output capacitor close to the IC's V_{OUT} and GND pins. Increasing capacitance and decreasing ESR can improve the circuit's PSRR and line transient response.

Current Limit

The JSM2019 series contain the current limiter of output power transistor, which monitors and controls the transistor, limiting the output current to 550mA (typical). The output can be shorted to ground indefinitely without damaging the part.

Dropout Voltage

The JSM2019 series use a PMOS pass transistor to achieve low dropout. When ($V_{IN} - V_{OUT}$) is less than the dropout voltage (V_{DROP}), the PMOS pass device is in the linear region of operation and the input-to-output resistance is the $RDS_{(ON)}$ of the PMOS pass element. V_{DROP} scales approximately with the output current because the PMOS device behaves as a resistor in dropout condition.

As any linear regulator, PSRR and transient response are degraded as ($V_{IN} - V_{OUT}$) approaches dropout condition.

Layout Consideration

By placing input and output capacitors on the same side of the PCB as the LDO, and placing them as close as is practical to the package can achieve the best performance. The ground connections for input and output capacitors must be back to the JSM2019 ground pin using as wide and as short of a copper trace as is practical.

Connections using long trace lengths, narrow trace widths, and/or connections through via must be avoided. These add parasitic inductances and resistance that results in worse performance especially during transient conditions.

OTP (Over Temperature Protection)

The over temperature protection function of JSM2019 series will turn off the P-MOSFET when the junction temperature exceeds 160°C (typ.). Once the junction temperature cools down by approximately 20°C, the regulator will automatically resume operation.

Thermal Application

For continuous operation, do not exceed the absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated as below:
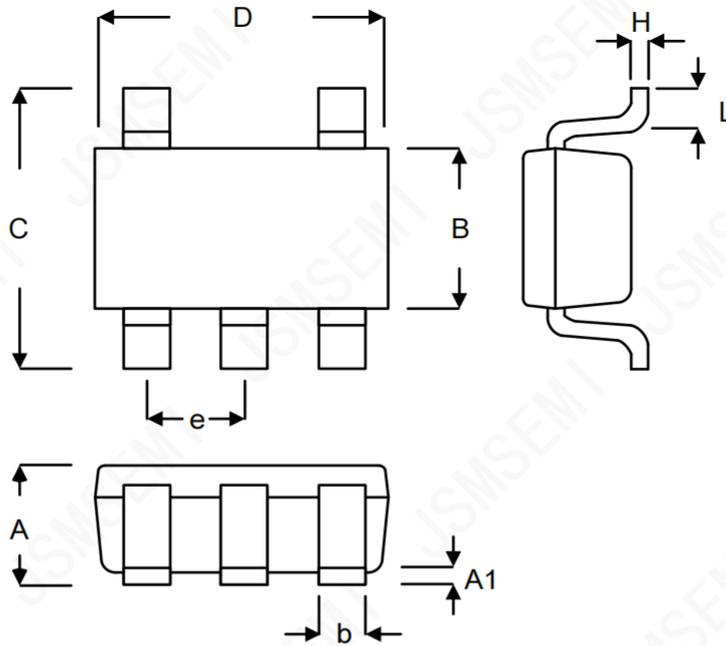
T_A=25°C, JSMSEMI PCB,

The max PD (Max) = (125°C − 25°C) / (220°C/W) = 0.45W for SOT-23-5 packages.

Power dissipation (PD) is equal to the product of the output current and the voltage drop across the output pass element, as shown in the equation below:

PD = (VIN – VOUT) × IOUT

SOT-23-5L

Symbol	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	0.889	1.295	0.035	0.051
A1	0.000	0.152	0.000	0.006
B	1.397	1.803	0.055	0.071
b	0.250	0.560	0.010	0.022
C	2.591	2.997	0.102	0.118
D	2.692	3.099	0.106	0.122
e	0.838	1.041	0.033	0.041
H	0.080	0.254	0.003	0.010
L	0.300	0.610	0.012	0.024