UMW SN74LVC1G57

Low-power Configurable Multiple Function Gate

1.Description

The SN74LVC1G57 is a configurable multiple function gate with Schmitt-trigger inputs. The device can be configured as any of the following logic functions AND, OR, NAND, NOR, XNOR, inverter and buffer; using the 3-bit input. All inputs can be connected directly to VCC or GND. Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in mixed 3.3 V and 5V environments. This device is fully specified for partial power down applications using IOFF. The IOFF circuitry disables the output, preventing the potentially damaging back-flow current through the device when it is powered down.

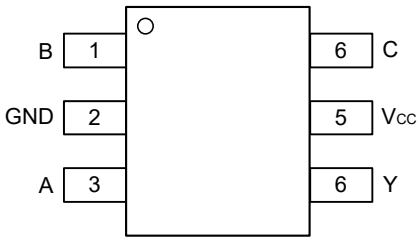
2.Applications

- Active Noise Cancellation (ANC)
- Bar-code Scanners
- Blood Pressure Monitors
- CPAP Machines
- Cable Solutions
- Embedded PCs
- Field Transmitter: Temperature or Pressure Sensors
- HVAC: Heating, Ventilating and Air Conditioning
- TVs: High-Definition (HDTV), LCD and Digital
- Video Communications Systems

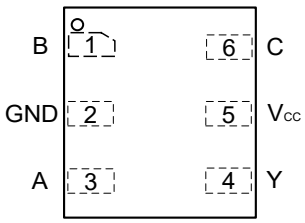
3.Features

- Wide Supply Voltage Range from 1.65V to 5.5V
- Over-voltage Tolerant Inputs to 5.5V
- High Noise Immunity
- ±24mA Output Drive (VCC=3.0V)
- CMOS Low Power Dissipation
- Latch-up Performance Exceeds 250mA
- Direct Interface with TTL Levels
- I_{OFF} Circuitry Provides Partial Power-down Mode Operation
- Multiple Package Options
- Complies with JEDEC Standard:
  --JESD8-7 (1.65V to 1.95V)
  --JESD8-5 (2.3V to 2.7V)
  --JESD8B/JESD36 (2.7V to 3.6V)
- ESD protection:
  --HBM JESD22-A114 exceeds 2000V
  --CDM JESD22-C101 exceeds 200V
- Specified from -40°C to +85°C and -40°C to +125°C

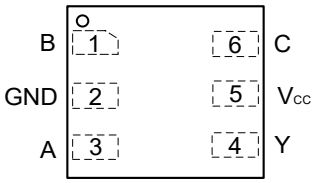
4.Pinning Information



SC70-6/SOT23-6



DFN6(1*1.5)



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Pin Function (74LVC1G57DCK/DBV/DSF/DRY)

Pin No.	Pin Name	Function
1	B	Data Input
2	GND	Ground
3	A	Data Input
4	Y	Data Output
5	V_{CC}	Supply Voltage
6	C	Data Input

5.Block Diagram

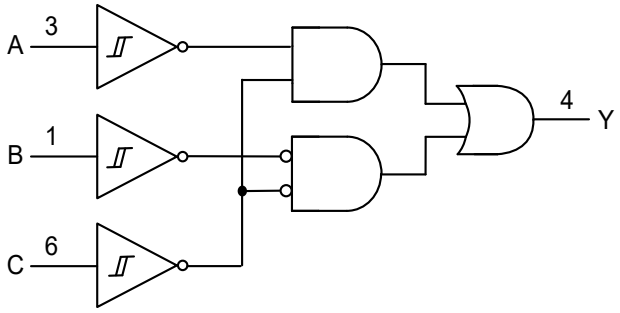


Figure2. Logic Symbol

Function Table

Input			Output
C	**B**	**A**	**Y**
L	L	L	H
L	L	H	L
L	H	L	H
L	H	H	L
H	L	L	L
H	L	H	L
H	H	L	H
H	H	H	H

6.Function Selection Table

Logic Function	Figure
2-input AND	See Fig 3.
2-input AND with both Inputs Inverted	See Fig 6.
2-input NAND with Inverted Input	See Fig 4. and Fig 5.
2-input OR with Inverted Input	See Fig 4. and Fig 5.
2-input NOR	See Fig 6.
2-input NOR with both Inputs Inverted	See Fig 3.
2-input XNOR	See Fig 7.
Inverter	See Fig 8.
Buffer	See Fig 9.

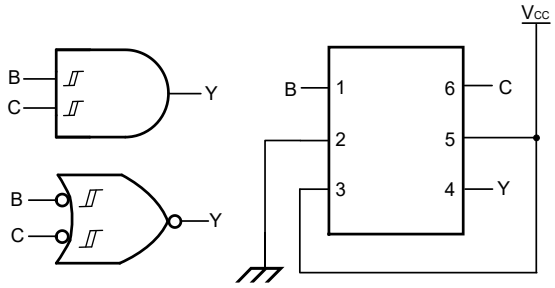


Fig3. 2-input AND gate or
2-input NOR gate with both inputs inverted

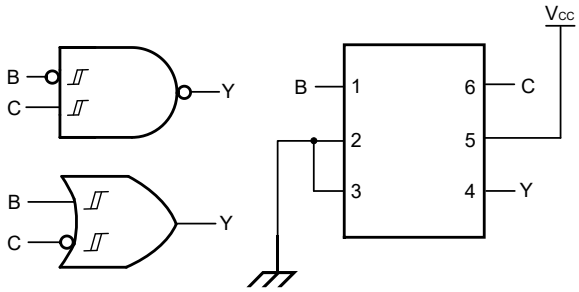


Fig4. 2-input NAND gate with input B inverted or
2-input OR gate with inverted C input

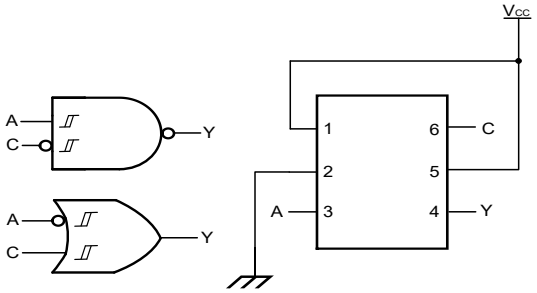


Fig5. 2-input NAND gate with input C inverted or
2-input OR gate with inverted A input

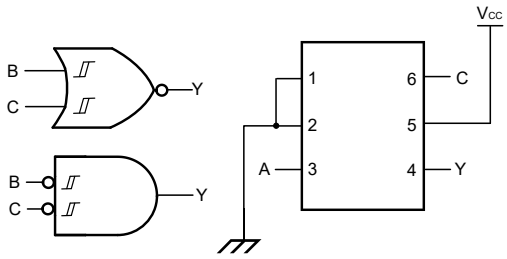


Fig6. 2-input NOR gate or
2-input AND gate with both inputs inverted

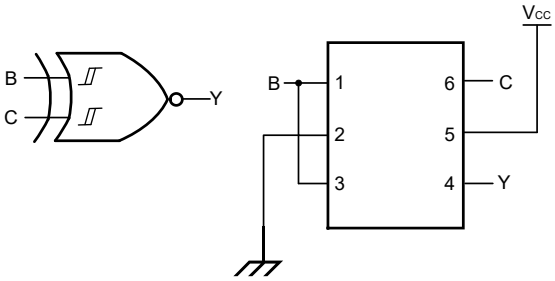


Fig7. 2-input XNOR gate

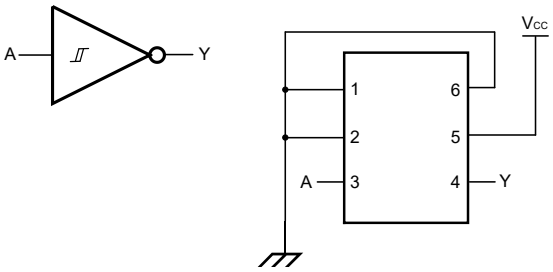
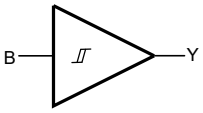


Fig8. Inverter



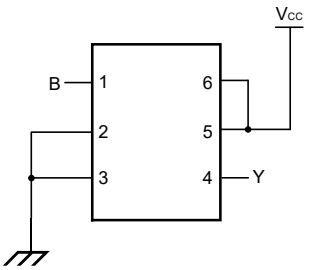


Fig 9. Buffer

7.Absolute Maximum Ratings

Parameter	Symbol	Conditions	Value	Units
DC Supply Voltage	V_{CC}		-0.5 to 6.5	V
Input Clamping Current	I_{IK}		-50	mA
Input Voltage (1)	V_I	V_I<0V	-0.5 to 6.5	V
Output Clamping Current	I_{OK}	V_O>V_{CC} or V_O<0V	±50	mA
Output Voltage (1)	V_O	V_O>V_{CC} or V_O<0V	-0.5 to 6.5	V
		Power-down mode; V_{CC}=0V	-0.5 to 6.5	V
Output Current	I_O	V_O=0V to V_{CC}	±50	mA
Supply Current	I_{CC}		100	mA
Ground Current	I_{GND}		-100	mA
Max Junction Temperature	T_J		150	°C
Storage Temperature Range	T_{STG}		-65 to 150	°C
HBM(JESD22-A114)	V_{ESD}		±4000	V
CDM(JESD22-C101)			±1500	V

Stresses exceeding those listed in this table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Note1:The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

8.Thermal Characteristics

Ratings	Package	Symbol	Value	Units
Thermal Characteristics, Thermal Resistance, Junction-to-Air	SC70-6	$R_{\theta JA}$	TBD	°C/W
	SOT23-6		TBD	
	DFN6(1.50×1.00)		TBD	
	DFN6(1.00×1.00)		TBD	
Power Dissipation in Still Air at 25°C	SC70-6	P_D@25°C	TBD	mW
	SOT23-6		TBD	
	DFN6(1.50×1.00)		TBD	
	DFN6(1.00×1.00)		TBD	

9.Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit
Supply Voltage Range	V_{CC}	1.65	5.5	V
Input Voltage	V_I	0	5.5	V
Output Voltage	V_O	0	V_{CC}	V
Ambient Temperature	T_A	-40	125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied.

10.1 Electrical Characteristics (Static Characteristics)

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Parameter	Symbol	Condition	V_{CC}(V)	−40°C≤T_A≤85°C			−40°C≤T_A≤125°C		Units
				Min	Typ(2)	Max	Min	Max	
LOW-level Output Voltage	V_{OL}	V_I=V_{T+} or V_{T-}							
		I_O=100μA	1.65V to 5.5V			0.1		0.1	V
		I_O=4mA	1.65V			0.45		0.7	V
		I_O=8mA	2.3V			0.3		0.45	V
		I_O=12mA	2.7V			0.4		0.6	V
		I_O=24mA	3V			0.55		0.8	V
		I_O=32mA	4.5V			0.55		0.8	V
HIGH-level Output Voltage	V_{OH}	V_I=V_{T+} or V_{T-}							
		I_O=-100μA	1.65V to 5.5V	V_{CC}-0.1			V_{CC}-0.1		V
		I_O=-4mA	1.65V	1.2			0.95		V
		I_O=-8mA	2.3V	1.9			1.7		V
		I_O=-12mA	2.7V	2.2			1.9		V
		I_O=-24mA	3V	2.3			2		V
		I_O=-32mA	4.5V	3.8			3.4		V
Input Leakage Current	I_I	V_I=5.5V or GND	0V to 5.5V		±0.1	±1		±1	μA
Power-Off Leakage Current	I_{off}	V_I or V_O=5.5V	0V		±0.1	±2		±2	μA
Supply Current	I_{CC}	V_I=5.5V or GND,I_O=0A	1.65V to 5.5V		0.1	4		4	μA
Additional Supply Current	ΔI_{CC}	V_I=V_{CC}-0.6V, I_O=0A	2.3V to 5.5V		5	500		500	μA
Input Capacitance	C_i	Input Capacitance			2.5				pF

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Note2: Typical values are measured at maximum V_{CC} and T_A=25°C.

10.2 Electrical Characteristics (Dynamic Characteristics)

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig 10.

Parameter	Symbol	Condition	V_{CC}(V)	−40°C≤T_A≤85°C			−40°C≤T_A≤125°C		Units
				Min	Typ(2)	Max	Min	Max	
Propagation Delay	T_{PD}	A, B, C to Y; See Fig.10(3)	tPHL						
			1.65V to 1.95V	2	10	15	2	18	ns
			2.3V to 2.7V	1.5	7	11	1.5	14	ns
			2.7V	1.5	6.7	10.5	1.5	13	ns
			3V to 3.6V	1.5	7	10	1.5	12	ns
			4.5V to 5.5V	1.5	5.5	9.5	1.5	11	ns
			tPLH						
			1.65V to 1.95V	4	20	29	4	32	ns
			2.3V to 2.7V	3	17.6	25	3	28	ns
			2.7V	3	19.2	24	3	27	ns
			3V to 3.6V	3	15.5	23	3	26	ns
			4.5V to 5.5V	3	13.5	21	3	24	ns
Power Dissipation Capacitance	C_{PD}	V_I=GND to V_{CC} (4)	3.3V		22				pF

Note3: T_{pd} is the same as T_{PLH} and T_{PHL}.

Note4: C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D=C_{PD} \times V_{CC}{}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}{}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

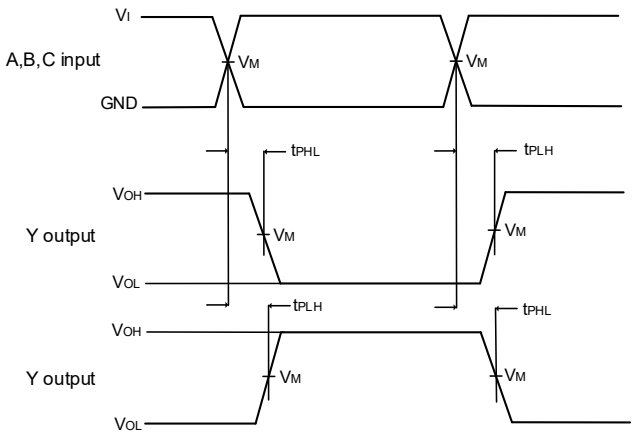
$\Sigma(C_L \times V_{CC}{}^2 \times f_o)$ = sum of outputs.

10.3 Electrical Characteristics (Transfer Characteristics)

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Parameter	Symbol	Condition	−40°C≤T_A≤85°C			−40°C≤T_A≤125°C		Units
			Min	Typ(2)	Max	Min	Max	
Positive-going Threshold Voltage	V_{T+}	See Fig.12, Fig.13, Fig.14 and Fig.15						
		V_{CC}=1.8V	0.95	1.2	1.45	0.9	1.4	V
		V_{CC}=2.3V	1.25	1.5	1.75	1.15	1.7	V
		V_{CC}=3V	1.6	1.9	2.15	1.5	2.1	V
		V_{CC}=4.5V	2.45	2.7	2.95	2.4	2.9	V
		V_{CC}=5.5V	2.85	3.1	3.35	2.8	3.3	V
Negative-going Threshold Voltage	V_{T-}	See Fig.12, Fig.13, Fig.14 and Fig.15						
		V_{CC}=1.8V	0.4	0.6	0.8	0.4	0.83	V
		V_{CC}=2.3V	0.58	0.77	1	0.58	1.03	V
		V_{CC}=3V	0.8	1.04	1.3	0.8	1.33	V
		V_{CC}=4.5V	1.21	1.55	1.9	1.21	1.93	V
		V_{CC}=5.5V	1.5	1.92	2.34	1.5	2.36	V
Hysteresis Voltage	V_H	(V_{T+} - V_{T-}) See Fig.12, Fig.13, Fig.14 and Fig.15						
		V_{CC}=1.8V	0.4	0.6	0.95	0.33	0.95	V
		V_{CC}=2.3V	0.5	0.73	0.97	0.43	0.97	V
		V_{CC}=3V	0.6	0.82	1.05	0.54	1.05	V
		V_{CC}=4.5V	0.7	1.05	1.3	0.64	1.3	V
		V_{CC}=5.5V	0.75	1.2	1.55	0.69	1.55	V

11.Test Circuit



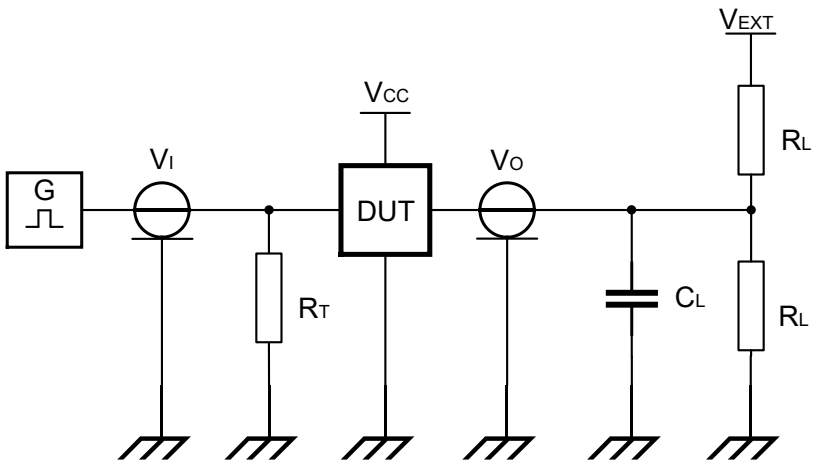
Measurement points are given in Table 1.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig.10 Input A, B and C to output Y propagation delay times

Table 1.Measurement Points

Supply Voltage	Input		Output
V_{CC}	V_M	V_I	V_M
1.65V to 1.95V	0.5 × V_{CC}	V_{CC}	0.5 × V_{CC}
2.3V to 2.7V	0.5 × V_{CC}	V_{CC}	0.5 × V_{CC}
2.7V	1.5V	2.7V	1.5V
3.0V to 3.6V	1.5V	2.7V	1.5V
4.5V to 5.5V	0.5 × V_{CC}	V_{CC}	0.5 × V_{CC}



Measurement points are given in Table 2.

Definitions test circuit:

R_L = Load resistance;

C_L = Load capacitance including jig and probe capacitance;

R_T = Termination resistance should be equal to output impedance Z_O of the pulse generator;

V_{EXT} = External voltage for measuring switching times.

Fig.11 Test circuit for measuring switching times

Table 2.Test Data

Supply Voltage	Input		Load		V_{EXT}
V_{CC}	V_I	$t_r=t_f$	C_L	R_L	t_{PLH}, t_{PHL}
1.65V to 1.95V	V_{CC}	≤2.0ns	30pF	1kΩ	open
2.3V to 2.7V	V_{CC}	≤2.0ns	30pF	500Ω	open
2.7V	2.7V	≤2.5ns	50pF	500Ω	open
3.0V to 3.6V	2.7V	≤2.5ns	50pF	500Ω	open
4.5V to 5.5V	V_{CC}	≤2.5ns	50pF	500Ω	open

12.Wave-forms Transfer Characteristics

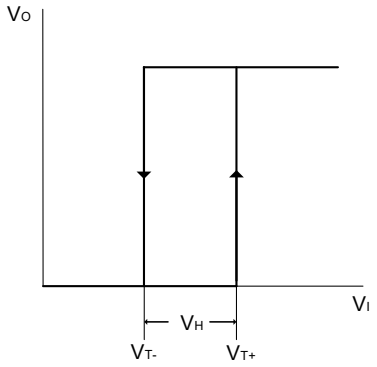
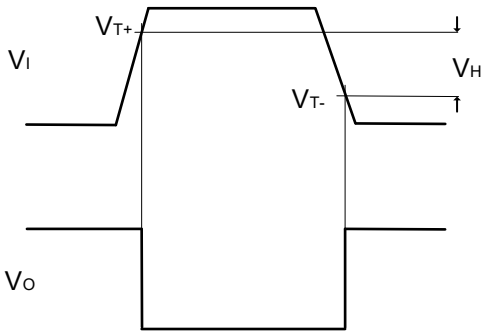


Fig. 12. Transfer characteristic



V_{T+} and V_{T-} limits are at 70 % and 20 %

Fig. 13. Definition of V_{T+} , V_{T-} and V_H

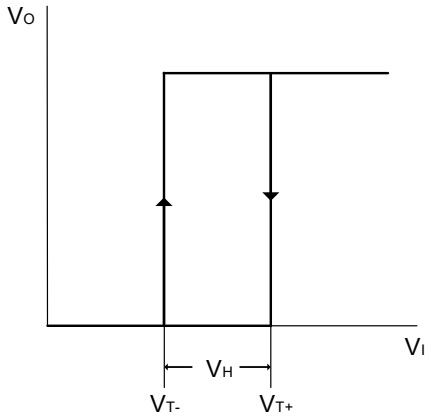
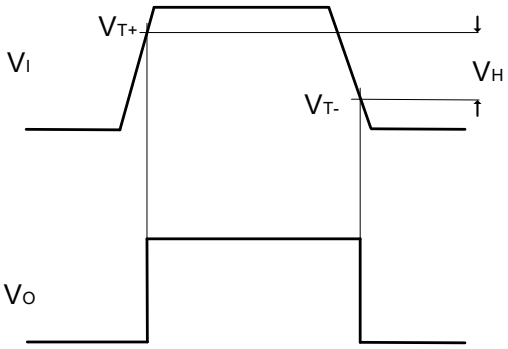


Fig. 14. Transfer characteristic



V_{T+} and V_{T-} limits are at 70 % and 20 %

Fig. 15. Definition of V_{T+} , V_{T-} and V_H

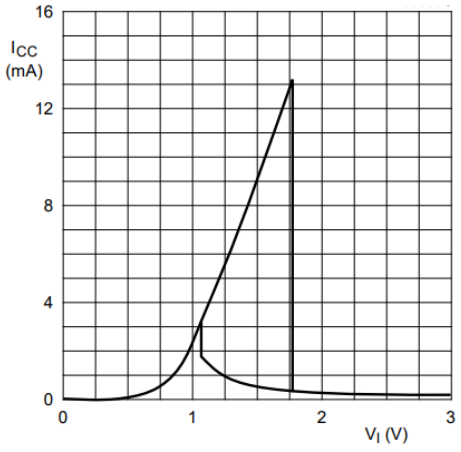


Fig 16. Typical SN74LVC1G57 transfer characteristic; V_{CC} = 3.0 V

13.Application Circuits

This application shows the SN74LVC1G57 configured as an OR gate with an inverted input. This particular configuration is helpful for dual sensor or switch applications where one of the inputs is normally closed or a logic high 1. Normally this application would require two external gates, but because the SN74LVC1G57 can be configured to meet this function the application can be implemented with a single chip solution.

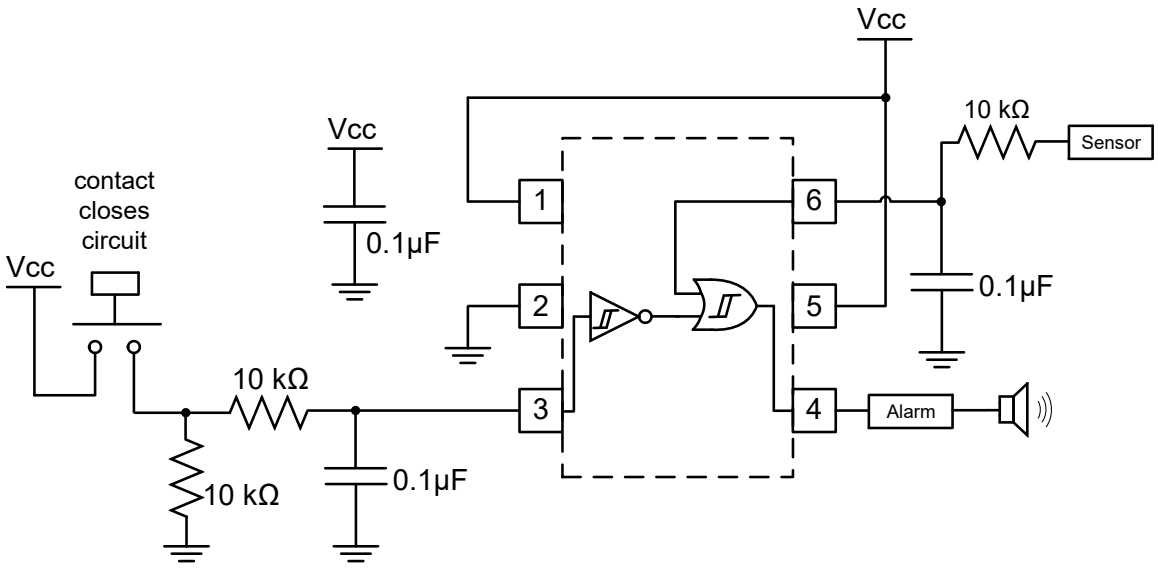
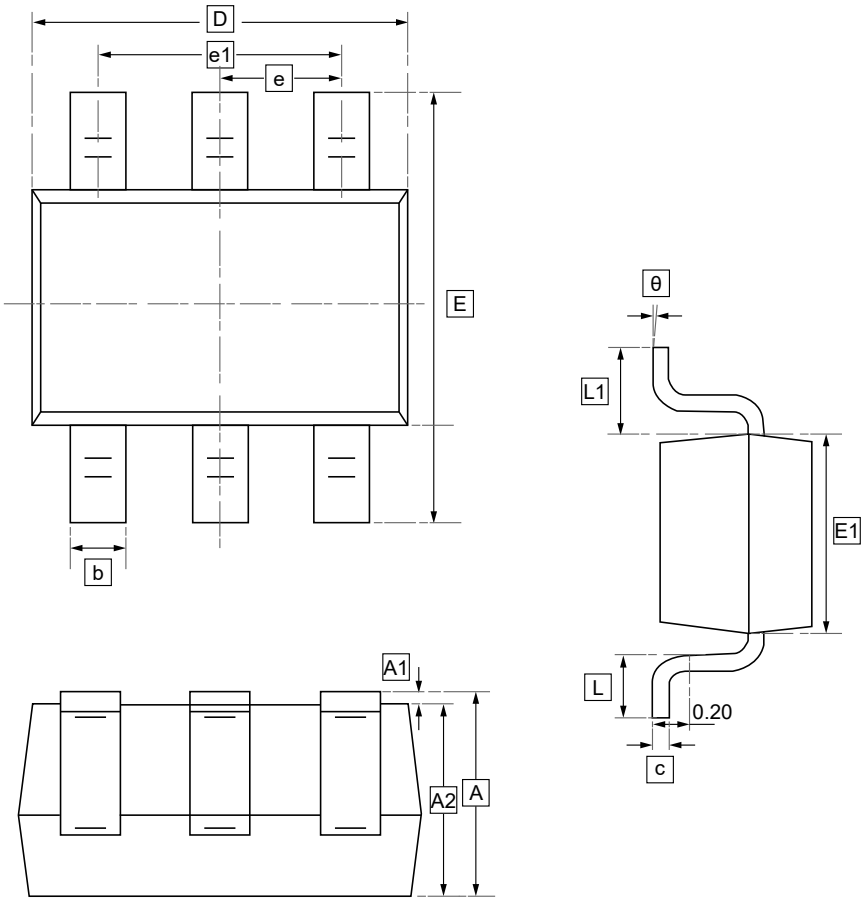


Fig 19. Dual-Sensor Alarm Trigger (5)

Note5: This application circuit is for reference only.

14.1 SC70-6 Package Outline Dimensions

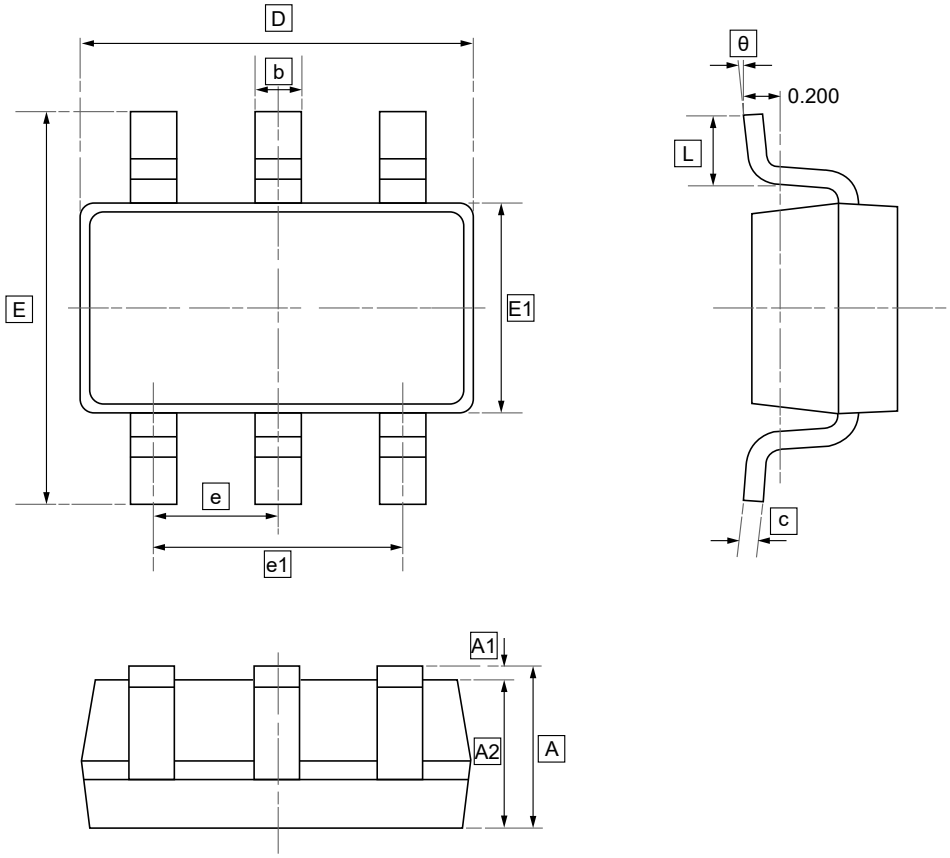


DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A2	b	c	D	E	E1	e	e1	L	L1
Min	0.90	0.00	0.90	0.15	0.08	2.05	2.15	1.15	0.65	1.2	0.26	0.525
Max	1.10	0.10	1.00	0.35	0.15	2.25	2.45	1.35	TYP.	1.4	0.46	REF.

Symbol	θ
Min	0°
Max	8°

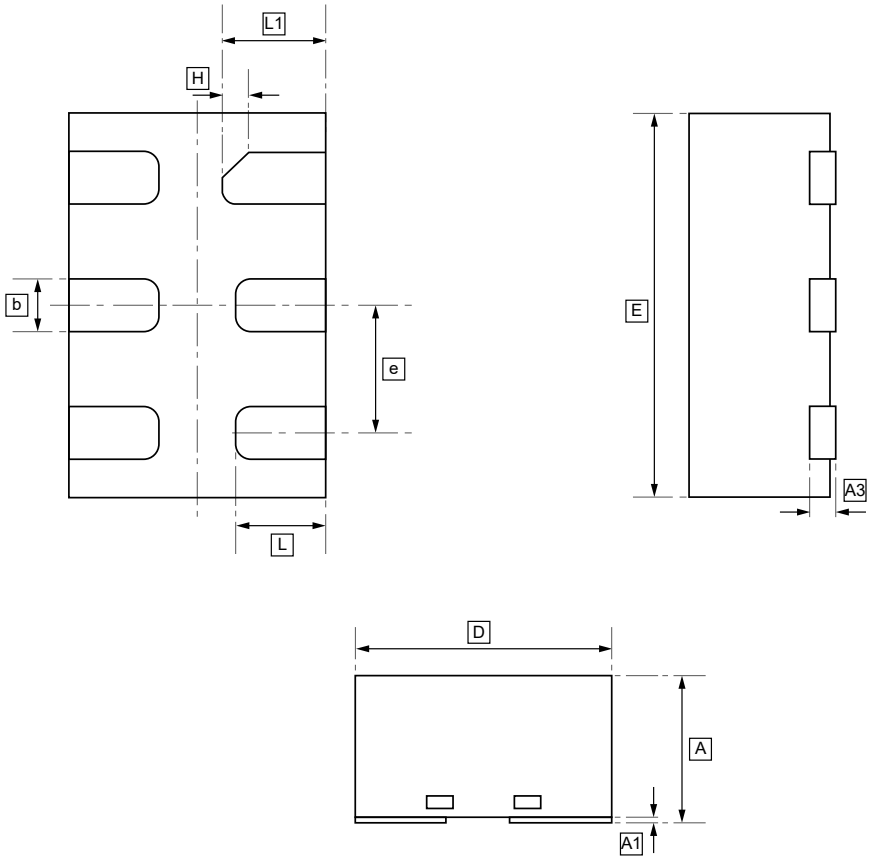
14.2 SOT23-6 Package Outline Dimensions



DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A2	b	c	D	E1	E	e	e1	L	θ
Min	1.050	0.000	1.050	0.300	0.100	2.820	1.500	2.650	0.950	1.800	0.300	0°
Max	1.250	0.100	1.150	0.500	0.200	3.020	1.700	2.950	BSC	2.000	0.600	8°

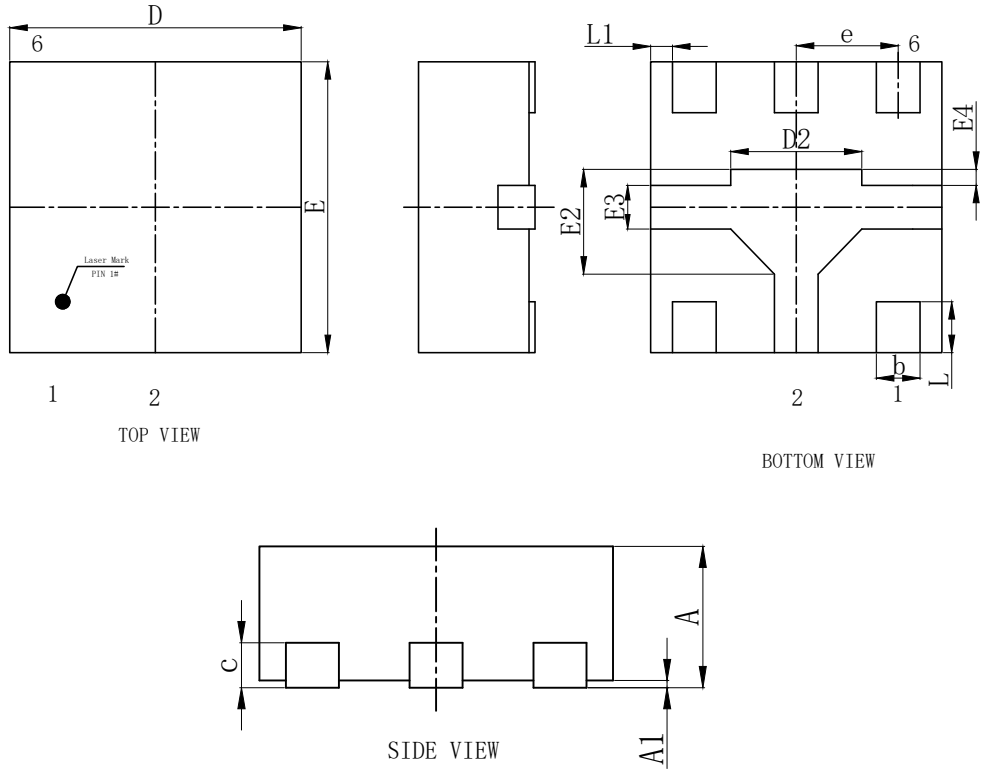
14.3 DFN6(1x1.5) Package Outline Dimensions



DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A3	b	D	E	e	H	L	L1
Min	0.50	0	0.10	0.15	0.90	1.40	0.40	0.10	0.30	0.35
Max	0.60	0.05	REF	0.25	1.10	1.60	0.60	REF	0.40	0.45

14.4 DFN6(1.0×1.0) Package Outline Dimensions

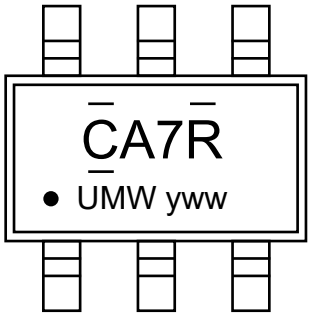


DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	b	c	D	D2	e	E	E2	E3	E4	L
Min	0.36	0.00	0.10	0.127	0.95	0.40	0.35	0.95	0.31	0.10	0.005	0.125
Max	0.40	0.05	0.20	REF	1.05	0.50	BSC	1.05	0.41	0.20	0.105	0.225

Symbol	L1
Min	0.075
Max	REF

15.Ordering Information



yww: Batch Code

Order Code	Marking	Package	Base QTY	Delivery Mode
UMW SN74LVC1G57DBVR	CA7R	SOT23-6	3000	Tape and reel
UMW SN74LVC1G57DCKR	CLR	SC70-6	3000	Tape and reel
UMW SN74LVC1G57DRYR	CL	DFN6(1*1.5)	5000	Tape and reel
UMW SN74LVC1G57DSFR	CL	DFN6(1*1)	5000	Tape and reel

16.Disclaimer

UMW reserves the right to make changes to all products, specifications. Customers should obtain the latest version of product documentation and verify the completeness and currency of the information before placing an order.

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