

## General Description

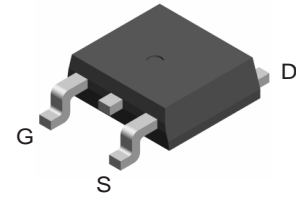
FIR2N60ALG is an N-channel enhancement mode power MOS field effect transistor which is produced using Silan proprietary F-Cell™ structure VDMOS technology. The improved planar stripe cell and the improved guard ring terminal have been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

These devices are widely used in AC-DC power suppliers, DC-DC converters and H-bridge PWM motor drivers.

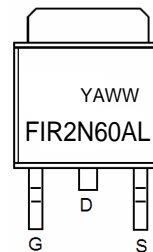
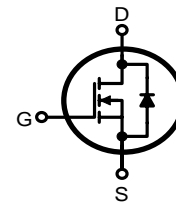
## Features

- 2A,600V,  $R_{DS(on)}$  (typ) = 3.7Ω @  $V_{GS}=10V$
- Low gate charge
- Low Crss
- Fast switching
- Improved dv/dt capability

## PIN Connection TO-252(D-PAK)



Schematic dia gram



## Marking Diagram

- Y = Year
- A = Assembly Location
- WW = Work Week
- FIR2N60AL= Specific Device Code

## Absolute Maximum Ratings (Ta = 25°C unless otherwise noted )

Characteristics	Symbol	Ratings	Unit
Drain-Source Voltage	$V_{DS}$	600	V
Gate-Source Voltage	$V_{GS}$	±30	V
Drain Current	$I_D$	$T_C=25^{\circ}C$	2.0
		$T_C=100^{\circ}C$	1.3
Drain Current Pulsed	$I_{DM}$	8	A
Power Dissipation( $T_C=25^{\circ}C$ ) -Derate above 25°C	$P_D$	35	W
		0.28	W/°C
Single Pulsed Avalanche Energy(Note 1)	$E_{AS}$	115	mJ
Operation Junction Temperature Range	$T_J$	-55~+150	°C
Storage Temperature Range	$T_{stg}$	-55~+150	°C

## Thermal Characteristics

Characteristics	Symbol	Ratings	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	3.57	$^{\circ}C/W$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	110	$^{\circ}C/W$

## Electrical Characteristics (Ta = 25°C unless otherwise noted)

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Drain -Source Breakdown Voltage	$B_{VDSS}$	25 °C, $V_{GS}=0V$ , $I_D=250\mu A$	600	--	--	V
		125 °C, $V_{GS}=0V$ , $I_D=250\mu A$	600	--	--	V
Drain-Source Leakage Current	$I_{DSS}$	25 °C, $V_{DS}=600V$ , $V_{GS}=0V$	--	--	10	$\mu A$
		125 °C, $V_{DS}=600V$ , $V_{GS}=0V$	--	--	50	$\mu A$
		150 °C, $V_{DS}=600V$ , $V_{GS}=0V$	--	--	100	$\mu A$
Gate-Source Leakage Current	$I_{GSS}$	$V_{GS}=\pm 30V$ , $V_{DS}=0V$	--	--	$\pm 100$	nA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS}=V_{DS}$ , $I_D=250\mu A$	2.0	--	4.0	V
Static Drain- Source On State Resistance	$R_{DS(on)}$	$V_{GS}=10V$ , $I_D=1.0A$	--	3.7	4.2	$\Omega$
Forward Transconductance	$G_{fs}$	$V_{DS}=10V$ , $I_D=1.0A$	--	1.3	--	S
Input Capacitance	$C_{iss}$	$V_{DS}=25V$ , $V_{GS}=0V$ , $f=1.0MHz$	--	301.7	--	pF
Output Capacitance	$C_{oss}$		--	13	--	
Reverse Transfer Capacitance	$C_{rss}$		--	1.1	--	
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=300V$ , $I_D=2.0A$ , $R_G=25\Omega$  (Note 2,3)	--	9.2	--	ns
Turn-on Rise Time	$t_r$		--	23.4	--	
Turn-off Delay Time	$t_{d(off)}$		--	15.3	--	
Turn-off Fall Time	$t_f$		--	20.1	--	
Total Gate Charge	$Q_g$	$V_{DS}=480V$ , $I_D=2.0A$ , $V_{GS}=10V$  (Note 2,3)	--	7.2	--	nC
Gate-Source Charge	$Q_{gs}$		--	1.57	--	
Gate-Drain Charge	$Q_{gd}$		--	2.1	--	

## Source-Drain Diode Ratings And Characteristics

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Continuous Source Current	$I_S$	Integral Reverse P-N Junction Diode in the MOSFET	--	--	2.0	A
Pulsed Source Current	$I_{SM}$		--	--	8.0	
Diode Forward Voltage	$V_{SD}$	$I_S=2.0A$ , $V_{GS}=0V$	--	--	1.4	V
Reverse Recovery Time	$T_{rr}$	$I_S=2.0A$ , $V_{GS}=0V$ , $di_F/dt=100A/\mu S$	--	356.75	--	ns
Reverse Recovery Charge	$Q_{rr}$		--	1.03	--	$\mu C$

### Notes:

- $L=30mH$ ,  $I_{AS}=2.52A$ ,  $V_{DD}=145V$ ,  $R_G=25\Omega$ , starting  $T_J=25^{\circ}C$ ;
- Pulse Test: Pulse width  $\leq 300\mu s$ , Duty cycle  $\leq 2\%$ ;
- Essentially independent of operating temperature.

## Typical Characteristics

Figure 1. On-Region Characteristics

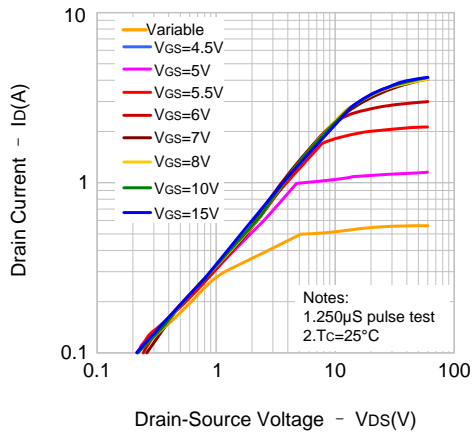


Figure 2. Transfer Characteristics

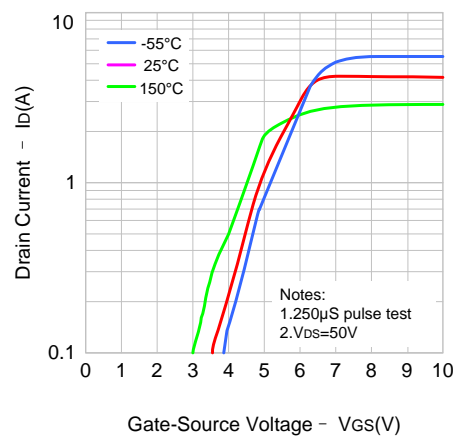


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

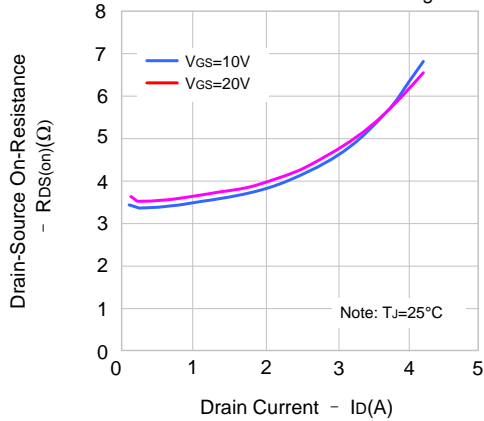


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

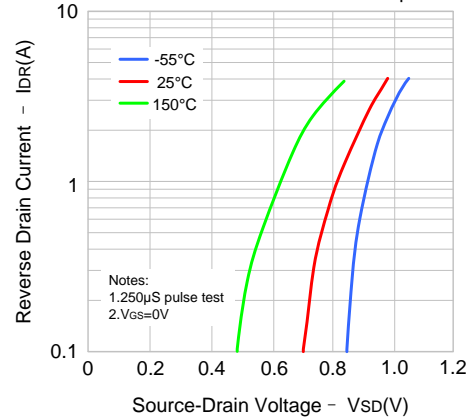


Figure 5. Capacitance Characteristics

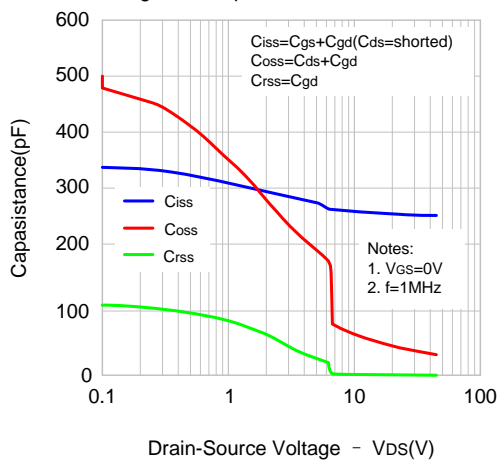
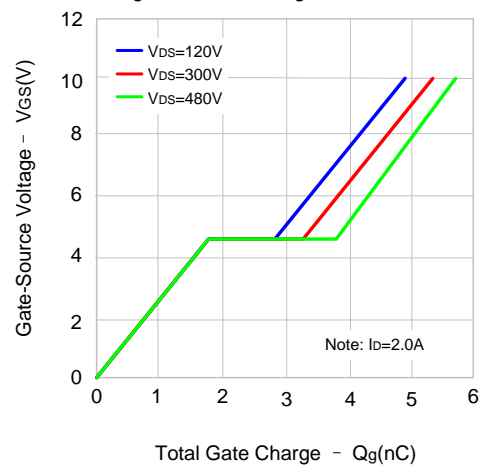
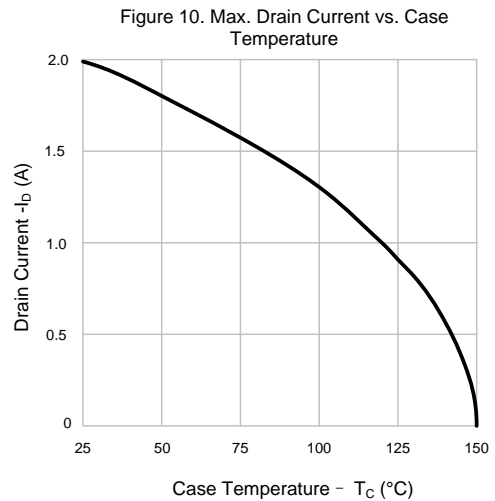
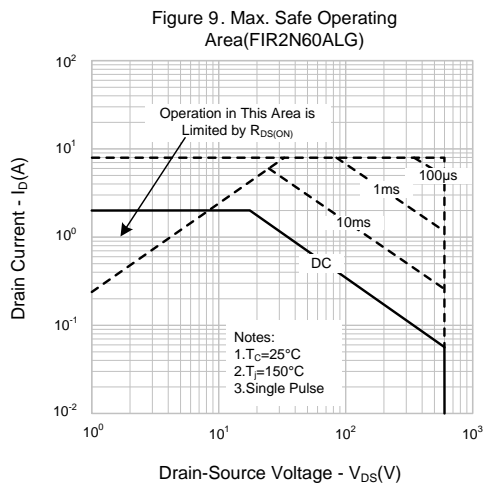
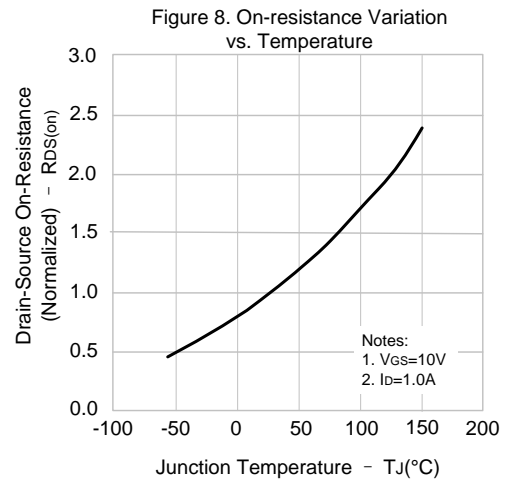
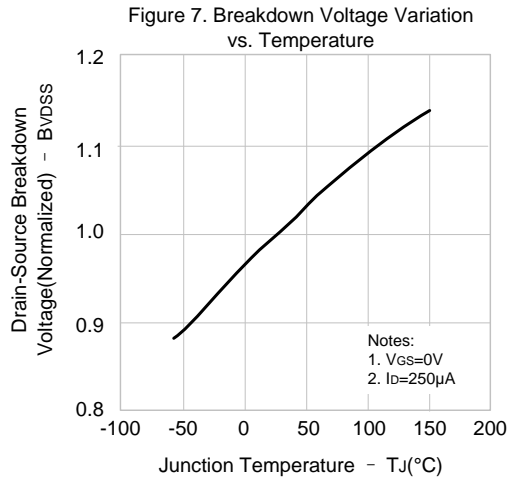


Figure 6. Gate Charge Characteristics

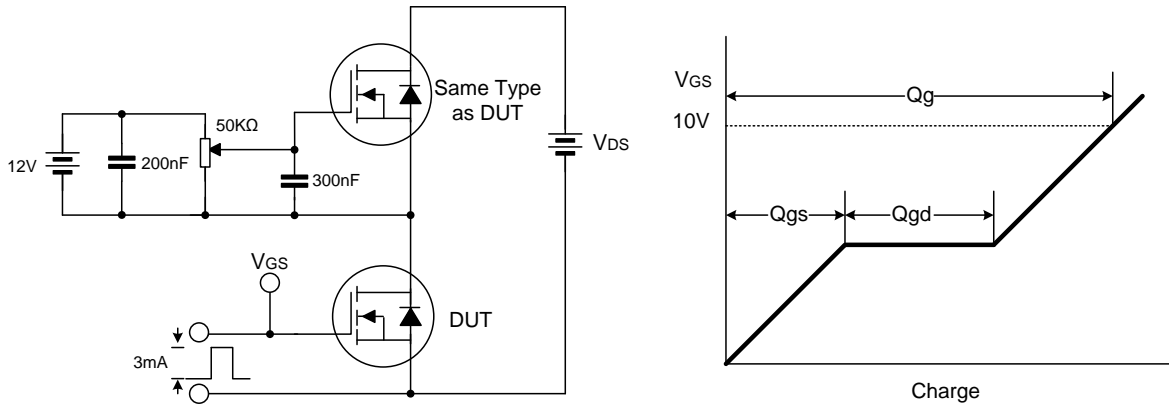


## Typical Characteristics(Continued)

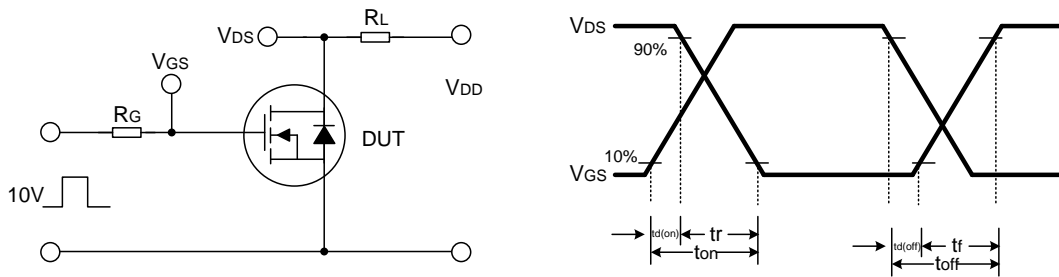


## Typical Test Circuit

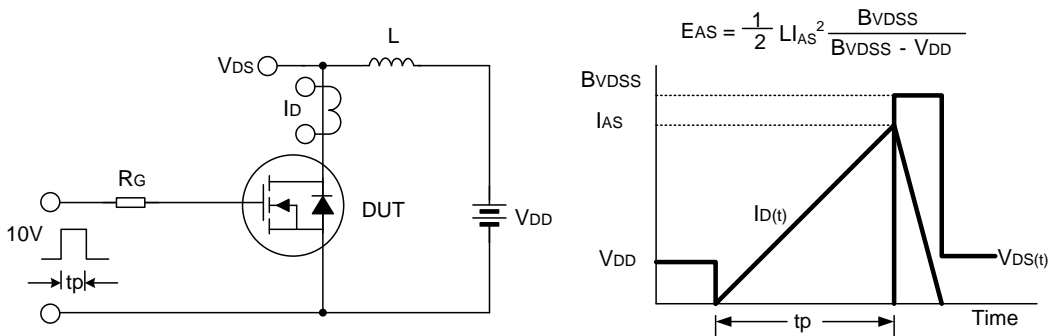
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveform

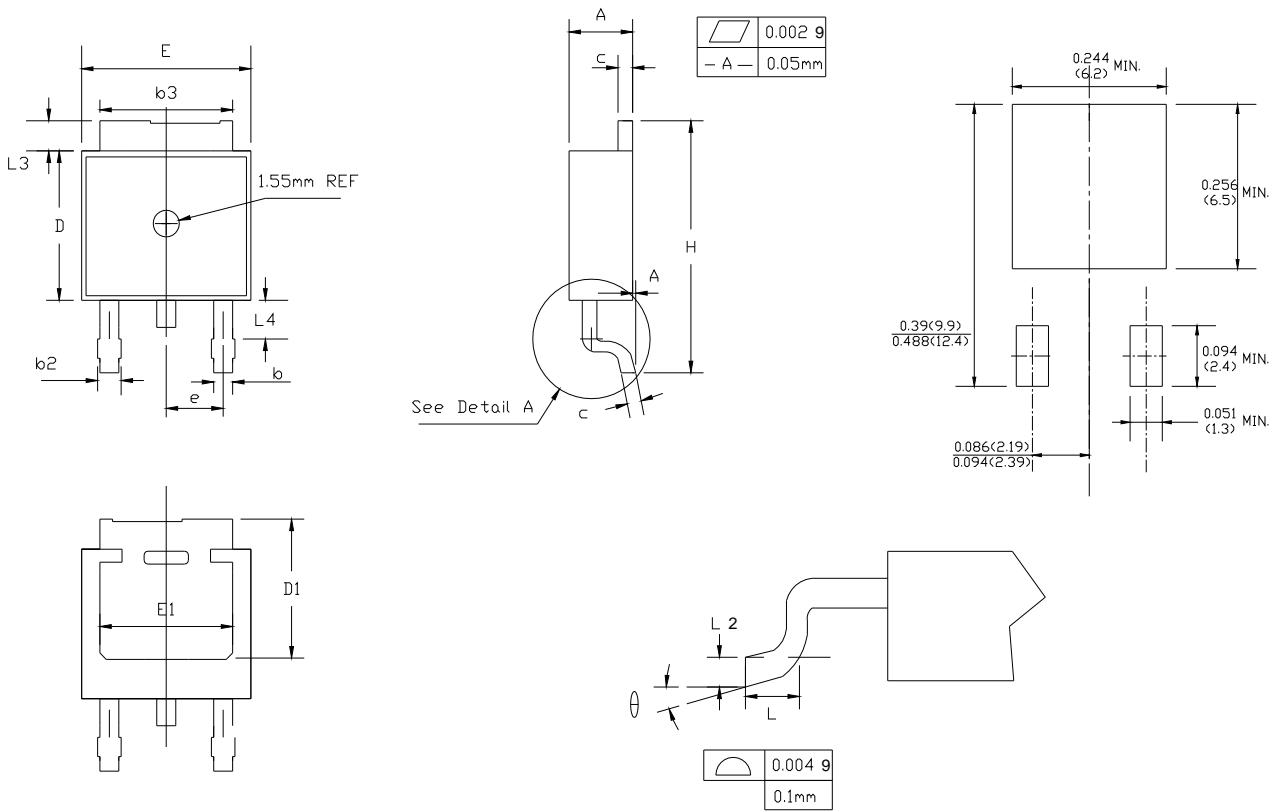


Unclamped Inductive Switching Test Circuit & Waveform



## Package Dimensions

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Revision History	
Date	Revision Changes
2017/7/3	<ol style="list-style-type: none"><li>1. Adding Minimum Ciss Value:297pF</li><li>2. Adding Maximum Ciss Value:306.1pF</li><li>3. Adding Minimum Coss Value:11pF</li><li>4. Adding Maximum Coss Value:17pF</li><li>5. Adding Minimum Crss Value:0.9pF</li><li>6. Adding Maximum Crss Value:1.3pF</li><li>7. Change Typical Ciss value from 250.1pF to 301.7pF</li><li>8. Change Typical Coss value from 35.7pF to 13pF</li><li>9. Change Typical Qg value from 5.67nC to 7.2nC</li><li>10. Change Typical Qgs value from 1.74nC to 1.57nC</li><li>11. Change Typical Qgs value from 1.99nC to 2.1nC</li></ol>