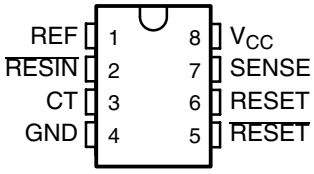
SLVS028I – APRIL 1983 – REVISED JULY 2009

- **Power-On Reset Generator**
- **Automatic Reset Generation After Voltage Drop**
- **Wide Supply-Voltage Range**
- **Precision Voltage Sensor**
- **Temperature-Compensated Voltage Reference**
- **True and Complement Reset Outputs**
- **Externally Adjustable Pulse Duration**

TL7702A, TL7709A, TL7712A, TL7715A . . . D OR P PACKAGE
TL7705A . . . D, P, OR PS PACKAGE,
(TOP VIEW)



description/ordering information

ORDERING INFORMATION†

T_A	PACKAGE‡		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP (P)	Tube of 50	TL7702ACP	TL7702ACP
	SOIC (D)	Tube of 75	TL7702ACD	7702AC
		Reel of 2500	TL7702ACDR	
	PDIP (P)	Tube of 50	TL7705ACP	TL7705ACP
	SOIC (D)	Tube of 75	TL7705ACD	7705AC
		Reel of 2500	TL7705ACDR	
	SOP (PS)	Reel of 2000	TL7705ACPSR	T7705A
	PDIP (P)	Tube of 50	TL7709ACP	TL7709ACP
	SOIC (D)	Tube of 75	TL7709ACD	7709AC
		Reel of 2500	TL7709ACDR	
	PDIP (P)	Tube of 50	TL7712ACP	TL7709ACP
	SOIC (D)	Tube of 75	TL7712ACD	7712AC
		Reel of 2500	TL7712ACDR	
	PDIP (P)	Tube of 50	TL7715ACP	TL7715ACP
	SOIC (D)	Tube of 75	TL7715ACD	7715AC
–40°C to 85°C	PDIP (P)	Tube of 50	TL7702AIP	TL7702AIP
	SOIC (D)	Tube of 75	TL7702AID	7702AI
		Reel of 2500	TL7702AIDR	
	PDIP (P)	Tube of 50	TL7705AIP	TL7705AIP
	SOIC (D)	Tube of 75	TL7705AID	7705AI
		Reel of 2500	TL7705AIDR	
	SOIC (D)	Reel of 2500	TL7712AIDR	7712AI

† For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

‡ Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

description/ordering information (continued)

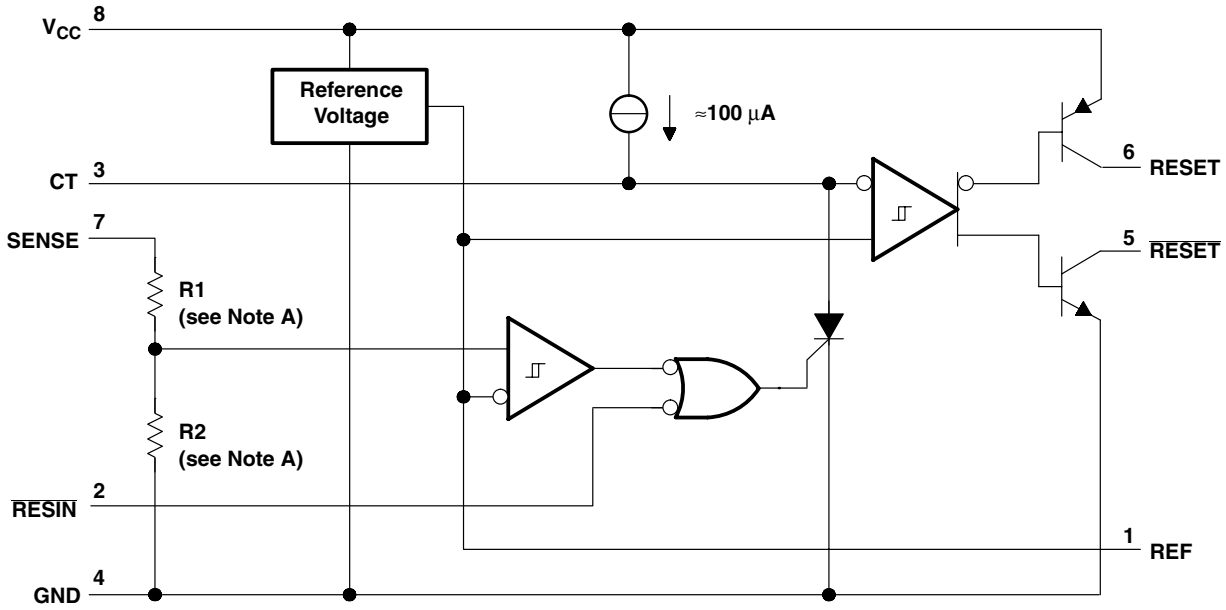
The TL77xxA family of integrated-circuit supply-voltage supervisors is designed specifically for use as reset controllers in microcomputer and microprocessor systems. The supply-voltage supervisor monitors the supply for undervoltage conditions at the SENSE input. During power up, the $\overline{\text{RESET}}$ output becomes active (low) when V_{CC} attains a value approaching 3.6 V. At this point (assuming that SENSE is above V_{IT+}), the delay timer function activates a time delay, after which outputs $\overline{\text{RESET}}$ and RESET go inactive (high and low, respectively). When an undervoltage condition occurs during normal operation, $\overline{\text{RESET}}$ and RESET go active. To ensure that a complete reset occurs, the reset outputs remain active for a time delay after the voltage at the SENSE input exceeds the positive-going threshold value. The time delay is determined by the value of the external capacitor C_T: $t_d = 1.3 \times 10^4 \times C_T$, where C_T is in farads (F) and t_d is in seconds (s).

During power down and when SENSE is below V_{IT-}, the outputs remain active until V_{CC} falls below 2 V. After this, the outputs are undefined.

An external capacitor (typically 0.1 μF) must be connected to REF to reduce the influence of fast transients in the supply voltage.

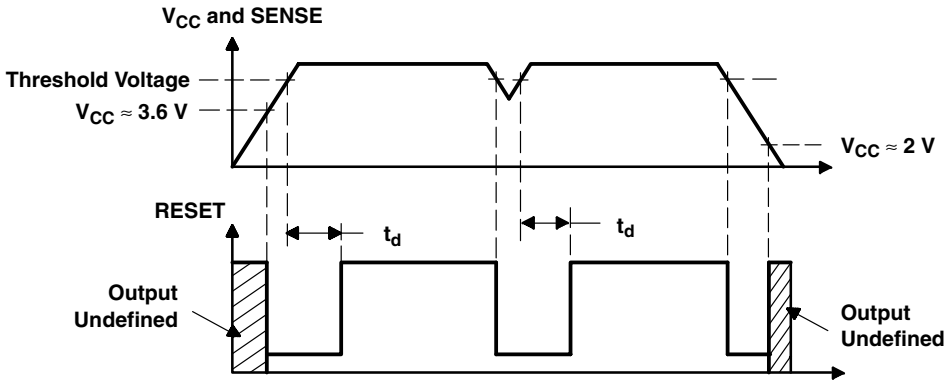
functional block diagram

The functional block diagram is shown for illustrative purposes only; the actual circuit includes a trimming network to adjust the reference voltage and sense-comparator trip point.



NOTES: A. TL7702A: R1 = 0 Ω, R2 = open
TL7705A: R1 = 7.8 kΩ, R2 = 10 kΩ
TL7709A: R1 = 19.7 kΩ, R2 = 10 kΩ
TL7712A: R1 = 32.7 kΩ, R2 = 10 kΩ
TL7715A: R1 = 43.4 kΩ, R2 = 10 kΩ
B. Resistor values shown are nominal.

timing diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) . . . . . 20 V
Input voltage range, V_I, $\overline{\text{RESIN}}$ . . . . . –0.3 V to 20 V
Input voltage range, V_I, SENSE: TL7702A (see Note 2) . . . . . –0.3 V to 6 V
TL7705A . . . . . –0.3 V to 20 V
TL7709A . . . . . –0.3 V to 20 V
TL7712A, TL7715A . . . . . –0.3 V to 20 V
High-level output current, I_{OH}, RESET . . . . . –30 mA
Low-level output current, I_{OL}, $\overline{\text{RESET}}$ . . . . . 30 mA
Package thermal impedance, θ_{JA} (see Notes 3 and 4): D package . . . . . 97°C/W
P package . . . . . 85°C/W
PS package . . . . . 95°C/W
Operating virtual junction temperature, T_J . . . . . 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to GND.
2. For proper operation of the TL7702A, the voltage applied to the SENSE terminal should not exceed V_{CC} – 1 V or 6 V, whichever is less.
3. Maximum power dissipation is a function of $T_J(max)$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) – T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
4. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		3.5	18	V
V_{IH}	High-level input voltage at $\overline{\text{RESIN}}$		2		V
V_{IL}	Low-level input voltage at $\overline{\text{RESIN}}$			0.6	V
V_I	Input voltage, SENSE	TL7702A	0	See Note 2	V
		TL7705A	0	10	
		TL7709A	0	15	
		TL7712A	0	20	
		TL7715A	0	20	
I_{OH}	High-level output current, RESET			–16	mA
I_{OL}	Low-level output current, $\overline{\text{RESET}}$			16	mA
T_A	Operating free-air temperature range	TL77xxAC	0	70	°C
		TL77xxAI	–40	85	

NOTE 2: For proper operation of the TL7702A, the voltage applied to the SENSE terminal should not exceed V_{CC} – 1 V or 6 V, whichever is less.

electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS†	TL77xxAC TL77xxAI			UNIT
				MIN	TYP	MAX	
V_{OH}	High-level output voltage, RESET		I_{OH} = –16 mA	V_{CC}–1.5			V
V_{OL}	Low-level output voltage, $\overline{\text{RESET}}$		I_{OL} = 16 mA			0.4	V
V_{ref}	Reference voltage		T_A = 25°C	2.48	2.53	2.58	V
$V_{IT–}$	Negative-going input threshold voltage, SENSE	TL7702A	T_A = 25°C	2.48	2.53	2.58	V
		TL7705A		4.5	4.55	4.6	
		TL7709A		7.5	7.6	7.7	
		TL7712A		10.6	10.8	11	
		TL7715A		13.2	13.5	13.8	
V_{hys}	Hysteresis, SENSE ($V_{IT+} – V_{IT–}$)	TL7702A	T_A = 25°C		10		mV
		TL7705A			15		
		TL7709A			20		
		TL7712A			35		
		TL7715A			45		
I_I	Input current	$\overline{\text{RESIN}}$	V_I = 2.4 V to V_{CC}			20	µA
			V_I = 0.4 V			–100	
		SENSE TL7702A	$V_{ref} < V_I < V_{CC} – 1.5$ V		0.5	2	
I_{OH}	High-level output current, $\overline{\text{RESET}}$		V_O = 18 V			50	µA
I_{OL}	Low-level output current, RESET		V_O = 0			–50	µA
I_{CC}	Supply current		All inputs and outputs open		1.8	3	mA

† All electrical characteristics are measured with 0.1-µF capacitors connected at REF, CT, and V_{CC} to GND.

switching characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		TL77xxAC TL77xxAI			UNIT
					MIN	TYP	MAX	
	Output pulse duration		C_T = 0.1 µF		0.65	1.2	2.6	msec
	Input pulse duration at $\overline{\text{RESIN}}$				0.4			µs
$t_{w(S)}$	Pulse duration at SENSE input to switch outputs		$V_{IH} = V_{IT-} + 200$ mV,	$V_{IL} = V_{IT-} - 200$ mV	2			µs
t_{pd}	Propagation delay time, $\overline{\text{RESIN}}$ to $\overline{\text{RESET}}$		V_{CC} = 5 V				1	µs
t_r	Rise time	RESET	V_{CC} = 5 V,	See Note 5			0.2	µs
		$\overline{\text{RESET}}$					3.5	
t_f	Fall time	RESET	V_{CC} = 5 V,	See Note 5			3.5	µs
		$\overline{\text{RESET}}$					0.2	

† All switching characteristics are measured with 0.1-µF capacitors connected at REF and V_{CC} to GND.
NOTE 5: The rise and fall times are measured with a 4.7-kΩ load resistor at RESET and $\overline{\text{RESET}}$.

PARAMETER MEASUREMENT INFORMATION

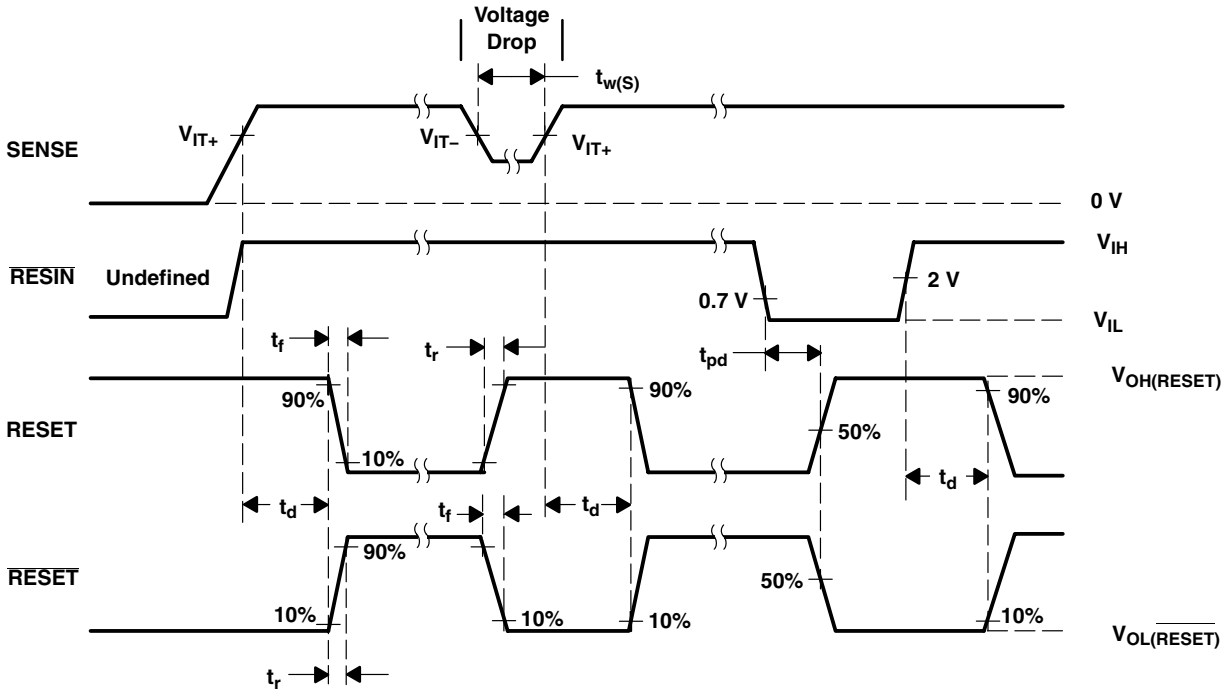


Figure 1. Voltage Waveforms

TYPICAL CHARACTERISTICS†

ASSERTION TIME vs LOAD RESISTANCE

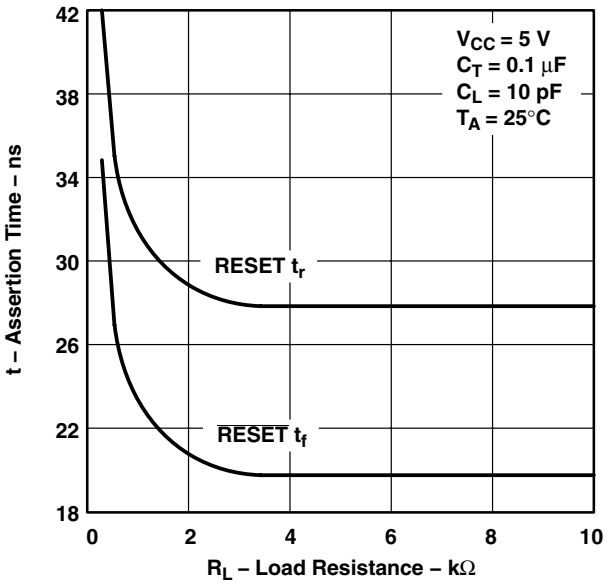


Figure 2

DEASSERTION TIME vs LOAD RESISTANCE

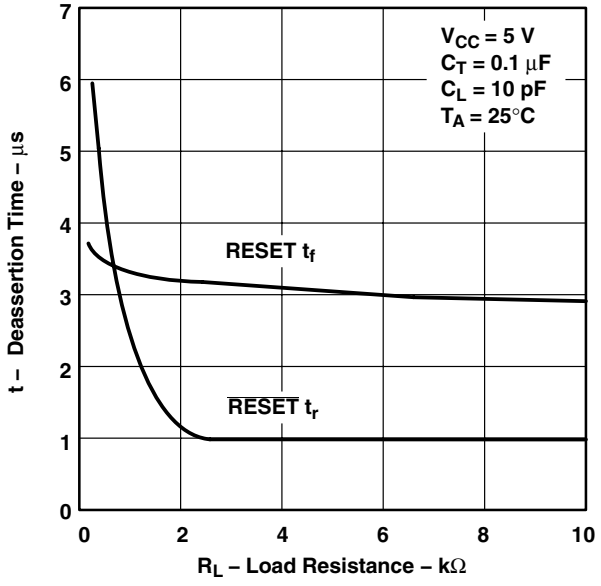


Figure 3

ASSERTION TIME vs LOAD CAPACITANCE

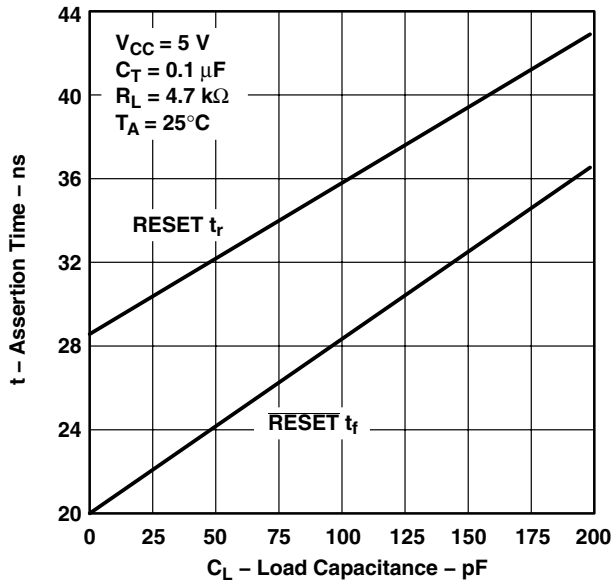


Figure 4

DEASSERTION TIME vs LOAD CAPACITANCE

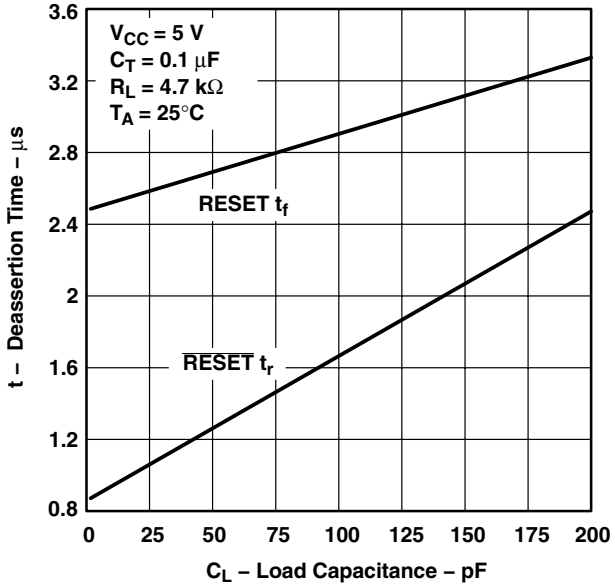


Figure 5

† For proper operation, both RESET and $\overline{\text{RESET}}$ should be terminated with resistors of similar value. Failure to do so may cause unwanted plateauing in either output waveform during switching.

APPLICATION INFORMATION

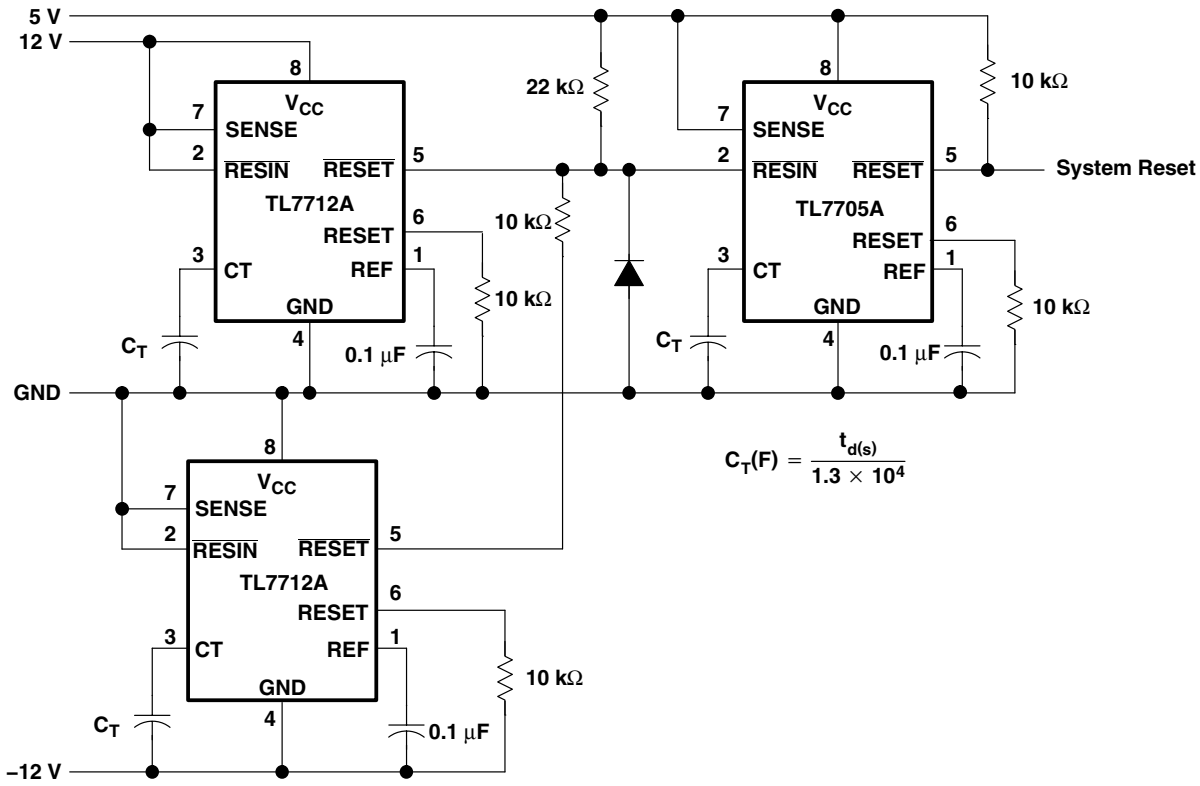


Figure 6. Multiple Power-Supply System Reset Generation

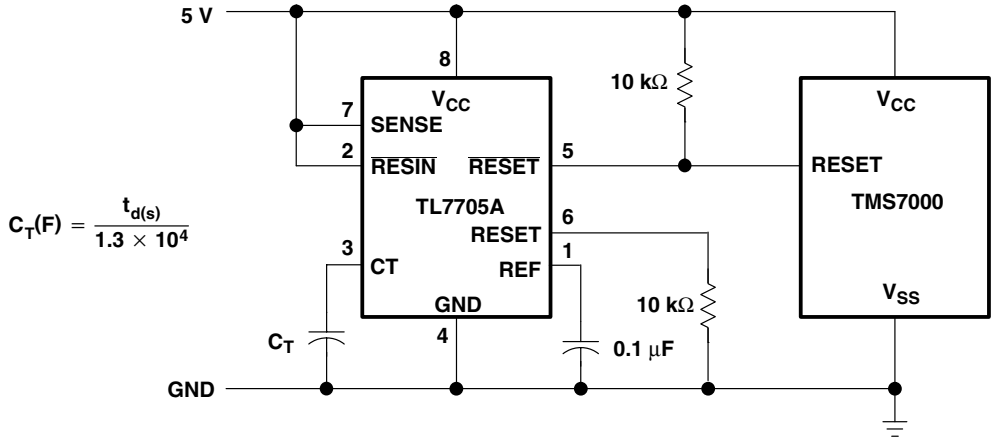


Figure 7. Reset Controller for TMS7000 System

APPLICATION INFORMATION

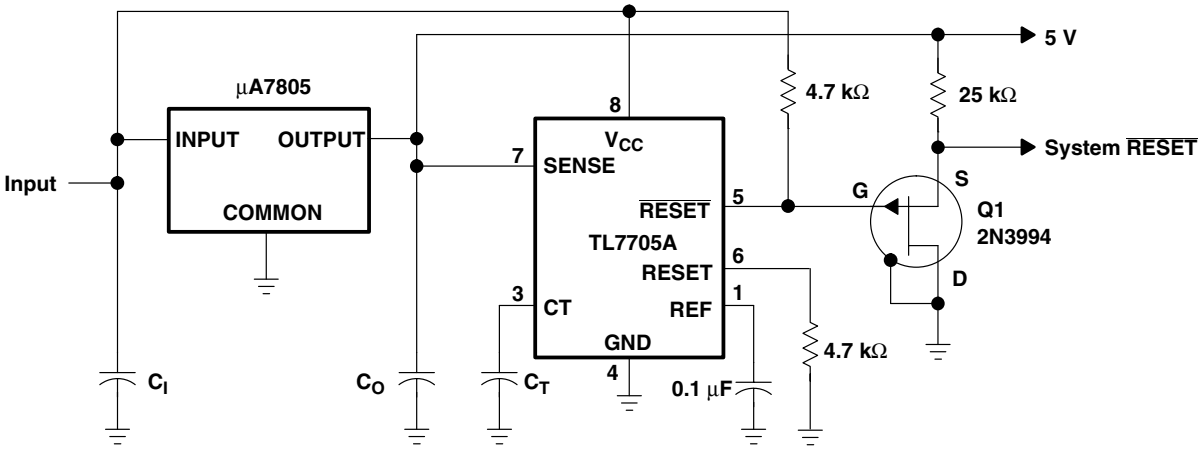


Figure 8. Eliminating Undefined States Using a P-Channel JFET

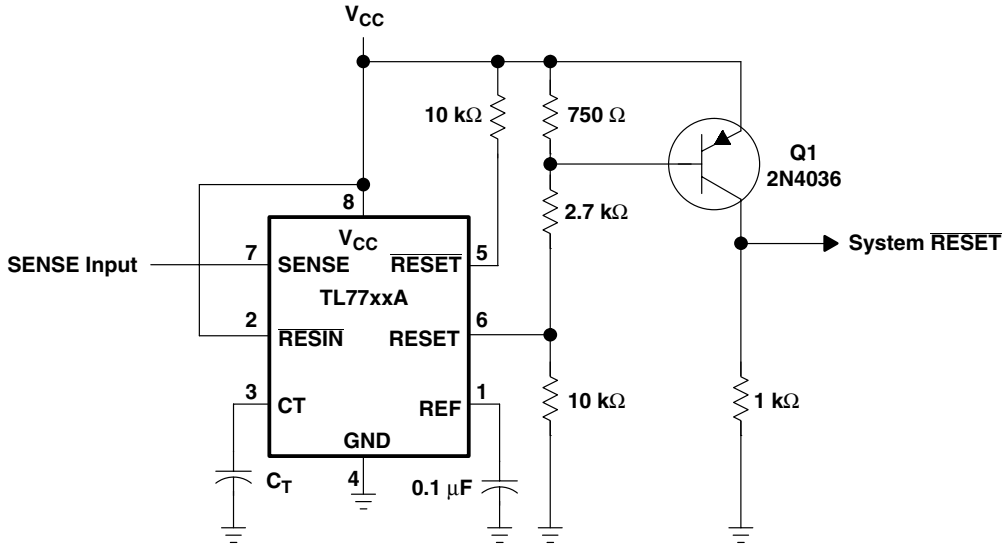


Figure 9. Eliminating Undefined States Using a pnp Transistor

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL7702ACD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	7702AC	Samples
TL7702ACDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	7702AC	Samples
TL7702ACDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	7702AC	Samples
TL7702ACDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	7702AC	Samples
TL7702ACDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	7702AC	Samples
TL7702ACP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL7702ACP	Samples
TL7702AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	7702AI	Samples
TL7702AIDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	7702AI	Samples
TL7702AIDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	7702AI	Samples
TL7702AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	7702AI	Samples
TL7702AIDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	7702AI	Samples
TL7702AIDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	7702AI	Samples
TL7702AIP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	TL7702AIP	Samples
TL7702AIPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	TL7702AIP	Samples
TL7702AMFKB	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI	-55 to 125		
TL7702AMJG	OBSOLETE	CDIP	JG	8		TBD	Call TI	Call TI	-55 to 125		
TL7702AMJGB	OBSOLETE	CDIP	JG	8		TBD	Call TI	Call TI	-55 to 125		
TL7705ACD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	7705AC	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL7705ACDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	7705AC	Samples
TL7705ACDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	7705AC	Samples
TL7705ACDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	7705AC	Samples
TL7705ACDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	7705AC	Samples
TL7705ACDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	7705AC	Samples
TL7705ACP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL7705ACP	Samples
TL7705ACPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL7705ACP	Samples
TL7705ACPSLE	OBSOLETE	SO	PS	8		TBD	Call TI	Call TI	0 to 70		
TL7705ACPSR	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T7705A	Samples
TL7705AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	7705AI	Samples
TL7705AIDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	7705AI	Samples
TL7705AIDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	7705AI	Samples
TL7705AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	7705AI	Samples
TL7705AIDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	7705AI	Samples
TL7705AIDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	7705AI	Samples
TL7705AIP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	TL7705AIP	Samples
TL7705AIPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	TL7705AIP	Samples
TL7709ACD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	7709AC	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL7709ACDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	7709AC	Samples
TL7709ACDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	7709AC	Samples
TL7709ACP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL7709ACP	Samples
TL7709ACPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL7709ACP	Samples
TL7709AID	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	-40 to 85		
TL7709AIP	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI	-40 to 85		
TL7712ACD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	7712AC	Samples
TL7712ACDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	7712AC	Samples
TL7712ACDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	7712AC	Samples
TL7712ACDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	7712AC	Samples
TL7712ACDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	7712AC	Samples
TL7712ACDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	7712AC	Samples
TL7712ACP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL7712ACP	Samples
TL7712ACPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL7712ACP	Samples
TL7712AID	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	-40 to 85		
TL7712AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		7712AI	Samples
TL7712AIP	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI	-40 to 85		
TL7715ACD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	7715AC	Samples
TL7715ACDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	7715AC	Samples
TL7715ACDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	7715AC	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL7715ACP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL7715ACP	Samples
TL7715ACPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL7715ACP	Samples
TL7715AID	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	-40 to 85		
TL7715AIP	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI	-40 to 85		

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

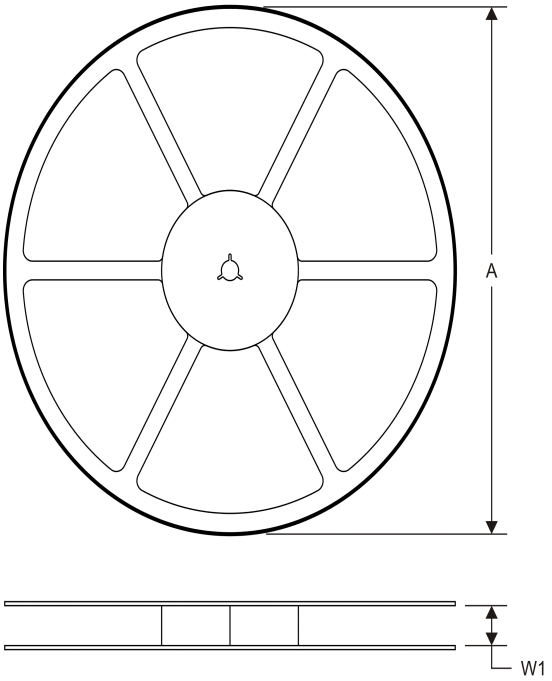
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

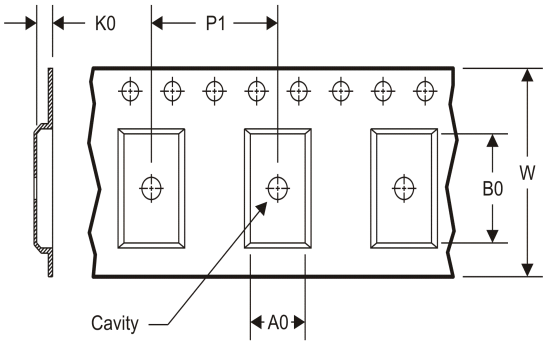
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



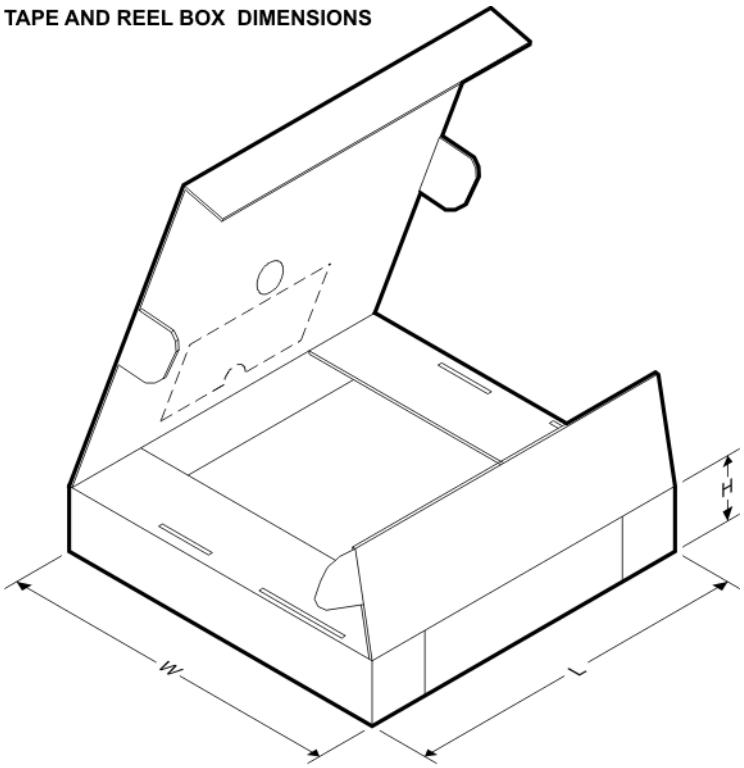
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL7702ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL7702ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL7702AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL7705ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL7705ACPSR	SO	PS	8	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
TL7705AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL7709ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL7712ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL7712AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

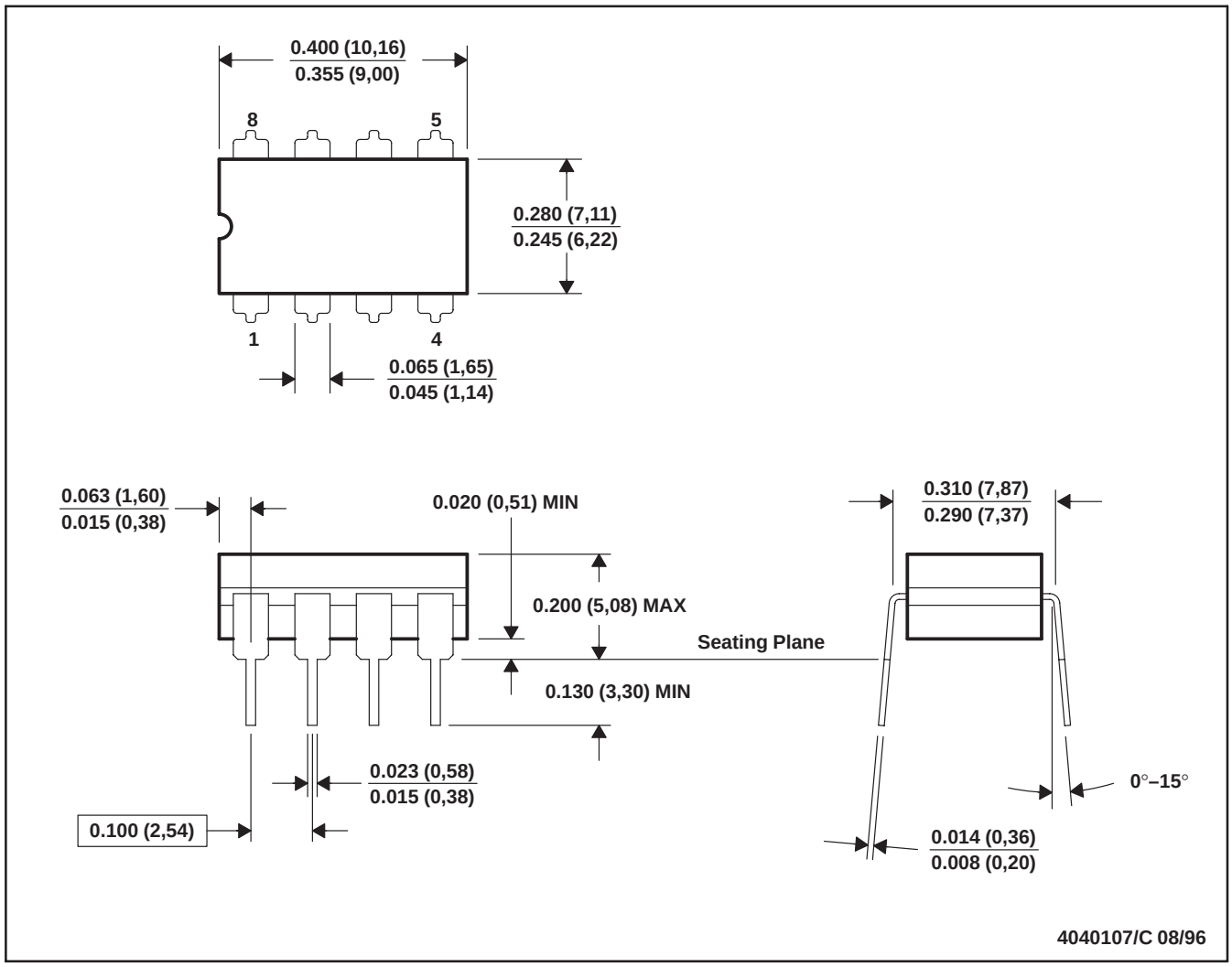


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL7702ACDR	SOIC	D	8	2500	340.5	338.1	20.6
TL7702ACDR	SOIC	D	8	2500	367.0	367.0	35.0
TL7702AIDR	SOIC	D	8	2500	340.5	338.1	20.6
TL7705ACDR	SOIC	D	8	2500	340.5	338.1	20.6
TL7705ACPSR	SO	PS	8	2000	367.0	367.0	38.0
TL7705AIDR	SOIC	D	8	2500	340.5	338.1	20.6
TL7709ACDR	SOIC	D	8	2500	340.5	338.1	20.6
TL7712ACDR	SOIC	D	8	2500	340.5	338.1	20.6
TL7712AIDR	SOIC	D	8	2500	340.5	338.1	20.6

MCER001A – JANUARY 1995 – REVISED JANUARY 1997

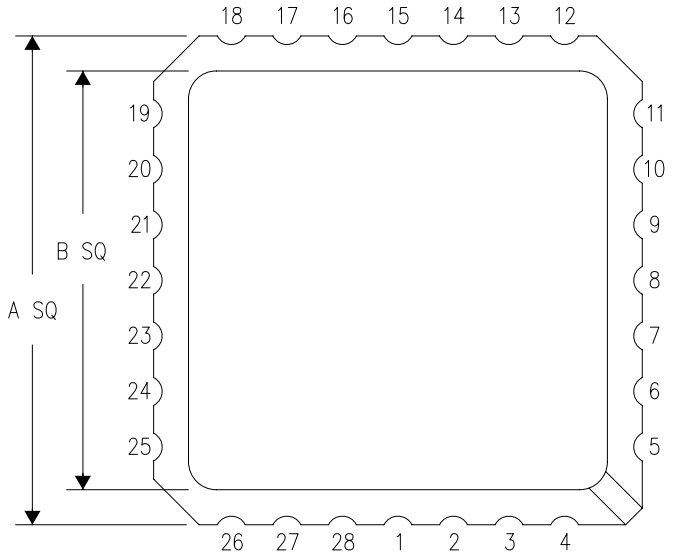
JG (R-GDIP-T8) **CERAMIC DUAL-IN-LINE**



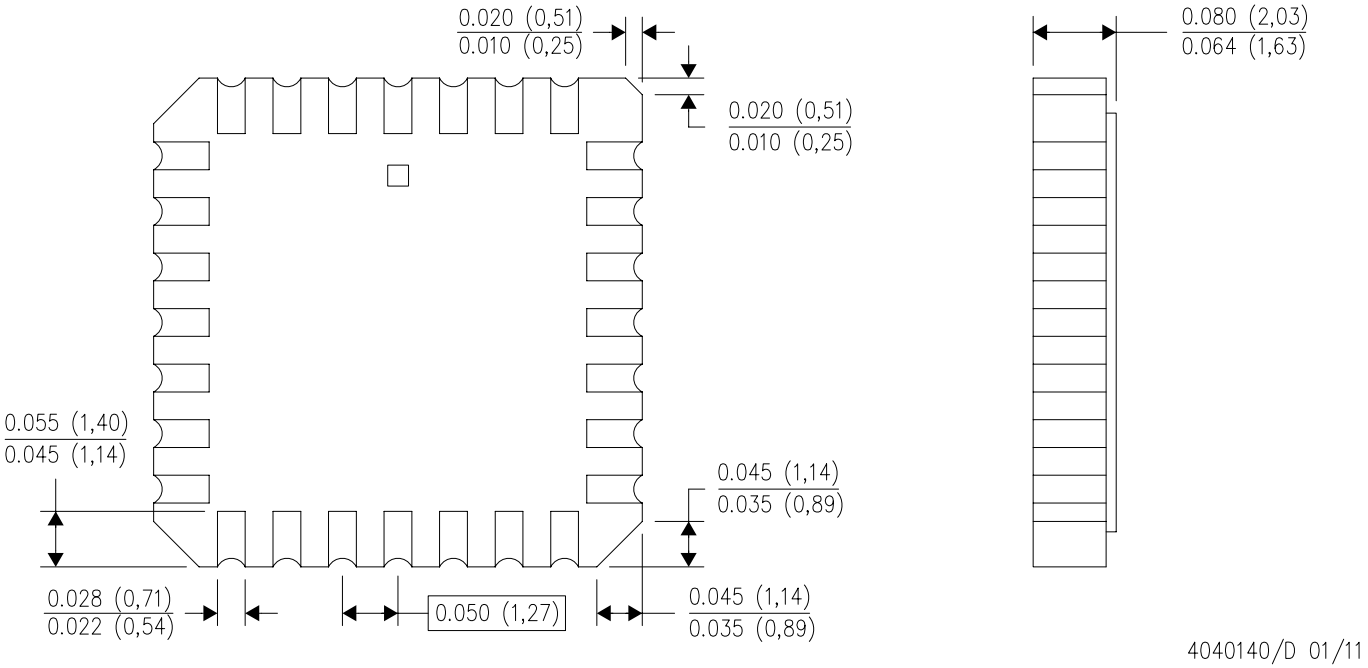
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification.
E. Falls within MIL STD 1835 GDIP1-T8

FK (S–CQCC–N**) LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



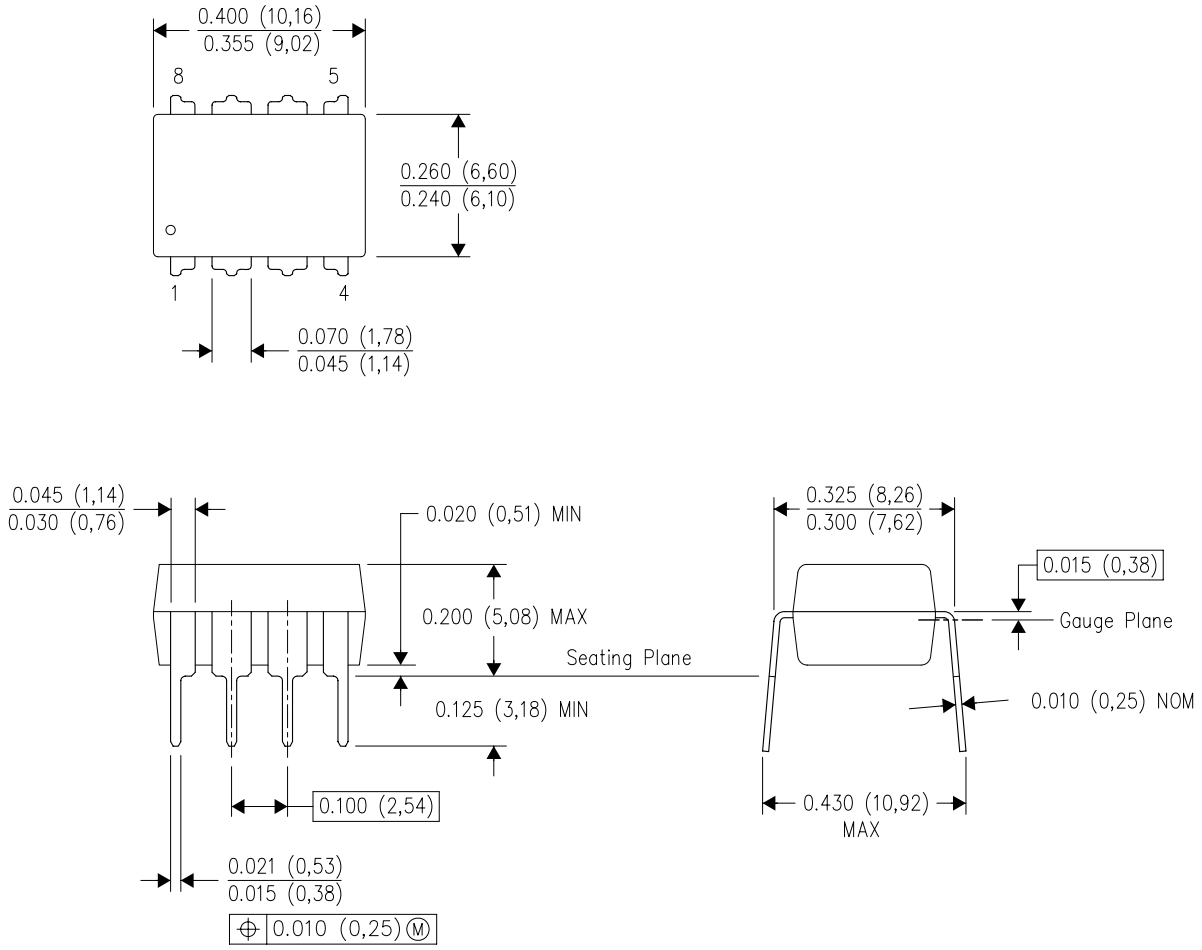
NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

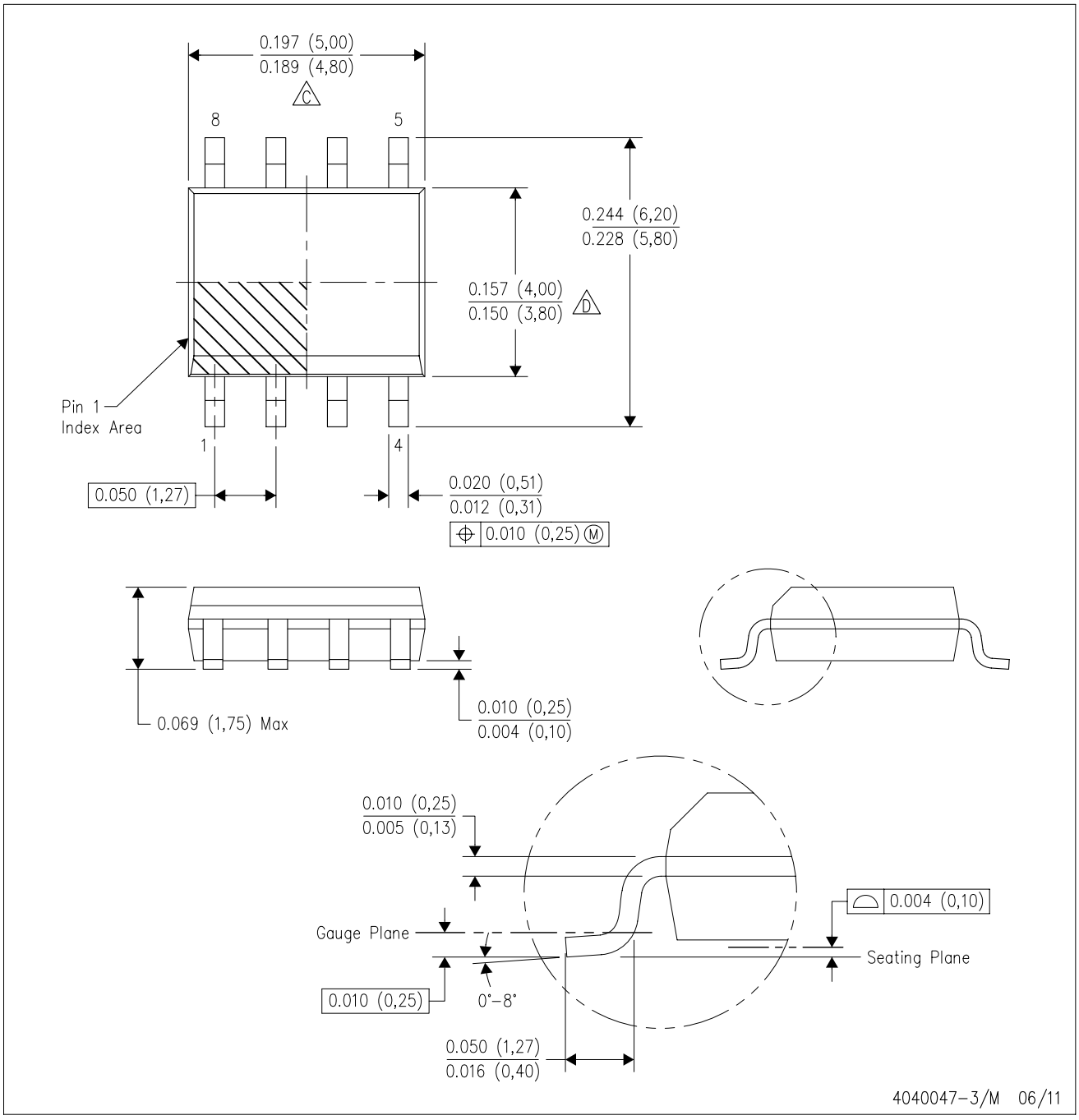
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. Falls within JEDEC MS–004

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



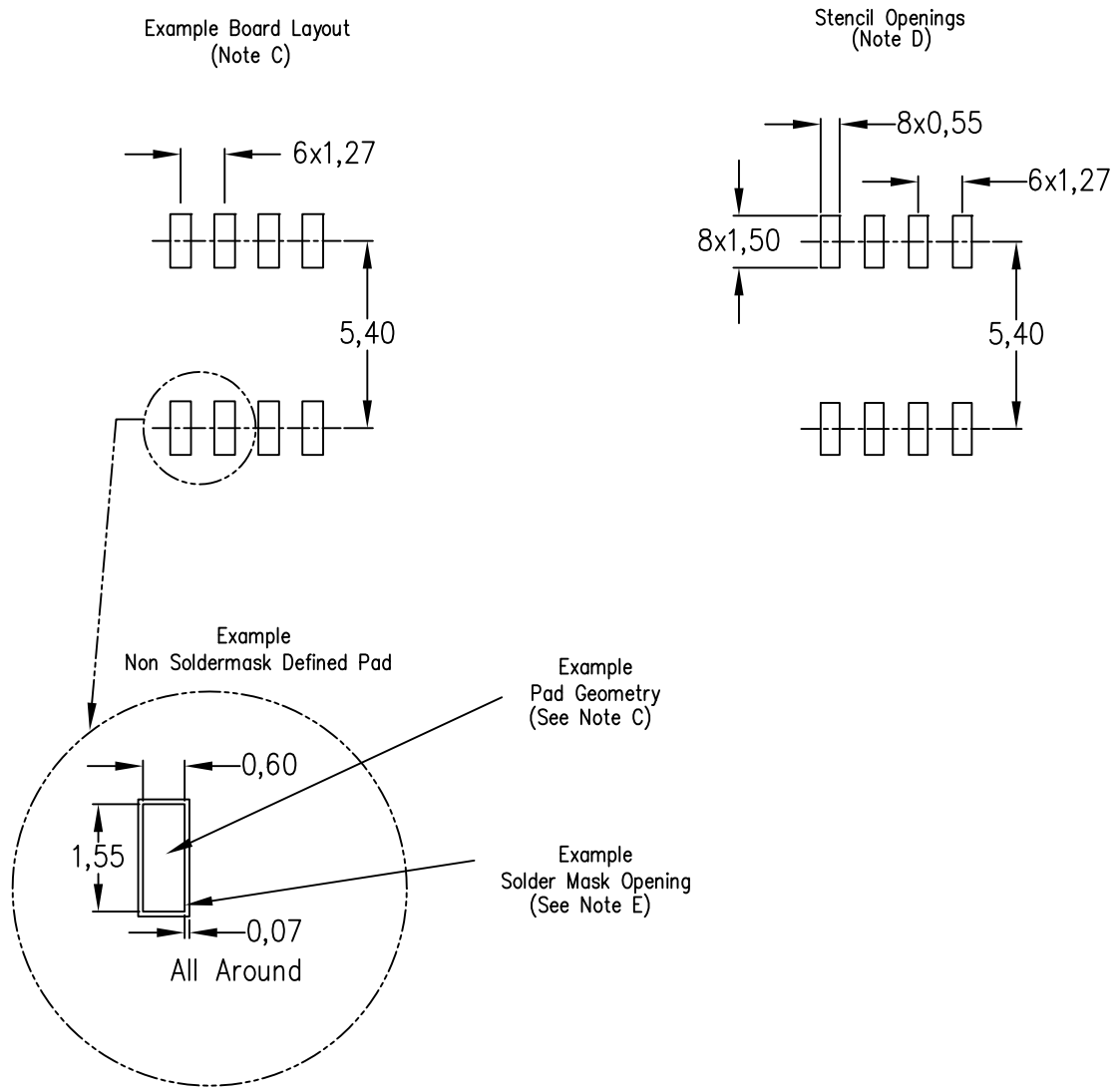
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

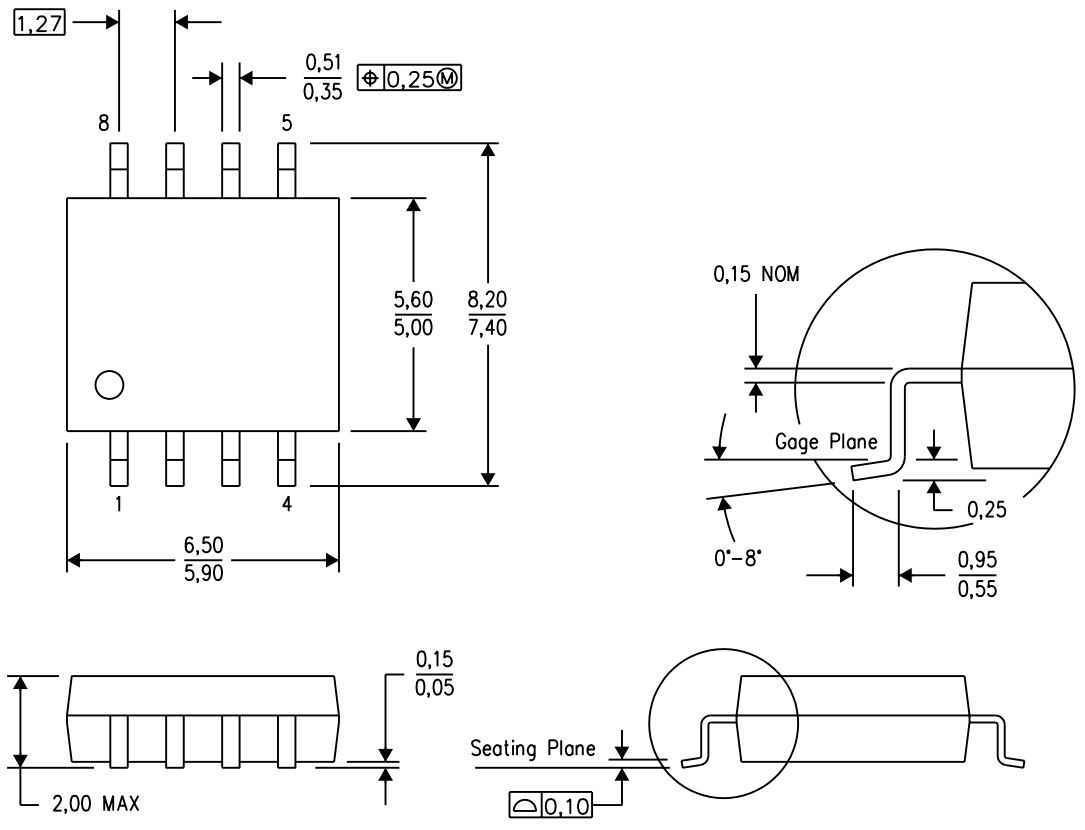
D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

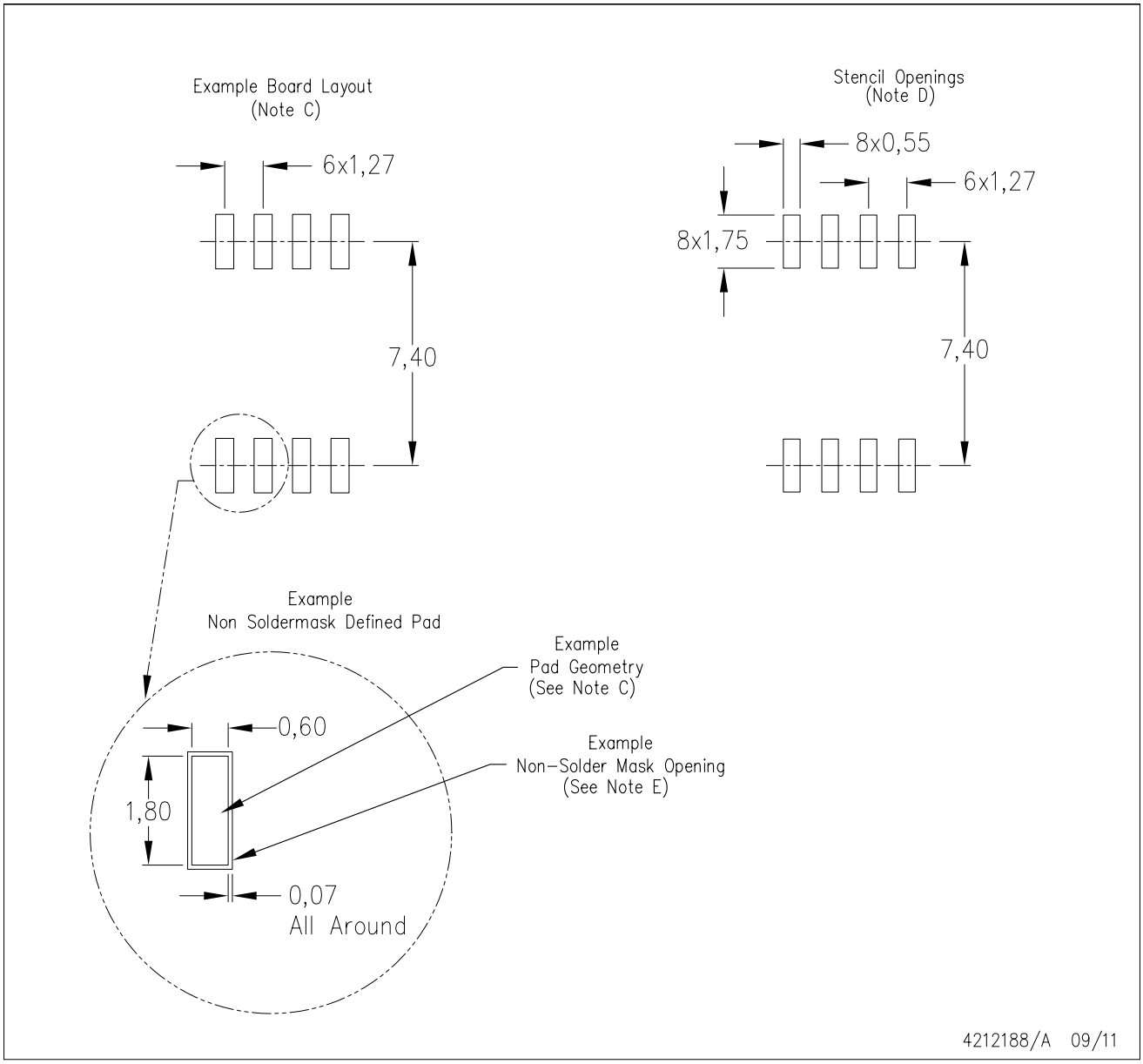
PS (R-PDSO-G8) **PLASTIC SMALL-OUTLINE PACKAGE**



4040063/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PS (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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