

BCT642

Low-Power, Three-Port , High-Speed MIPI Switch

GENERAL DESCRIPTION

The BCT642 is a bi-directional, low-power, high-speed analog switch. The pin out is designed to ease differential signal layout and is configured as a triple-pole, double-throw switch (TPDT). The BCT642 is optimized for switching between two MIPI devices, such as cameras or LCD displays and on-board Multimedia Application Processors (MAP).

The BCT642 is compatible with the requirements of Mobile Industry Processor Interface (MIPI). The low-capacitance design allows the BCT642 to switch signals that exceed 500MHz in frequency. Superior channel-to-channel crosstalk immunity minimizes interference and allows the transmission of high-speed differential signals and single-ended signals, as described by the MIPI specification. BCT642 is a direct replacement for FSA642.

FEATURES

- Low On Capacitance:7.0pF Typical
- Low On Resistance:7.0Ω Typical
- Wide -3db Bandwidth:1G Hz Typical
- 24-Lead QFN (2.5 x 3.4mm) Package

APPLICATIONS

Dual Camera Applications for Cell Phones
 Dual LCD Applications for Cell Phones, Digital Camera Displays, and Viewfinders

ORDERING INFORMATION

Order Number	Package Type	Temperature Range	Marking	QTY/Reel
BCT642EGG-TR	QFN-24(2.5 mmx 3.4 mm)	-40°C to +85°C	642	3000

TYPICAL OPERATING CIRCUIT

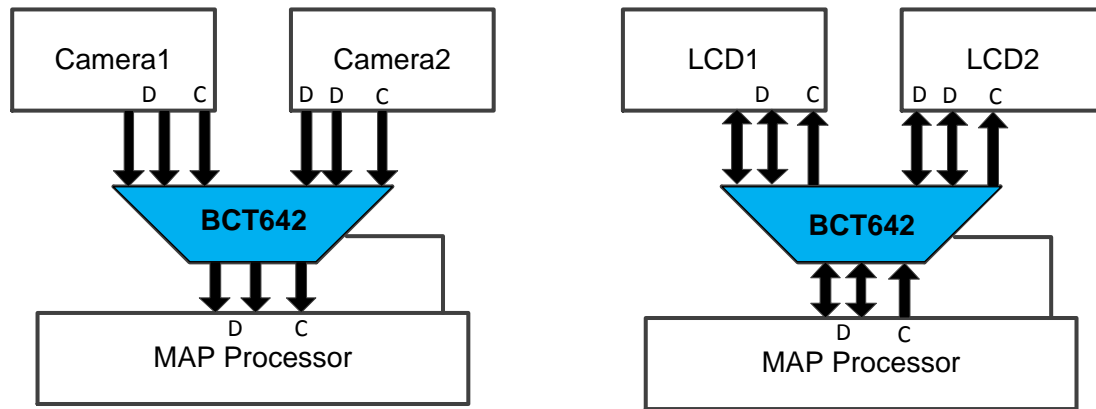


Figure 1. Application Block Diagram

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC}).....	-0.5V to +5.25V
DC Input Voltage (SEL, /OE) ⁽¹⁾	-0.5V to V_{CC} V
DC Switch I/O Voltage.....	-0.5V to $V_{CC}+0.3$ V
DC Input Diode Current.....	-50mA
DC Output Current	50mA
Storage Temperature Range.....	-65°C to +150°C
Junction Temperature.....	150°C
Operating Temperature Range.....	-40°C to +85°C
Lead Temperature (Soldering, 10 sec).....	260°C
ESD Susceptibility	
All Pins.....	4KV

CAUTION

This integrated circuit can be damaged by ESD if you don't pay attention to ESD protection. Broadchip recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

Broadchip reserves the right to make any change in circuit design, specification or other related things if necessary without notice at any time. Please contact Broadchip sales office to get the latest datasheet.

RECOMMENDED OPERATING CONDITIONS

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications.

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply Voltage	2.65	4.3	V
V_{CTRL}	Control Input Voltage(SEL,/OE) ⁽²⁾	0	V_{CC}	V
V_{SW}	Switch I/O Voltage	-0.5	V_{CC}	V
T_A	Operating Temperature	-40	+85	°C

Notes:

1. The input and output negative ratings maybe exceed if the input and output diode current ratings are observed.
2. The control input must be held HIGH or LOW; it must not float.

PIN CONFIGURATION

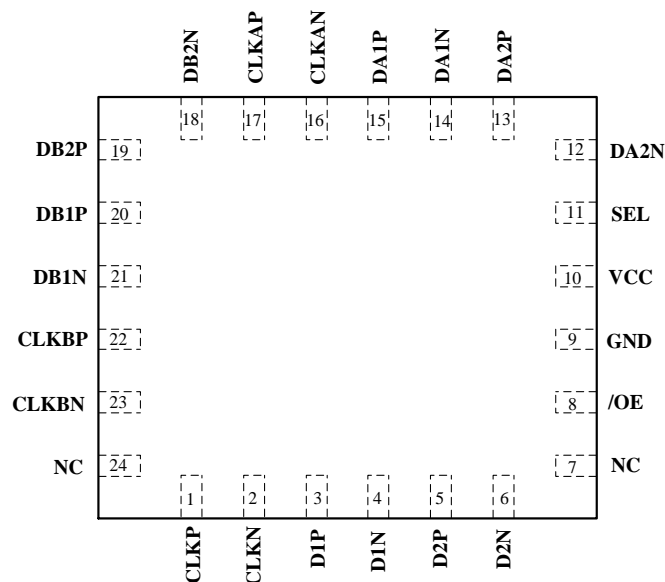


Figure2. Pin Configuration(Top Through View)

PIN DESCRIPTION

PIN	NAME	FUNCTION
1, 2	CLKP, CLKN	Clock Path (Common)
3, 4	D1P, D1N	Data Path 1 (Common)
5, 6	D2P, D2N	Data Path2 (Common)
7, 24	NC	No Connect (Float)
8	/OE	Output Enable (Active Low)
9	GND	Ground
10	VCC	Power
11	SEL	Select (0=A,1=B)
12, 13	DA2N, DA2P	Data Path (A2)
14, 15	DA1N, DA1P	Data Path (A1)
16, 17	CLKAN, CLKAP	Clock Path (A)
18, 19	DB2N, DB2P	Data Path (2B)
20, 21	DB1P, DB1N	Data Path (1B)
22, 23	CLKBP, CLKBN	Clock Path (B)

FUNCTIONAL DIAGRAM

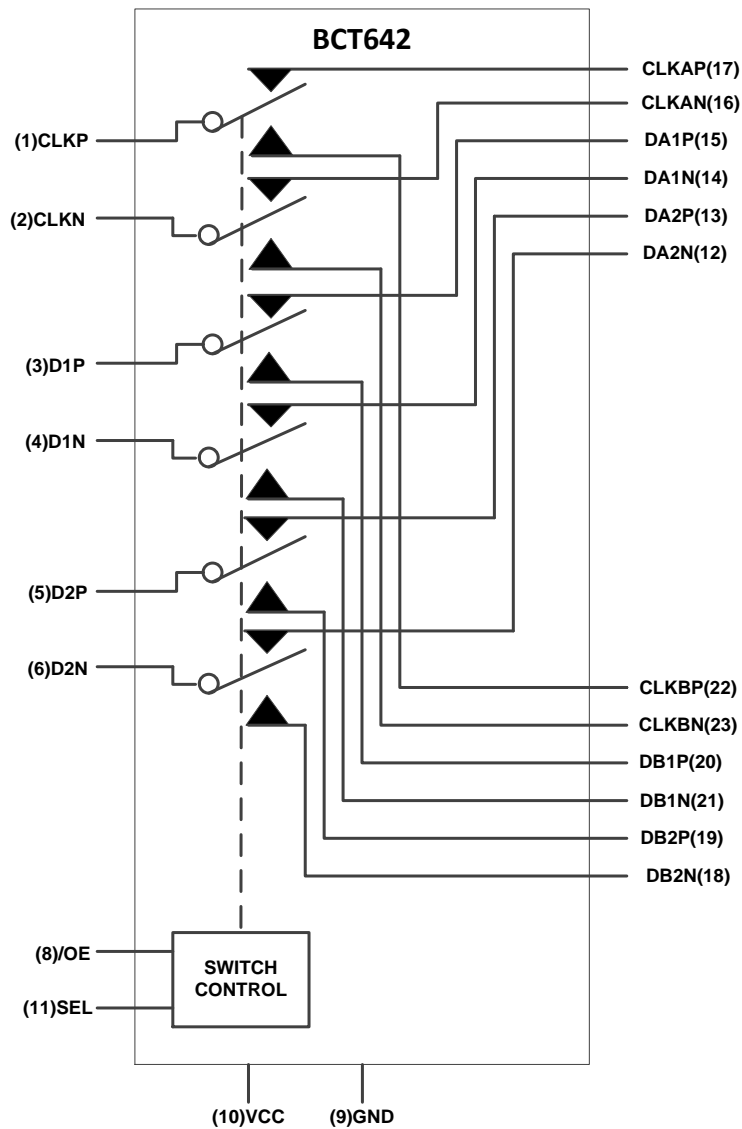


Figure3. Functional Diagram

TRUTH TABLE

SEL	/OE	Function
Don't care	HIGH	Disconnect
LOW	LOW	D1, D2, CLK=DA1, DA2, CLKA
HIGH	LOW	D1, D2, CLK=DB1, DB2, CLKB

DC ELECTRICAL CHARACTERISTICS

(All typical values are $T_A = 25^\circ\text{C}$, unless otherwise specified.)

PARAMETER	SYM	CONDITIONS	V_{CC} (V)	MIN	TYP	MAX	UNITS
Clamp Diode Voltage	V_{IK}	$I_{IN} = -18\text{mA}$	2.775			-1.2	V
Control Input Leakage	I_{IN}	$V_{SW} = 0$ to 4.3V	4.3	-1		1	μA
Input Voltage High	V_{IH}	$V_{IN} = 0$ to V_{CC}	2.65 to 2.775	1.3			V
			4.3	1.7			
Input Voltage Low	V_{IL}	$V_{IN} = 0$ to V_{CC}	2.65 to 2.775			0.5	V
Off-State Leakage	I_{OZ}	$A, B = +0.3\text{V}$ to $V_{CC} - 0.3$	4.3	-2		2	μA
Quiescent Supply Current	I_{CC}	$V_{CNTRL} = 0$ or V_{CC} , $I_{OUT} = 0$	4.3			1	μA
Increase in I_{CC} Current Per Control Voltage and V_{CC}	I_{CCT}	$V_{CNTRL} = 1.8\text{V}$	2.775			1.5	μA

DC ELECTRICAL CHARACTERISTICS, LOW-SPEED MODE

(All typical values are $T_A = 25^\circ\text{C}$, unless otherwise specified.)

PARAMETER	SYM	CONDITIONS	V_{CC} (V)	MIN	TYP	MAX	UNITS
LS Switch On Resistance ⁽³⁾	R_{ON}	$V_{SW} = 1.2\text{V}$, $I_{ON} = -10\text{mA}$	2.65		10	14	Ω
LS Delta R_{ON} ⁽⁴⁾	ΔR_{ON}	$V_{SW} = 1.2\text{V}$, $I_{ON} = -10\text{mA}$ (Intra-pair)	2.65		0.65		Ω

Notes:

3. Measured by the voltage drop between A/B and CLK/Dn pins at the indicated current through the switch.
4. Guaranteed by characterization

DC ELECTRICAL CHARACTERISTICS, HIGH-SPEED MODE

(All typical values are $T_A = 25^\circ\text{C}$, unless otherwise specified.)

PARAMETER	SYM	CONDITIONS	V_{CC} (V)	MIN	TYP	MAX	UNITS
HS Switch On Resistance ⁽⁵⁾	R_{ON}	$V_{SW} = 0.4\text{V}$, $I_{ON} = -10\text{mA}$	2.65		7	9.5	Ω
HS Delta R_{ON} ⁽⁶⁾	ΔR_{ON}	$V_{SW} = 0.4\text{V}$, $I_{ON} = -10\text{mA}$ (Intra-pair)	2.65		0.65		Ω

Notes:

5. Measured by the voltage drop between A, B, and Dn pins at the indicated current through the switch.
6. Guaranteed by characterization

AC ELECTRICAL CHARACTERISTICS

(All values are at $R_L=50\Omega$ and $R_S=50\Omega$ and all typical values are $V_{CC}=2.775V$ at $T_A=25^\circ C$ unless otherwise specified.)

PARAMETER	SYM	CONDITIONS	V_{CC} (V)	MIN	TYP	MAX	UNITS
Off Isolation ⁽⁷⁾	Q_{IRR}	$f=100MHz, R_T=50\Omega$	2.775		-35		dB
Non-Adjacent Channel Crosstalk ⁽⁷⁾	Xtalk	$f=100MHz, R_T=50\Omega$	2.775		-55		dB
-3db Bandwidth ⁽⁷⁾	BW	$C_L=0pF, R_T=50\Omega$	2.775		1.0		GHz
Turn-On Time SEL, /OE to Output	t_{ON}	$C_L=5pF, V_{SW}=1.2V$	2.65 to 2.775		20	37	ns
Turn-Off Time SEL, /OE to Output	t_{OFF}	$C_L=5pF, V_{SW}=1.2V$	2.65 to 2.775		15	27	ns
Propagation Delay ⁽⁷⁾	t_{PD}	$C_L=5pF$	2.775		0.25		ns
Break-Before-Make Time	t_{BBM}	$C_L=5pF$ $V_{SW1}=V_{SW2}=1.2V$	2.65 to 2.775	3	5	8	ns

Note:

7. Guaranteed by characterization.

AC ELECTRICAL CHARACTERISTICS

(All typical values are $V_{CC}=2.775V$ at $T_A=25^\circ C$ unless otherwise specified.)

PARAMETER	SYM	CONDITIONS	V_{CC} (V)	MIN	TYP	MAX	UNITS
Channel-to-Channel Skew Across Multiple Parts ^(8,9)	$t_{SK(Part_Part)}$	$V_{SW}=0.2V$ diff _{PP} , $C_L=5pF$	2.775		40	80	ps
Channel-to-Channel Skew Within a Single Part ⁽⁸⁾	$t_{SK(Chl-Chl)}$	$V_{SW}=0.2V$ diff _{PP} , $C_L=5pF$	2.775		15	30	ps
Skew of Opposite Transitions in the Same Differential Channel ⁽⁸⁾	$t_{SK(Pulse)}$	$V_{SW}=0.2V$ diff _{PP} , $C_L=5pF$	2.775		10	20	ps

Notes:

8. Guaranteed by characterization.

9. Assumes the same V_{CC} and temperature for all device.

CAPACITANCE

PARAMETER	SYM	CONDITIONS	V_{CC} (V)	MIN	TYP	MAX	UNITS
Control Pin Input Capacitance ⁽¹⁰⁾	C_{IN}	$V_{CC}=0V$	0		1.5		pF
Dn/CLK-On Capacitance ⁽¹⁰⁾	C_{ON}	/OE=0V, $f=1MHz$	2.775		7		
Dn/CLK Off Capacitance ⁽¹⁰⁾	C_{OFF}	/OE=2.775V, $f=1MHz$	2.775		2.5		

Note:

10. Guaranteed by characterization.

TEST DIAGRAMS

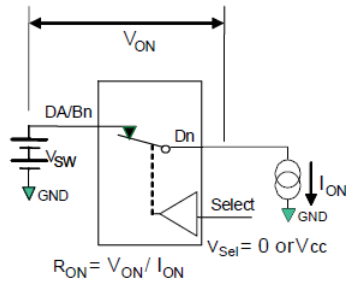
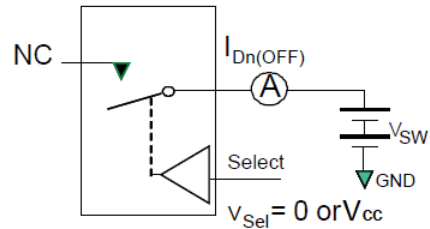
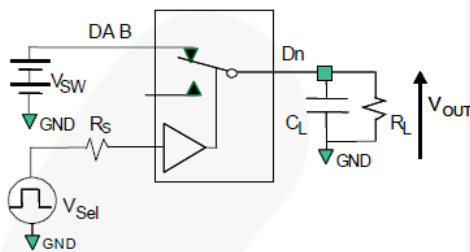


Figure 4. On Resistance



**Each switch port is tested separately

Figure 5. Off Leakage



R_L , R_S , and C_L are functions of the application environment (see AC Tables for specific values). C_L includes test fixture and stray capacitance.

Figure 6. AC Test Circuit Board

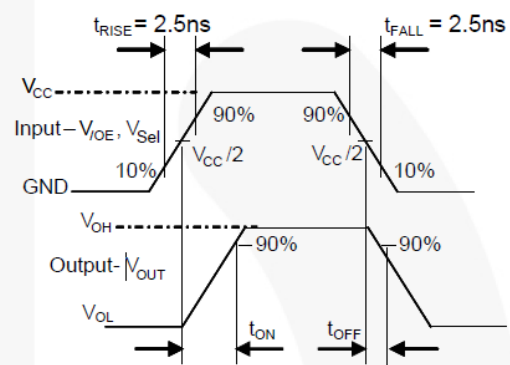


Figure 7. Turn-On/Turn-Off waveform

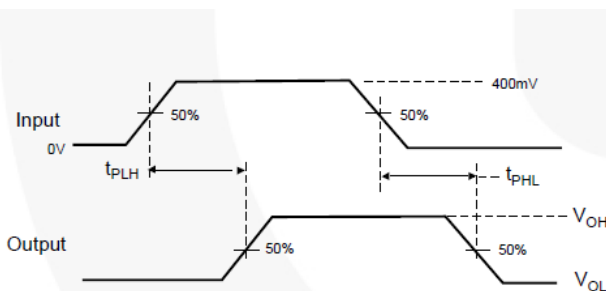


Figure 8. Propagation Delay (t_{RtF} = 500ps)

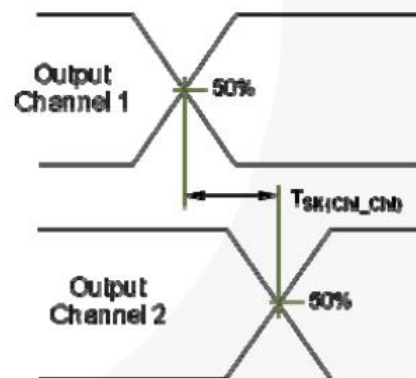


Figure 9. Channel to Channel Skew

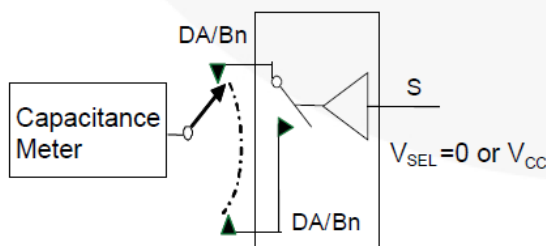


Figure 10. Channel Off Capacitance

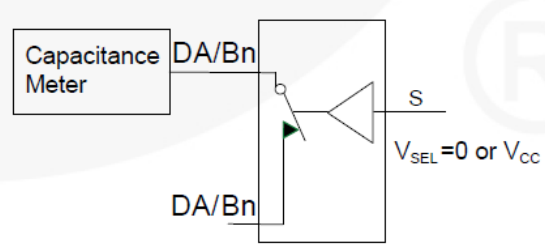


Figure 11. Channel On Capacitance

TEST DIAGRAMS(CONTINUED)

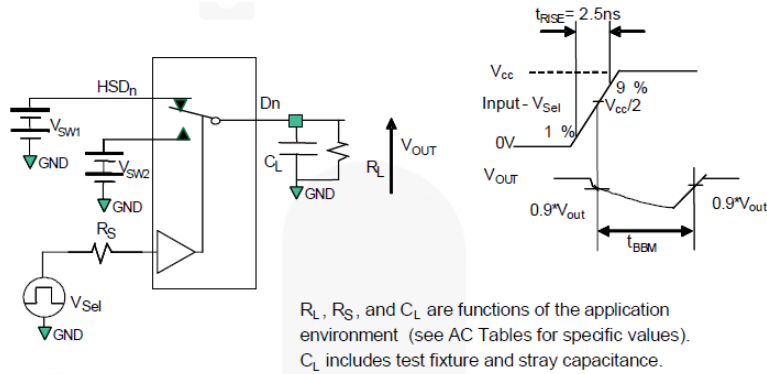


Figure 12. Break-Before-Make Interval Timing

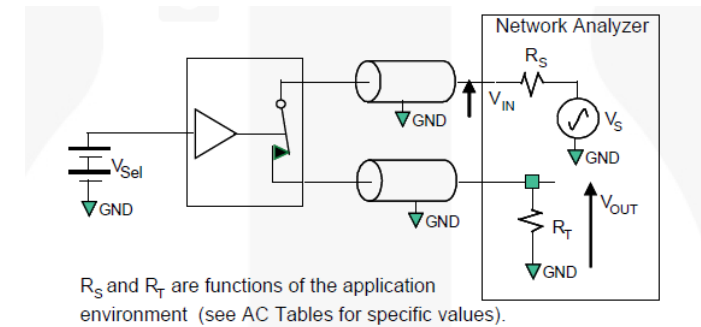


Figure 13. Bandwidth

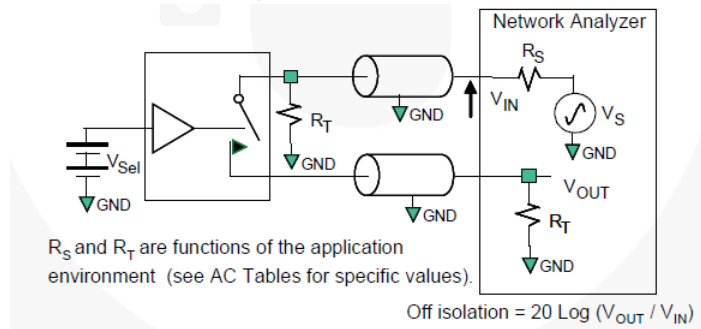


Figure 14. Channel Off Isolation

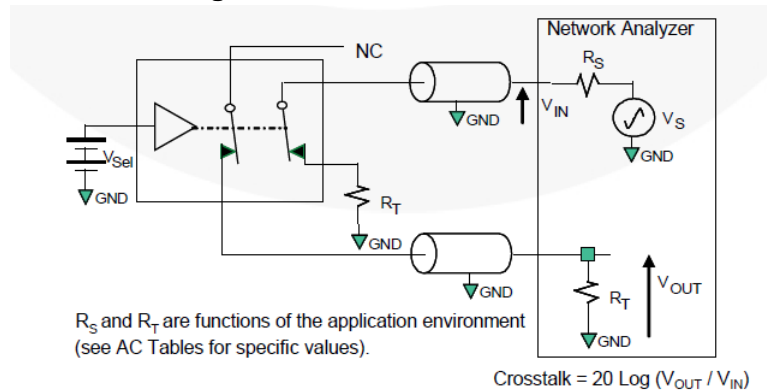
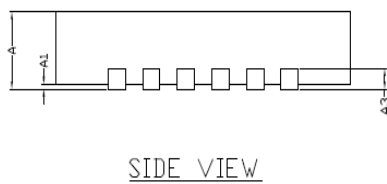
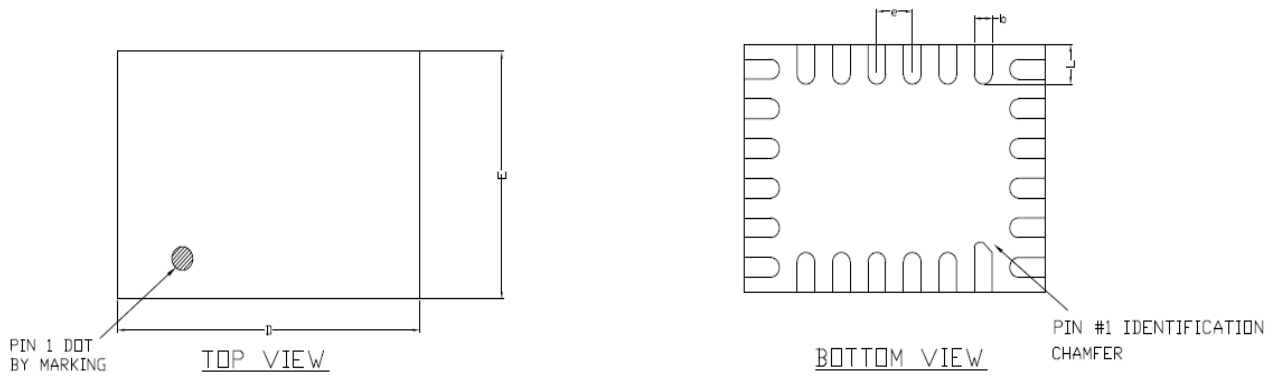


Figure 15. Non-Adjacent Channel-to-Channel Crosstalk

PACKAGE OUTLINE DIMENSIONS



COMMON DIMENSIONS(MM)			
PKG. REF.	W/VERY VERY THIN		
	MIN.	NOM.	MAX
A	0.70	0.75	0.80
A1	0.00	-	0.05
A3		0.2 REF.	
D	3.35	3.40	3.45
E	2.45	2.50	2.55
b	0.15	0.20	0.25
L	0.30	0.40	0.50
e	0.40 BSC		

Remark:

Lead Finish: NiPdAu

Figure 16. 24-Lead QFN(2.5mm x 3.4mm) Package