



## USB Dedicated Fast-Charging Port Controller

### 1 FEATURES

- Support HiSilicon® Fast Charge Protocol(FCP)
- Support Samsung® Adaptive Fast Charging(AFC)
- Support Qualcomm® Quick Charging 3.0/2.0(QC3.0/QC2.0)™ Protocol
- Support USB DCP applying 2.7V on DP and DM line, output Current up to 2.4A for Apple® Device
- Meets Battery Charging Specification BC 1.2 for DCP
- Meets Chinese Telecommunication Industrial Standard YD/T 1591-2009
- Automatic Selection of D+/D- mode for an attached device
- Power Consumption below 1mW at 5V output
- SOT23-6 Package

### 2 APPLICATIONS

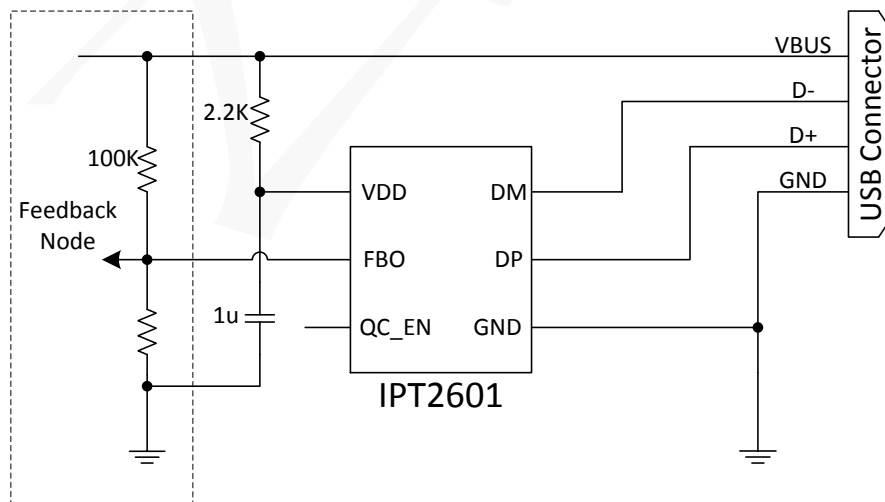
- Adapter
- Car Charger
- USB Power Output Ports
- Power Bank

### 3 DESCRIPTION

IPT2601 is a low-cost USB Dedicated Fast Charging Port Controller which is fully compatible with BC1.2 and other non BC1.2 standards like YD/T 1591-2009 Apple® & Samsung® Charging Spec, HiSilicon® Fast Charge Protocol, Qualcomm® Quick Charging™ 3.0/2.0.

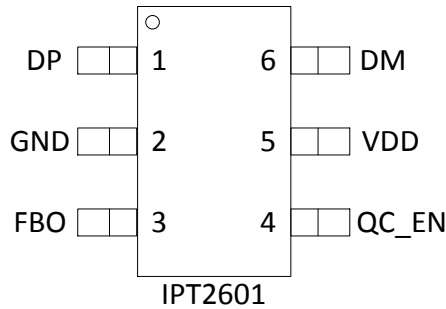
IPT2601 automatically detect whether a connected Power Device(PD) is Quick Charge 2.0/3.0 or FCP Capable before enabling output voltage adjustment. If a PD not compliant to Quick Charge 2.0/3.0 is detected the IPT2601 disables output voltage adjustment to ensure safe operation with legacy 5V only USB PDs. The IPT2601 is available in SOT23-6 package.

### 4 Typical Application Schematic





## 5 PIN FUNCTIONS



NO.	NAME	TYPE	DESCRIPTION
1	DP	I/O	USB positive data line.
2	GND	P	Ground connection.
3	FBO	I/O	Feedback output. Current source/sink output.
4	QC_EN	I	FCP/QC function enable, H-z to enable FCP/QC and LOW to disable.
5	VDD	P	Power supply.
6	DM	I/O	USB negative data line.

## 6 SPECIFICATIONS

### 6.1 ABSOLUTE MAXIMUM RATINGS <sup>(1)</sup>

PARAMETER		MIN	MAX	UNIT
Voltage Range (To PGND)	VDD	-0.3	6.5	V
	Others	-0.3	6.5	V
Operating Junction Temperature	T <sub>J</sub>	-40	150	°C
Storage Temperature Range	T <sub>STG</sub>	-65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 6.2 ESD RATING

SYMBOL	PARAMETER	VALUE	UNIT
V <sub>ESD</sub>	Human Body Model (HBM)	±4000	V

### 6.3 RECOMMENDED OPERATING CONDICTIONS

PARAMETER		MIN	TYP	MAX	UNIT
VDD	Input Supply Voltage	3.2	5	6.4	V
C <sub>VDD</sub>	Input Capacitance	0.47			μF
T <sub>A</sub>	Operation Temperature Range	-40		85	°C



## 6.4 ELECTRICAL CHARACTERISTICS

Conditions are  $T_j = 25^\circ\text{C}$ ,  $V_{DD} = 5\text{V}$ .

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>INPUT POWER</b>						
$V_{VDD}$	VDD Input Voltage Range		3.2		5.5	V
$I_{VDD}$	VDD Supply Current	$V_{DD}=5\text{V}$		200		$\mu\text{A}$
$V_{VDD(\text{SHUNT})}$	VDD Shunt Voltage	$I_{VDD}=3.5\text{mA}$		4.75		V
<b>VDD UVLO Test</b>						
$V_{DD(\text{ON})}$	VDD (turn on threshold voltage)	$V_{VDD}$ Rising	2.9	3.0	3.1	V
$V_{DD(\text{OFF})}$	VDD (turn off threshold voltage)	$V_{VDD}$ Falling	2.8	2.9	3.0	V
$\Delta V_{UVLO}$	UVLO Hysteresis	$V_{DD(\text{ON})} - V_{DD(\text{OFF})}$		0.1		V
<b>High Voltage Dedicated Charging Port (HVDCP)</b>						
$V_{\text{DAT}(\text{REF})}$	Data Detect Voltage		0.25	0.325	0.4	V
$V_{\text{SEL}(\text{REF})}$	Output voltage selection reference		1.8	2	2.2	V
$T_{\text{GLITCH}(\text{DP})\text{HIGH}}$	D+ High Glitch Filter Time		1	1.25	1.5	s
$T_{\text{GLITCH}(\text{DM})\text{LOW}}$	D- Low Glitch Filter Time			1		ms
$T_{\text{GLITCH}(\text{V})\text{CHANGE}}$	Output Voltage Glitch Filter Time		20	40	60	ms
$T_{\text{GLITCH}(\text{CONT})\text{CHANGE}}$	Continuous Mode Glitch Filter Time		100	150	200	$\mu\text{s}$
$R_{\text{DAT}(\text{LKG})}$	D+ Leakage Resistance	$V_{DD}=3.1\text{-}7\text{V}$ , $V(\text{D}+)=0.5\text{-}3.6\text{V}$ , Switch SW1=Off	300	500	800	$\text{K}\Omega$
$R_{\text{DM}(\text{DWN})}$	D- Pull-Down Resistance		14.2	19.5	24.5	$\text{K}\Omega$
$R_{\text{ON}(\text{N1})}$	Switch SW1 on-resistance	$V_{DD}=3.1\text{-}7\text{V}$ , $V(\text{D}+)\leq 3.6\text{V}$ , $I_{\text{DRAIN}}=200\mu\text{A}$		20	40	$\Omega$
$C_{\text{DAT}}$	Data Line Capacitance				1	nF
$V_{\text{TH}(\text{PD})}$	Output Device Connection Detection threshold		0.25	0.325	0.4	V
$T_{\text{DPD}}$	Output Device connection Detection Glitch Filter Time		120	160	200	ms
$\Delta I_{\text{T}(\text{UP})}$	Up Current Step	$R_{\text{IREF}}=100\text{K}\Omega$		2		$\mu\text{A}$
$\Delta I_{\text{T}(\text{DO})}$	Down Current Step	$R_{\text{IREF}}=100\text{K}\Omega$		2		$\mu\text{A}$
$T_{\text{DUR}(\text{step})}$	Duration for current step	QC3.0 mode	80	100	120	$\mu\text{s}$
<b>DCP 1.2V Mode</b>						
$V_{\text{DAT}(1.2\text{V})}$	D+ _1.2V/D- _1.2V line output voltage		1.08	1.2	1.32	V
$R_{\text{DAT}(1.2\text{V})}$	D+ _1.2V/D- _1.2V line output Impedance			100		$\text{K}\Omega$
<b>Apple 2.4A Mode</b>						



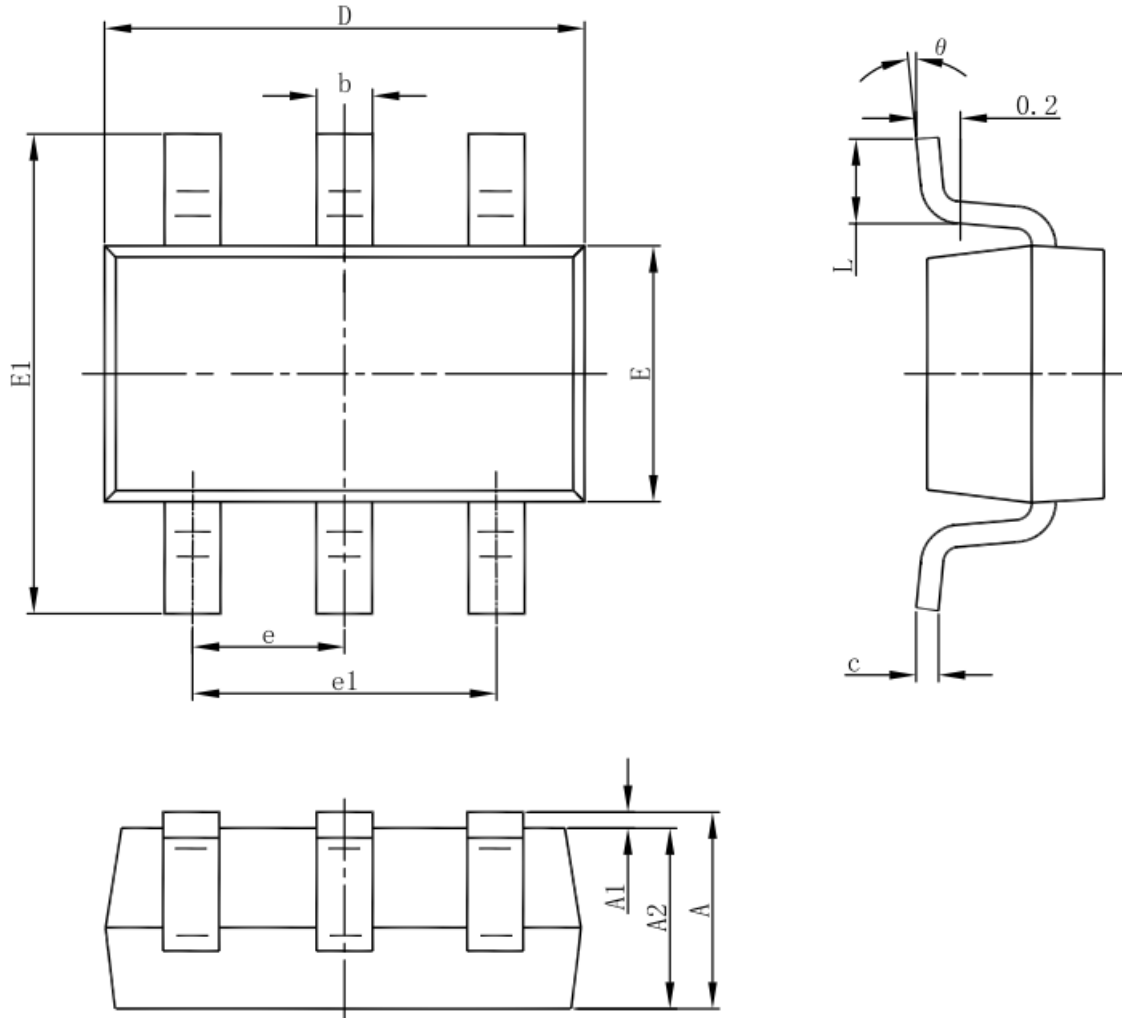
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V <sub>DAT(2.7V)</sub>	D+/D- line output voltage		2.57	2.7	2.84	V
R <sub>DAT(2.7V)</sub>	D+/D- line output Impedance			33.6		KΩ
<b>FCP Mode</b>						
V <sub>TX-VOH</sub>	D- FCP TX Valid High		2.35		3.6	V
V <sub>TX-VOL</sub>	D- FCP TX Valid Low				0.3	V
V <sub>RX-VIH</sub>	D- FCP RX Valid High		1.5		3.6	V
V <sub>RX-VIL</sub>	D- FCP RX Valid High				1.0	V
R <sub>PD</sub>	D- Pull-Down Resistance		400	500	600	Ω
T <sub>UI</sub>	Unit Interval for PHY	F <sub>CLK</sub> =125KHz	144	160	176	us
T <sub>RISE</sub>	FCP Pulse Rise Time	10% - 90%		1	2.5	us
T <sub>FALL</sub>	FCP Pulse Fall Time	90% - 10%		1	2.5	us



## 7 Outline Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950		0.037	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
$\theta$	0°	8°	0°	8°