

Feature

- 3 ~3.6V Power Supply Voltage
- Chip available in MSOP-8 Package
- Power dissipation: 25mA low Power Consumption(3.3V)

Comparator:

- 30ns Propagation Delay (@100mV Overdrive)
- Rail to Rail Output, CMOS/TTL Compatible
- Internal Hysteresis to Ensure Clean Switching
- Low Offset Voltage: +/-3mV Max
- Low HYS Voltage Temperature Drift: 3.6uV/°C

Video Filter:

- 1 channel 6th order 72MHz (-3dB) Butterworth video filter
- 6 dB DC gain
- DC or AC coupled Input
- DC or AC coupled Rail to Rail Output
- Attenuation -20dB @100MHz/-39dB@144MHz

Applications

- TVI FHD Camera and CVI FHD Camera;
- DVD video players, device of communication, Digital Set Top Box, etc.

Block diagram

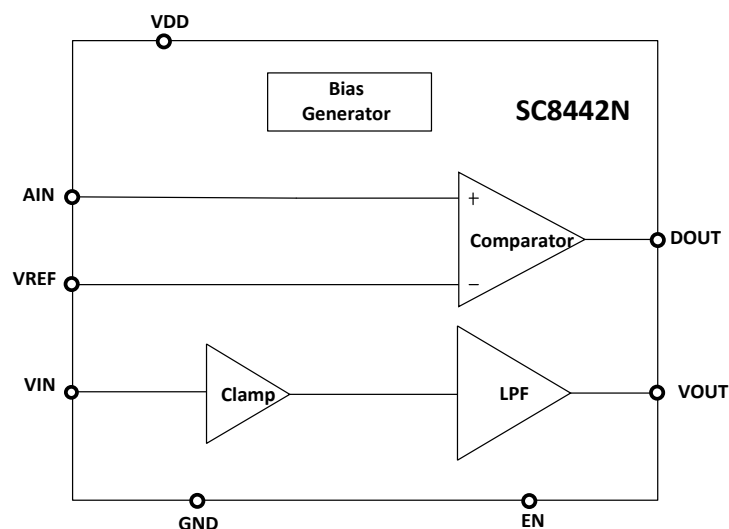


Fig.1 block diagram of SC8442N

REV. 1.0

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Absolute Maximum Ratings

(If out of these ratings, the filter may be fail or damaged)

Table 1

Symbol	Parameter	Rating	units
VDD	Power supply	5.5	V
T _A	Operating ambient Temperature Range	-40~+85	°C
T _{STG}	Storage Temperature	-65~+150	°C

Recommended Operating Conditions

Table 2

Symbol	Parameter	Rating	units
VDD	Power supply	2.7~5.5	V
T _A	Operating ambient Temperature Range	-40~+85	°C

Electrical Characteristics Video Filter Part
DC Characteristics

 (Specifications are at $R_L=150\Omega$, $V_{in}=1V_{pp}$, $T=25\text{ }^\circ\text{C}$, $V_{DD}=3.3V$)

Table 3

Symbol	Parameter	Min	Typ	Max	Units
ICC	Total supply current ($V_{dd}=3.3V$)		16		mA
	Total supply current ($V_{dd}=5V$)		18		
I_Q	Quiescent current ($V_{dd}=3.3V$, NO input & load)		13		mA
Isc	Output short to VDD ($v_{in}=V_{DD}$, Output to VDD)		72		mA
	Output short to GND ($v_{in}=V_{DD}$, Output 10 Ω to GND)		85		mA
Vols	Output Level Shift Voltage ($V_{in}=0V$, no load, input referred)		80		mV
V_{OH}	Output Voltage High Swing ($V_{DD}=3.3V$)		2.8		V
	Output Voltage High Swing ($V_{DD}=5V$)		4.5		V
V_{OL}	Output Voltage Low Swing ($V_{DD}=3.3V/5V$)		240		mV
AV	Output Voltage Gain		6		dB
Iclamp-up	Pull up clamp current		6		mA
Iclamp-down	Pull down clamp current		160		nA
PSRR	Power supply rejection ratio ($f=50Hz$)		58		dB
	Power supply rejection ratio ($f=1MHz$)		36		

AC Characteristics

 (Specifications are at $R_L=150\Omega$, $V_{in}=1V_{pp}$, $T=25\text{ }^\circ\text{C}$, $V_{DD}=3.3V$)

Table 4

Symbol	Parameter	Min	Typ	Max	Unit
BW(-3 dB)	The Band width of -3dB		72		MHz
Att($f=100MHz$)	Stop band Attenuation at 100MHz		-20		dB
Att($f=144MHz$)	Stop band Attenuation at 144MHz		-39		dB
THD	Total Harmonic Distortion(25M , 0.6Vpp)		-48		dB
SNR	Signal to Noise Ratio* ¹		64		dB
T_{GD}	Group Delay Variation [100k~21MHz]		6		ns
Rout	Output Impedance at $f=10MHz$		1		ohm
SR	Slow Rate ($V_{in}=1V$, 20%~80%)		110		V/us

*1: White Signal, 100kHz~30MHz, SNR=20*Log(714mV/RMS noise)

Electrical Characteristics Comparator Part

(Specifications are at VDD=+2.7V ~ +5.5V, Vin+=VDD, Vin-=1.2V, RL=10Kohm, CL=15pF, T=25 °C)

Table 5

Symbol	Parameter	Min	Typ	Max	Units
VDD	Operating Supply Voltage	2.7	3.3	5.5	V
V _{OS}	Input Offset Voltage* ¹	-3	+/-0.15	+3	mV
V _{OS_TC}	Input Offset voltage Temp Drift	0.6	2.0	4.7	uV/°C
V _{hyst}	Input Hysteresis Voltage	4	5	6	mV
V _{hyst_TC}	Input Hysteresis Voltage Temp Drift		3.8	5.4	uV/°C
C _{IN}	Input Capacitance	Differential	1.8		pF
		Common Mode	3.6		
R _{IN}	Input Resistance		>100		GΩ
I _Q	Quiescent Current		251		uA
I _{SC}	Output short to VDD		25		mA
V _{in_cm}	Common mode Input voltage	GND+0.2	-	VDD-0.2	V
V _{OH}	Output Voltage High Swing	VDD-0.3			V
V _{OL}	Output Voltage Low Swing			GND+0.3	V
I _{clamp-up}	Pull up clamp current		6.7		mA
I _{clamp-down}	Pull down clamp current		126		nA
CMRR	Common Mode Rejection Ratio		70		dB
PSRR	Power supply rejection ratio		63		dB
t _R	Rising time		3.5		ns
t _F	Falling time		2.8		ns
T _{PD+}	Propagation Delay(Low to High)		30		ns
T _{PD-}	Propagation Delay(High to Low)		28.5		ns
T _{PDSKEW}	Propagation Delay Skew* ²		1.50		ns

*1: The input offset voltage is the average of the input-referred trip points. The input hysteresis is the difference between the input-referred trip points.

*2: Propagation Delay Skew is defined as: T_{PD+}-T_{PD-}.

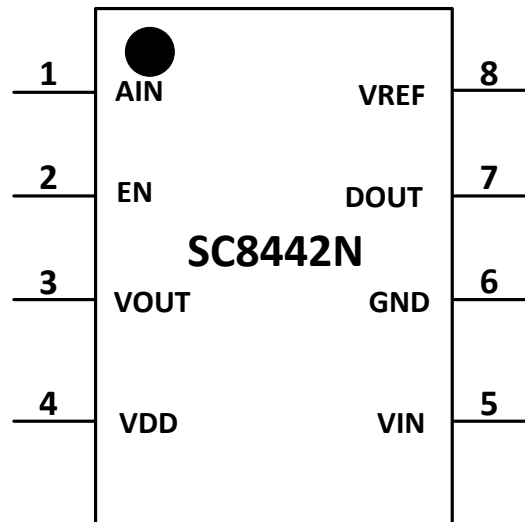
PAD Definition


Fig.2 Pad definition of SC8442N

Table 6 Pad definition

Pin	Name	I/O	Analog/Digital	Description
1	AIN	I	A	Input Signal PAD for Comparator
2	EN	I	A	The whole chip enable control pin, EN=high chip work; EN=low chip shut down;
3	VOUT	O	A	Video Filter output PAD
4	VDD	POWER	POWER	Power supply (3.3V/5V) ,connect to positive voltage supply
5	VIN	I	A	Video signal input PAD, AC coupled, Apply with 80mV Clamp up voltage
6	GND	GROUND	GROUND	Ground pin. Connect to the most negative supply, ALL GND pads are connected on die
7	DOUT	O	A	Comparator Output PAD, High Voltage level is Pulled to VDD, Low Voltage is GND
8	VREF	I	A	The DC reference voltage input PAD for comparator

Application Circuits

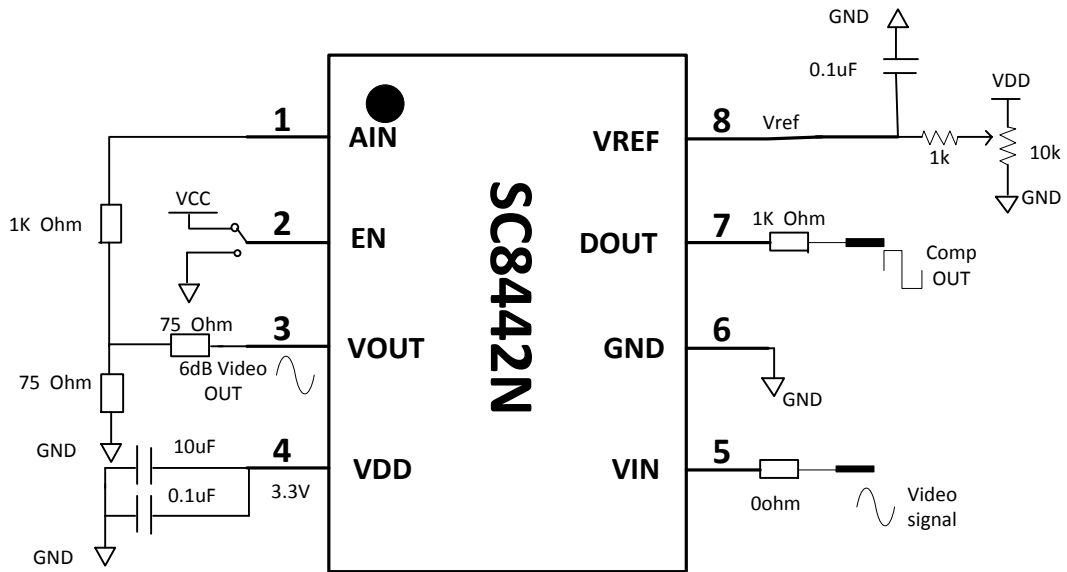
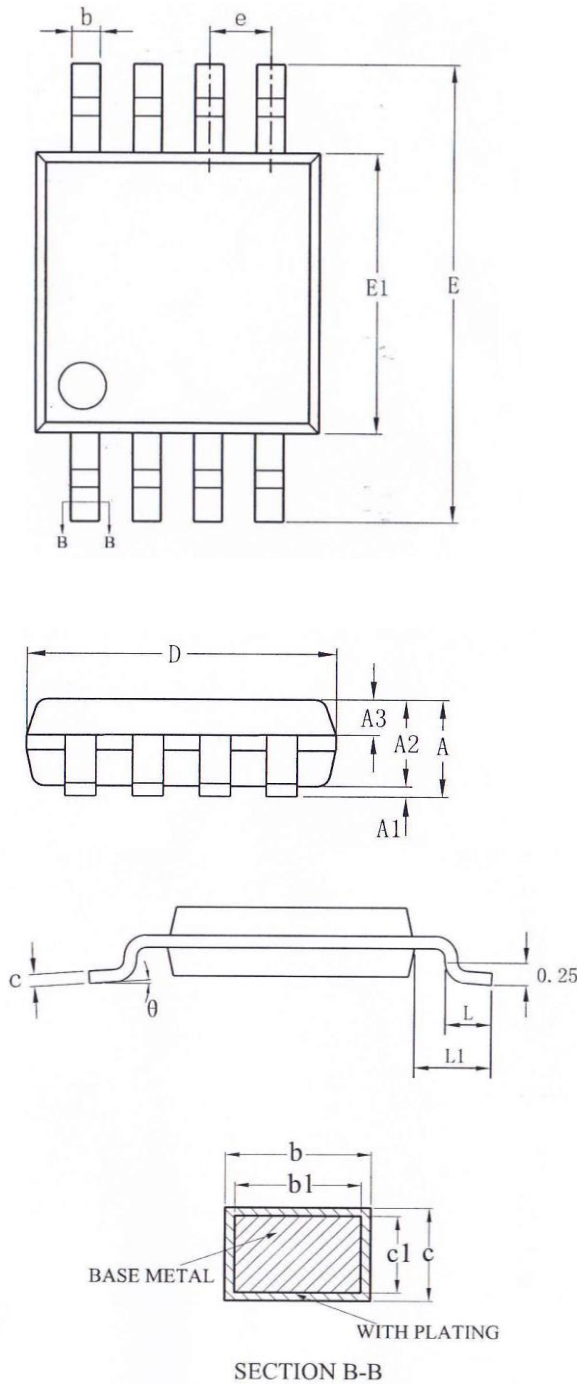


Fig.3 Applications Circuits of SC8442N

Package

MSOP-8



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.10
A1	0.05	—	0.15
A2	0.75	0.85	0.95
A3	0.30	0.35	0.40
b	0.28	—	0.36
b1	0.27	0.30	0.33
c	0.15	—	0.19
c1	0.14	0.15	0.16
D	2.90	3.00	3.10
E	4.70	4.90	5.10
E1	2.90	3.00	3.10
e	0.65BSC		
L	0.40	—	0.70
L1	0.95REF		
θ	0	—	8°

Fig.4 Package of SC8442N

Version History :

Ver.	Modify date	Modify Reason	Author	note
Initial(V1.0)	2017-02-24		nyzhang	